Strained Si/SiGe-on-Insulator (SGOI) RF Power MOSFETs

Personnel
N. Waldron (J. A. del Alamo)

Sponsorship
DARPA

This project proposes to use the emerging strained Si/SiGe MOSFET technology to develop high performance RF power devices that can operate in the 10-20 GHz range at power levels of hundreds of milliwatts. Such devices will rival the performance of GaAs technology which has predominantly been used to fulfill the power amplifier function of wireless communication products. Strained-Si technology can be achieved at a lower cost and has the potential for System-On-Chip (SOC) integration.

The basis for the superior performance of strained Si/SiGe MOSFET technology is that it exhibits an enhancement in the fundamental transport properties of Si resulting in improved device speed and power dissipation. Stress in a thin Si layer can by introduced by means of epitaxially growing thin Si on a relaxed SiGe buffer layer. The strain induced from the lattice mismatch between the Si and SiGe layers results in improved carrier transport through the thin Si film for both holes and electrons. Recent experimental work has shown increases of up to 80% in the low field mobility of n-MOSFETs. The incorporation of an insulator layer underneath the stack (as in SOI) offers the further benefits of lower capacitance and improved power efficiency.

The device technology on which the design will be based is that of the Laterally Double Diffused MOSFET (LDMOSFET). The LDMOSFET has shown to be very promising for fulfilling the RF power amplifier function. One of the ground rules of this design is that it be as compatible as possible with a strained-Si CMOS process in order to enable SOC technology. A key issue is then that the CMOS devices are expected to have a gate oxide thickness on the order of 2nm while the LDMOSFET will require a gate oxide thickness on the order of 10nm. We have investigated two options for the LDMOSFET gate oxide by means of a simple capacitor flow. One composite oxide scheme where the initial 2nm of oxide was grown by a thermal step and then the remainder 8nm deposited by means of LTO. In the second option the strained-Si was grown to a thickness greater than the theoretical critical thickness limit. of about 12nm and the entire 10nm gate oxide was then grown by a dry/wet/dry thermal oxidation process. The interface trap density (D_{it}) of both options was measured by means of the parallel conductance method. The Dit of the composite oxide was $4x10^{11}cm^2eV^{-1}$ as measured near flatband and $1.5x10^{11}cm^2eV^{-1}$ near midgap. For the fully thermal oxide the results were $1.7x10^{11}cm^2eV^{-1}$ and $1x10^{11}cm^2eV^{-1}$ near flatband and midgap respectively. A high frequency capacitance curve for both schemes is shown in Figure 9. Both schemes seem to be acceptable for the gate oxide option in the process.

Other process modules that are currently being investigated include the formation of the n-drift region which is required for high breakdown performance and the body doping profile which is required for high transconductance and fT.

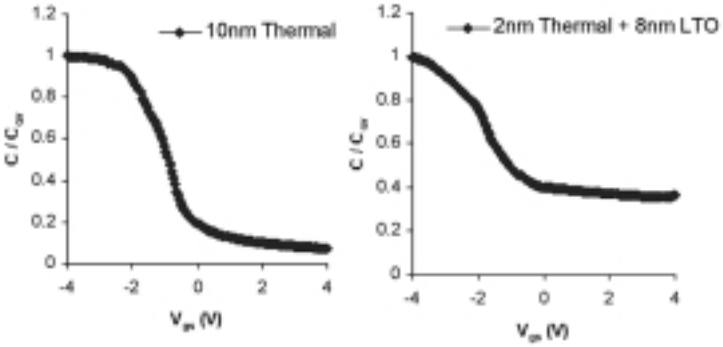

Fig. 9: High frequency capacitance measurements for the fully thermally grown oxide and composite oxide schemes. The C/C_{ox} minimum is different for both options as the substrate doping was ~$2e^{17}$ cm^{-3} for the composite oxide scheme and ~$1e^{15}$ cm^{-3} for the fully thermal oxide.