Exploring Transport in Ultra-Thin Silicon Films for Double-Gate CMOS

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Deeply scaled Double-Gate (DG) and Ground-Plane (GP) MOSFETs require ultra-thin silicon channels in order to maintain electrostatic integrity. Experimental evidence has shown reduced mobility compared to bulk for silicon films between 15 nm and 7 nm. However, theory indicates that between 5 nm and 3 nm increased occupancy of the 2-fold valleys results in increased mobility compared to bulk. This work seeks to gather experimental evidence for the increased mobility in sub-5 nm films.

A schematic of a process to build ultra-thin channel DG/GP MOSFETS is shown in Figure 8. Starting with SOI wafers (1-1), LOCOS isolation is performed (1-2), followed by silicon thinning(1-3). Then a gate oxide is grown, polysilicon is deposited, and the over-sized bottom gates are patterned (1-4). LTO is then deposited, planarized (1-5), and the wafer is bonded to a handle wafer (1-6). The bulk of the original SOI wafer is then removed by mechanical grinding and chemical etching, using the buried oxide as an etch stop. The buried oxide is then removed with a timed etch, exposing the silicon channel (1-7). The top gate oxide is grown, polysilicon is deposited, and the short top gate is patterned (1-8). Spacers are defined (1-9), followed by raised source/drain growth (1-10). Salicide is then formed (1-11). Interconnects are added to finish the device.

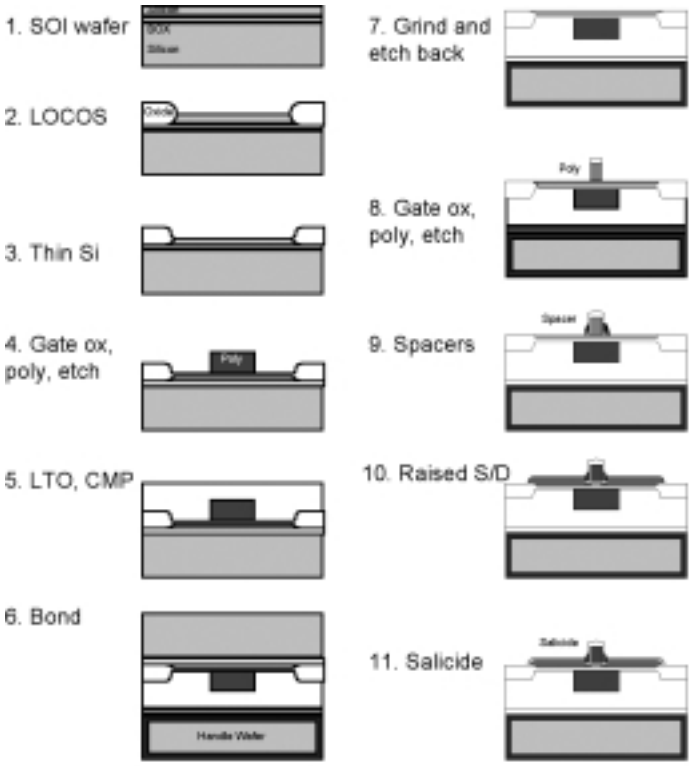

Fig. 8: