Measurements and Simulation of RF Power CMOS

Personnel
J. Scholvin (J.A. del Alamo)

Sponsorship
GCD and IBM

The vision of future System-On-Chip (SOC) integration of wireless systems is to have both the digital baseband and the analog transceiver integrated onto a single chip. For short-range wireless systems, CMOS is a strong candidate because it offers the cheapest manufacturing cost of all technologies. However, the conventional vision of wireless SOC leaves the Power Amplifier (PA) off chip. Our goal is to determine what it takes to integrate the PA onto a standard CMOS SOC and when it makes sense to do this.

To reach this goal, a precise model and good understanding of the device technology is necessary. The work presented here focuses on the measurement and characterization of RF Power CMOS.

We have characterized 0.25 µm CMOS devices manufactures at a standard foundry for their DC, AC and power behavior. The power measurements were taken at a frequency of 2.45 GHz. Typical results are shown in Figure 7. The data shown is the transducer gain (Gain) and the device linearity (IM_3), both as a function of the output power (P_{out}). This graph also includes simulations using the foundry-supplied BSim3v3 and an improved model that we have developed. We can see that the BSim3v3 by itself does not accurately model the power behavior of the Gain and IM_3. It is to correct this deficiency that we have developed a new model that is entirely derived from small signal measurements. The new model is shown in the figure inset.

For a model that is applicable over a wide range of devices and bias conditions, it is important to use physically meaningful parameters. Starting with the BSim3v3 as the core without modifying it, we can add physically meaningful elements around it to build an RF model. The model contains four groups of elements. The gate resistance is an important element found in all RF models, since for power, the unit finger width of the devices must be large enough. Another common aspect of effective RF models is a substrate network. A wide range of topologies has been published modeling the substrate. For the devices we used, it is sufficiently accurate to use a single resistor rather than a more complicated R-C network. Terminal inductances on the gate, source and drain are also necessary to deliver accuracy at frequencies above 10 GHz. While this is far above the frequency of interest for the device operation, it is necessary in the development of the model since high frequencies allow an accurate extraction of the gate resistance. Finally, an additional output resistance helps to compensate for discrepancies in the output conductance predicted by the model, probably as a result of self-heating and weak impact ionization. As seen in the figure, the new model does an excellent job in predicting the RF power measurement even though it was entirely derived from small-signal characterization.

The approach and results demonstrated in this work will be instrumental in developing accurate device models and in understanding the connections between model parameters and topology, device design and device operation for RF Power CMOS.

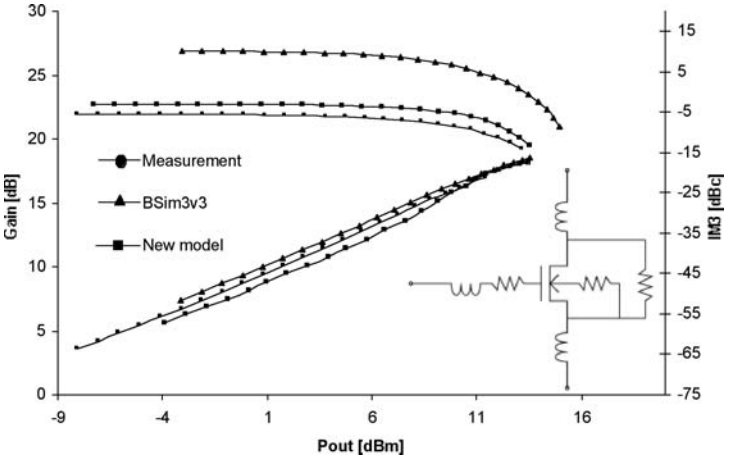

Fig. 1: Large signal measurements and simulations for a 0.25 µm CMOS device (16 fingers, 20µm unit finger width). The insert shows the improved RF model topology.