CMOS Technology for 25 nm Channel Length

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Sponsorship
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The Double-Gate (DG) MOSFET (Figure 4) is considered a promising device for CMOS scaling to deep sub-100 nm gate lengths. However, realization of the ideal DG-MOSFET structure involves significant technological challenges, particularly formation and alignment of the upper and lower gates. We employ a direct alignment approach, known as Interferometric-Broad-Band-Imaging (IBBI), to form upper-gates with correct relative placement to the lower-gates. We have demonstrated this scheme at 150 nm upper-gate length with alignment to within 5 nm. Figure 5 displays this result by demonstrating the upper-gate in resist and the lower-gate as polySi embedded in LTO.

Our alignment detectivity is on the order of a nanometer. However, our final alignment results are equally a function of precise pattern placement on the upper and lower-gate x-ray masks. We use a scheme of close proximity x-ray mask replication to transfer patterns directly from upper-gate mask to lower-gate mask. This allows us to create a mask pair containing patterns that overlay one another to high precision. The two major challenges in this scheme are: 1) the pattern on the replicated mask must be of the same polarity as that on the source, and 2) it is necessary to maintain sub-100 nm resolution. Maintaining pattern polarity is a subtle yet crucial aspect of this process. It involves: X-ray patterning of positive resist, liftoff (yielding a pattern reversal), etch down through polymer layer (forming trenches) and finally, Au electroplating within those trenches. Figure 6 shows this result: a sub-100 nm Au line on a replicated lower-gate mask. The current focus of the project is move to a higher resolution mask set and improve the spatial range over which these exceptional alignment results exist.

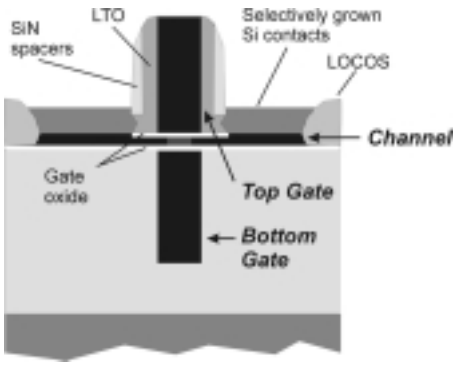

Fig. 4: Schematic of Double-Gate (DG) NMOS transistor.

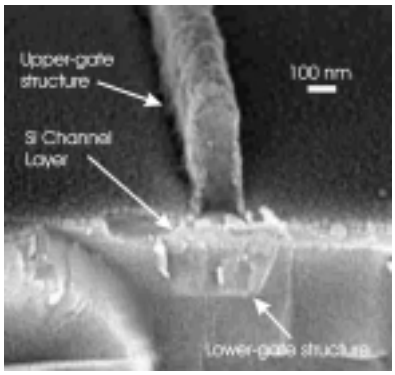

Fig. 5: Double-gate structure demonstrating the required 5 nm alignment of upper-to-lower gate structures.

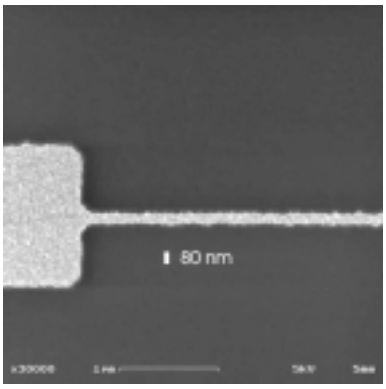

Fig. 6: Demonstration of the x-ray mask replication process. This is a sub-100 nm gold gate feature on a replicated lower-gate x-ray mask.