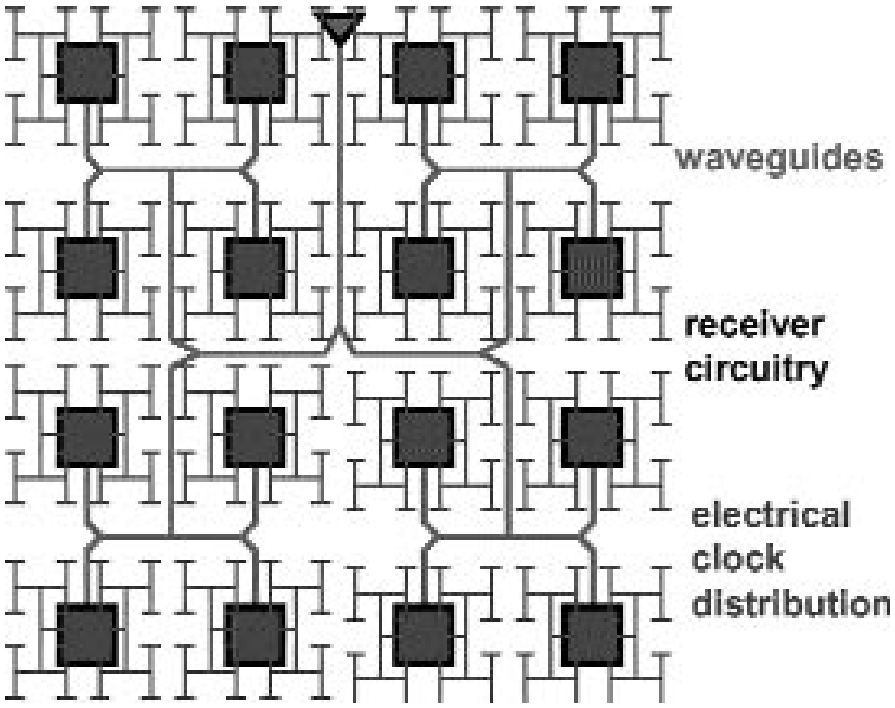
Opposite Page:
On-chip optical clock distribution.
Courtesy of S. L. Sam (D. Boning and A. Chandrakasan)

Modeling and Simulation



Modeling and Simulation

- *Modeling of Advanced Devices*
- *Efficient 3-D Interconnect Analysis*
- *Numerical Techniques for Integral Equations*
- *Modeling of Grain Growth in Thin Films and Nano-Structures*
- *Simulation of and Experimental Characterization of Electromigration-Induced Failure of IC Interconnects*
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- *Modeling of Copper Chemical Mechanical Polishing*
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Modeling of Advanced Devices

Personnel
I. J. Djomehri
(D. A. Antoniadis)

Sponsorship
SRC

Direct quantitative 2-D profile characterization of sub-100 nm MOSFETs continues to be elusive. This research develops a comprehensive indirect inverse modeling technique for extracting the 2-D device topology using combined log(I)-V and C-V data. An optimization loop minimizes the error between a broad range of simulated and measured electrical characteristics by adjusting parameterized doping profiles. The extracted profiles are reliable in that they exhibit decreased RMS error as the doping parameterization becomes increasingly comprehensive of doping features.

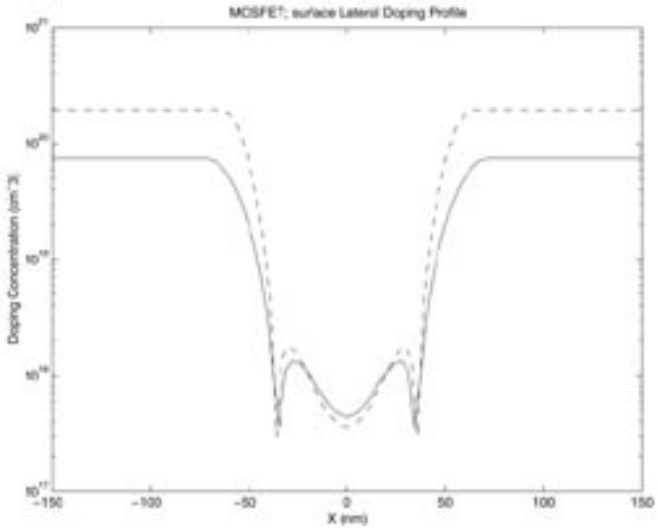

Fig. 1: Comparison between the extracted lateral doping profiles at the surface using combined "I-V & C-V" data (solid line) versus "I-V Only" data (dashed line). This nFET device has L = 90 nm, T_{ox} = 45 A.

The inverse modeling methodology is a formal algorithm that pieces together complementary MOSFET data sets such as Cgg of the gate stack, process simulation for initial guess, 1-D doping analysis, subthreshold I-V which is a strong function of 2-D doping (especially in the channel), and C-V data. To accelerate convergence and improve sensitivity, we have found that utilizing Cgsd-V data detects device features especially in depleted source/drain regions and gate overlap. Figure 1 shows how combining the data sets enhances the extracted profile of a 90 nm NMOS device fabricated at MIT.

An important use of this technique is in the calibration of carrier transport models. With an accurate device topology known from inverse modeling, the transport model parameters can be adjusted to predict the device behavior. Utilizing a mobility model that conforms to the experimental effective field dependence and including a correction for parasitic resistance, the engineer calibrates for instance the drift-diffusion model for an advanced NMOS generation at various lengths as in Figure 2. Employing the hydrodynamic model can yield an energy relaxation value valid over all device nodes.

The main advantages of this technique include: (1) high resolution descriptions of the 2-D (and potentially 3-D) profiles of very small devices; (2) extracting key features (e.g., effective channel length, doping level); (3) low dependence on mobility model; and (4) non-destructive measurement. Future directions include further inverse modeling of state-of-the-art MOSFETs and evaluating their process technologies.

Fig. 2: The leakage current Ioff versus drive current Ion curve of a

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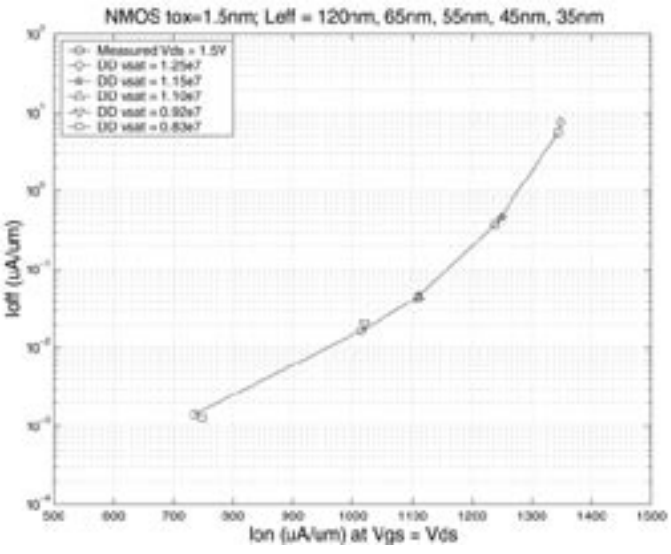
Efficient 3-D Interconnect Analysis



state-o148f-the-art NMOS family with T_{ox} = 15A. The drift-diffusion transport model has been adjusted using the inverse modeled profile to match the experimental results for various L_{eff} nodes.

Personnel

Balk, L. Daniels, J. Kanapka, T. Klemas, J. Li, M.Rewienski, and J. Wang (J. White)

Sponsorship

SRC and MARCO Focused Research Center on Interconnect (SRC/DARPA)

We have developed multipole-accelerated algorithms for computing capacitances and inductances of complicated 3-D geometries, and have implemented these algorithms in the programs FASTCAP and FASTHENRY. The methods are accelerations of the boundary-element or method-of-moments techniques for solving the integral equations associated with the multiconductor capacitance or inductance extraction problem. Boundary-element methods become slow when a large number of elements are used because they lead to dense matrix problems which are typically solved with some form of Gaussian elimination. This implies that the computation grows as N cubed, where N is the number of panels or tiles needed to accurately discretize the conductor surface charges. Our new algorithms, which use Krylov subspace iterative algorithms with a multipole approximation to compute the iterates, reduces the complexity so that accurate multiconductor capacitance and inductance calculations grow nearly as NM where M is the number of conductors. For practical problems which require as many as 10,000 panels or filaments, FASTCAP and FASTHENRY are more than two orders of magnitude faster than standard boundary-element based programs. Manuals and source code for FASTCAP and FASTHENRY are available from our web site (http://rle-vlsi.mit.edu).

In more recent work, we have been developing an alternative to the fast-multipole approach to potential calculation. The new approach uses an approximate representation of charge density by point charges lying on a uniform grid instead of by multipole expansions. For engineering accuracies, the grid-charge representation has been shown to be a more efficient charge representation than the multipole expansions. Numerical experiments on a variety of engineering examples arising indicate that algorithms based on the resulting "precorrected-FFT" method are comparable in computational efficiency to multipole-accelerated iterative schemes, and superior in terms of memory utilization. The precorrected-FFT method has another significant

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advantage over the multipole-based schemes, in that it can be easily generalized to some other common kernels. Preliminary results indicate that the precorrected-FFT method can easily incorporate kernels arising from the problem of capacitance extraction in layered media. More importantly, problems with a Helmholtz equation kernel have be solved at moderate frequencies with only a modest increase in computational resources over the zero-frequency case. An algorithm based on the precorrected-FFT method which efficiently solves the Helmholtz equation could form the basis for a rapid yet accurate full-wave electromagnetic analysis tool.

Reduced-order modeling techniques are now commonly used to efficiently simulate circuits combined with interconnect. Generating reduced-order models from realistic 3-D structures, however has received less attention. Recently we have been studying an accurate approach to using the iterative method in the 3-D magnetoquasistatic analysis program FASTHENRY to compute reduced-order models of frequency-dependent inductance matrices associated with complicated 3-D structures. This method, based on a Krylov-subspace technique, namely the Arnoldi iteration, reformulates the system of linear ODE's resulting from the FASTHENRY eqquation into a state-space form and directly produces a reduced-order model in state-space form. The key advantage of this method is that it is no more expensive than computing the inductance matrix at a single frequency. The method compares well with the standard Pade approaches and may present some advantages because in the Arnoldi-based algorithm, each set of iterations produces an entire column of the inductance matrix rather than a single entry, and if matrix-vector product costs dominate then the Arnoldi-based algorithm produces a better approximation for a given amount of work. Finally, we have shown that the Arnoldi method generates guaranteed stable reduced order models, even for RLC problems.
Another approach to computing these reduced order models are the Truncated Balanced Realization (TBR) methods. These methods have largely been abandoned for the interconnect model-order reduction application, even though they produce optimal reduced-order models, because TBR requires the solution of a Lyapunov equation and has been believed to be too computa-tionally expensive to use on large problems. We recently developed a new algorithm, Vector ADI, for approximately solving the Lyapunov equation. The new method is formulated in terms of finding an orthnormal basis for a Krylov subspace based on rational functions of the system matrix. The new method requires work comparable to the Arnoldi methods, but produces reduced-order models that are near the TBR optimum.

Additional recent work has focussed on fast techniques of model reduction which automatically generate low order models of the interconnect directly from the discretized Maxwell's equations under the quasistatic assumption. When combined with with fast potential solvers, the overall algorithm efficiently generates accurate models suitable for coupled circuit-interconnect simulation.

Also in this area, we have been investigating techniques analyzing coupling problems in single chip mixed-signal systems, where both analog and digital functional blocks share a common substrate. A major challenge for mixed-signal design tools is the accurate modeling of the parasitic noise coupling through the common substrate between the high-speed digital and high-precision analog components. We recently developed a wavelet-like approach which makes it possible to reduce the time and memory required to compute the interactions between N substrate contacts from order N squared down to order N log N.

Numerical Techniques for Integral Equations

Personnel

B. Buchmann, T. Korsmeyer, J. Tausch, and J. Huang
(J. White)

Sponsorship

SRC and MultiUniversity Research Intiative

Finding computationally efficient numerical techniques for simulation of three dimensional structures has been an important research topic in almost every engineering domain. Surprisingly, the most numerically intractable problem across these various discplines can be reduced to the problem of solving a three-dimensional potential problem with a problem-specific Greens function. Application examples include electrostatic analysis of sensors and actuators; electro- and magneto- quasistatic analysis of integrated circuit interconnect and packaging; and potential flow based analysis of wave-ocean structure interaction.

Although the boundary element method is a popular tool to solve the integral formulation of many three-dimensional potential problems, the method become slow when a large number of elements are used. This is because boundary-element methods lead to dense matrix problems which are typically solved with some form of Gaussian elimination. This implies that the computation grows as cubically with the number of unknowns tiles needed to accurately discretize the problem. Over the last decade, algorithms with grow linearly with problem size have been developed by combining iterative methods with multipole approximations. Our work in this area has been to develop precorrected-FFT techniques, which can work for general Greens functions, and Wavelet based techniques, which generate extremely effective preconditioners which accelerate iterative method convergence.

The development of fast boundary-element based solvers has renewed interest in developing well-conditioned integral formulations for a variety of engineering problems. In the past year, we have developed a novel surface-only formulation for quasistatic and full-wave analysis of interconnect. The new approach eliminates some of the low-frequency ill-conditioning problems associated with previous efforts. In addition, we developed an new formulation based on fictious magnetic charge for including nonconductive magnetic materials in an integral formulation for inductance extraction.

Modeling of Grain Growth in Thin Films and Nano-Structures

Personnel

W. Fayad and M. Kobrinsky
(H.J. Frost and C.V. Thompson)

Sponsorship

NSF and SRC

We have developed computer simulations for normal and abnormal grain growth during deposition and subsequent heat treatments of polycrystalline thin films. We have included the effects of grain boundary drag due to surface grooving and due to the presence of solutes. The former leads to stagnation of normal grain growth at a point where the grain sizes are lognormally distributed and the average grain diameter is about three times the film thickness. This simulation result closely matches experimental results in a wide variety of systems. To account for observations of texture evolution during abnormal grain growth in thin films, we have included the effects of surface, interface, and strain energy anisotropy in our simulations of grain growth in films. These simulations allow investigations of the effect of energetic anisotropies on the evolution of texture and grain orientation distributions, as well as on the evolution of the average grain size and the distribution of grain sizes. Predictive simulations of the evolution of the distribution of grain sizes and orientations can be made as a function of materials selection, film thickness, and processing conditions, in both continuous and patterned films.

We have recently used simulations of grain growth in 2D strips to develop analytic models for the evolution of grain structures in interconnect structures (rectangular prisms). We have focused on the evolution from polycrystalline structures with grain boundaries lying along the length of an interconnect, to 'bamboo' structures in which all grain boundaries span the width and thickness of the line, dividing the line into bamboo-like segments. The resulting analytic model provides a compact means for predicting the effects of post-patterning anneals on the grain structure of interconnects. The grain structure of interconnects strongly affects the rate of electromigration, and therefore strongly impacts their reliability. Analytic models for grain structure evolution are used with simulations of electromigration to make process and structure-sensitive reliability predictions.

To developed models with improved accuracy for grain structure evolution in rectangular prisms with near-unit aspect ratio, evolution of soap froths in rectangular prisms was characterized. Three phases of the evolution to bamboo grain structures were identified: an *incubation* period during which the structure is polygranular, a *nucleation* regime during which grains grow to span the prism cross-section and become bamboo grains, and a *steady-state* regime during which the clusters of bamboo grains grow at the expense of the clusters of non-bamboo grains (polygranular clusters). When the prism width-to-thickness ratio w/h is greater than 1.5, the conversion of the 3D grain structure to a 2D (columnar) grain structure occurs primarily during the incubation phase and the early part of the nucleation phase. When w/h~1.0, the conversion from 3D grain structures to 2D structures continues throughout the evolution to fully-bamboo structures. The kinetics of the evolution was shown to scale with μ/w^2 (with w being the largest of the two prism cross-sectional dimensions and μ being the grain boundary mobility). It was found that the duration of the incubation phase becomes longer as the aspect ratio w/h approaches 1. It was observed, and demonstrated using a dimensional analysis, that the nucleation rate is proportional to μ/w^3, and that the polygranular cluster shrinkage velocity is proportional to μ/w. The latter is shown to be constant during the steady-state regime, and higher for 3D clusters, due to the effects of compound boundary curvature. The polygranular cluster length distribution remains well fit by an exponential distribution during the evolution toward fully-bamboo structures and reaches, in the steady-state, a constant distribution with an average cluster length of approximately 1.5 w in all cases. The final bamboo structure is characterized by a grain length distribution scaling with w and with an average value of approximately 1.5 w. A prism-

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geometry-sensitive analytic model for the transformation to full-bamboo grain structures, based on a system of coupled differential equations, was developed and validated through comparisons with experimental results.

Simulation of and Experimental Characterization of Electromigration-Induced Failure of IC Interconnects

Personnel

V. Andleigh, W. Fayad, C. Hau-Riege, S. Hau-Riege, C.L. Gan, F. Wei, Z. Choi, K.L. Pey, W.K. Coi, C.V. Thompson

Sponsorship

SRC

We have developed a software tool for structure-sensitive simulation of electromigration and electromigration-induced failure of interconnects, MIT/EmSim. A web-based version of this tool, EmSim-Web, can be accessed at http://nirvana.mit.edu/emsim/. The tool generates grain structures with known statistical variations as a function of median grain size and line width, and predicts failure statistics as a function of various failure criteria, and as a function of the current density and of the temperature. The effects of wide-to-narrow transitions, junctions, and thermal history have also been included, and have been tested through comparison with experiments carried out on Al-based interconnects. Experiments on Cu-based interconnects processed at Sematech and IME (Singapore) are currently being carried out.

In the conventional interconnect reliability assessment methodology, accelerated lifetime tests are carried out at elevated current densities and temperatures, and specific scaling behavior is assumed in predicting lifetimes at in-service current densities and temperatures. For example, it is assumed that lifetimes scale with the current density j to the power -2 for void-nucleation-limited failure, and j to the power -1 for void-growth-limited failure. Using simulations we have shown that there can be a transition in scaling behavior in going from to test to service conditions, leading substantial scaling errors when this is not accounted for. Further, we have shown that short lines can display conventional scaling behavior at test conditions but be immune to failure at service conditions. These simulation results are consistent with a growing body of experimental results. This complex behavior must be accounted for in order to make accurate reliability projections, and in order to take advantage of the greatly improved reliabilities of short lines. To catalog scaling behavior we have developed 'failure-mechanism maps' which show the scaling behavior as a function of current density and line length. Such maps can be used in reliability assess-

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ments and in developing optimum circuit layout strategies. MIT/EmSim can be used to generate these maps for different metallization materials and processes.

In the last year, electromigration tests were performed on Cu/Ta interconnect structures which were fabricated in MTL, IME (Singapore), and Sematech. These Cu experiments demonstrated a similar void nucleation and growth process as has been observed in Al interconnects. The results from these experiments allowed the determination of several Cu electromigration parameters necessary to complete the development of a Cu electromigration model, and these were incorporated into MIT/EmSim. Simulation of electromigration in Cu interconnects based on this revised model show that a knowledge of the current density exponent behavior is critical for evaluating the reliability of Cu at service conditions based on accelerated test data. Furthermore, trends in comparisons of Al and Cu failure data at accelerated conditions may not necessarily be evident at service conditions due to a change in current density exponents. Finally, while the elimination of the diffusion barriers present at the studs in Cu damascene structures has been suggested in future designs, simulations results using MIT/EmSim demonstrate that these diffusions barriers have a very beneficial effect on Cu reliability through short line effects, and that their removal could have a detrimental effect on the overall reliability of Cu interconnects.

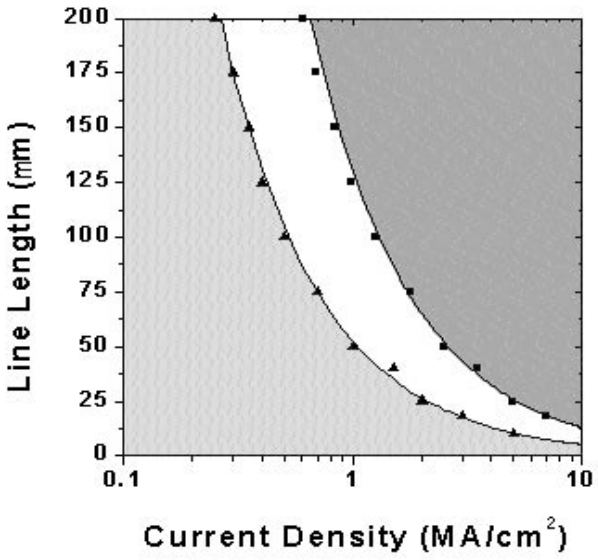

Fig. 3: Failure mechanism map for a Cu/Ta interconnect: From left to right, the map contains a region of immortality, region of void-nucleation-limited failures with n>1 scaling, and a void-growth-limited regime with n=1 scaling. No significant region of resistance saturation is present.

CAD for Microelectromechanical Systems (MEMCAD)

Personnel

M. Varghese (S. D. Senturia, in collaboration with the research group of J. K. White and with Coventor (formerly Microcosm Technologies))

Sponsorship

DARPA

The goal of this project has been to create a CAD system which is directed toward mechanical and electromechanical aspects of microsystem design. The MIT MEMCAD system has been licensed to Coventor, Inc. for commercial distribution. Continuing work at MIT has focused on new classes of problems that will enhance the breadth of device applications for MEMCAD.

Perhaps the most critical need in such systems is the ability to construct low-order dynamic macro-models of device behavior that can be used in system-level simulators (such as SPICE), while maintaining consistency with the true behavior as represented by meshed simulation. The TCAD portion of the MEMCAD system generates the device shape based on masks and process information, and the device simulators evaluate responses to applied loads in a highly meshed, numerically intensive environment. At the system level, however, where it is desirable to connect the MEMS device into circuits, and to understand the effects of feedback, accurate and energetically correct low-order dynamical behavior models are needed, either in the form of equivalent lumped circuit models, or as a small number of coupled Ordinary Differential Equations (ODE's).

Our group has worked extensively on the use of modal and basis-function methods for creating dynamic reduced-order models. We have now published several approaches to automatic generation of dynamic reduced order models, a modal method which works well when there is no stress-stiffening (a result of large deformations in clamped structures) and several approaches that deal with systems that are stress-stiffened. The most recent work on reduced-order models for stress-stiffened MEMS structures was presented at MSM 2000. This paper outlines a general procedure for capturing the non-linear effects of stress stiffening, while still using normal modes to represent the positional state of a structure. We have also made significant progress in automating the model generation process, particularly for multi-electrode electromechanical problems. This work has been submitted for presentation at Transducers 2001 (Münich, June, 2000).

Simulation Tools for Micromachined Device Design

Personnel
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(J. White)

Sponsorship
DARPA and SRC

Micromachining technology has enabled the fabrication of several novel microsensors and microactuators. Because of the specialized processing involved, the cost of prototyping even simple microsensors, microvalves, and microactuators is enormous. In order to reduce the number of prototype failures, designers of these devices need to make frequent use of simulation tools. To efficiently predict the performance of micro-electro-mechanical systems these simultion tools need to account for the interaction between electrical, mechanical, and fluidic forces. Simulating this coupled problem is made more difficult by the fact that most MEMS devices are innately three-dimensional and geometrically complicated. It is possible to simulate efficiently these devices using domain-specific solvers, provided the coupling between domains can be handled effectively. In this work we have developed several new approaches and tools for efficient computer aided design and analysis of MEMS.

One of our recent efforts in this area has been in developing algorithms for coupled-domain mixed regime simulation. We developed a matrix-implicit multi-level Newton methods for coupled domain simulation which has much more robust convergence properties than just iterating between domain-specific analysis programs, but still allows one to treat the domain analysis programs as black boxes. In addition, we developed another approach to accelerating coupled-domain simulation by allowing physical simplifications where appropriate. We refer to this as mixed regime simulation. For example, self-consistent coupled electromechanical simulation of MEMS devices face a bottleneck in the finite element based nonlinear elastostatic solver. Replacing a stiff structural element by a rigid body approximation which has only 6 variables, all variables associated with the internal and surface nodes of the element are eliminated which are now a function of the rigid body parameters. Using our coupled domain approach has made it possible to perform coupled electromechanical analysis of an entire comb drive accelerometer in less than 15 minutes.

Analysis of the resonance behavior of micromachined devices packaged in air or fluid requires that fluid damping be considered. Since the spatial scales are small and resonance analyses are typically done assuming a small amplitude excitation, fluid velocities can often be analyzed by ignoring convective and inertial terms and then using the steady Stokes equation. For higher frequency applications, the convective term may still be small, but the inertial term rises linearly with frequency. Therefore, analyzing higher frequency resonances requires the unsteady Stokes equations, though the small amplitudes involved make it possible to use frequency domain techniques. We have developed a fast Stokes solver, FastStokes, based on the precorrected-FFT accelerated boundary-elment techniques. The program can solve the steady Stokes equation or the frequency domain unsteady Stokes equation in extremely complicated geometries. For problems discretized using more than 50,000 unknowns, our accelerated solver is more than three orders of magnitude faster than direct methods.

Modeling of Copper Electroplating Pattern Dependencies

Personnel
T. Park and T. Tugbawa
(D. Boning)

Sponsorship
SEMATECH and Texas Instruments

Copper interconnect technology requires both electroplating to fill patterned trenches and vias, and chemical-mechanical polishing to remove excess copper from the field regions, leaving the copper only in the desired trench areas. The ability of the electroplating process to fill different sized structures and array regions generally shows pattern dependencies, as illustrated in Fig. 4. In particular, the amount of "array recess" (or "array bulge"), and the local feature step height appear to depend on pattern density, line width, and line spacing.

Using patterned wafer test wafer data, a new model for the resulting copper thicknesses has been developed, as a function of pattern factors. As shown in Fig. 5, the model is able to capture the effects seen in conventional copper fill. The step height is found to most strongly depend on line width, while the array recess also depends strongly on line space. A similar modeling approach can also be used in "superfill" electroplating processes where excess copper often results over patterned trench regions. The copper electroplating model is also being integrated with a copper CMP model, to enable the prediction of copper line thickness for different product layouts.

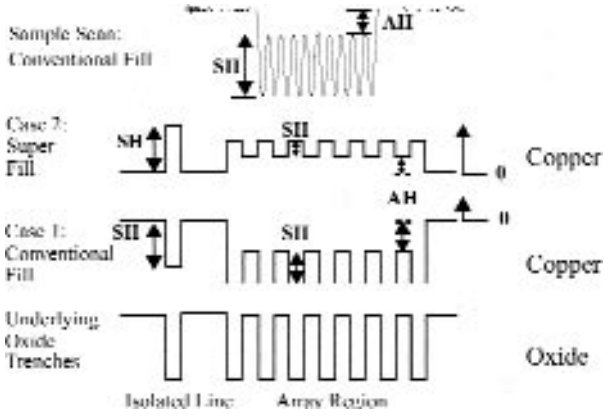

Fig. 4: Surface height variations (feature step height or SH, and array height or AH), resulting after copper electroplating, in both conventional and super fill cases.

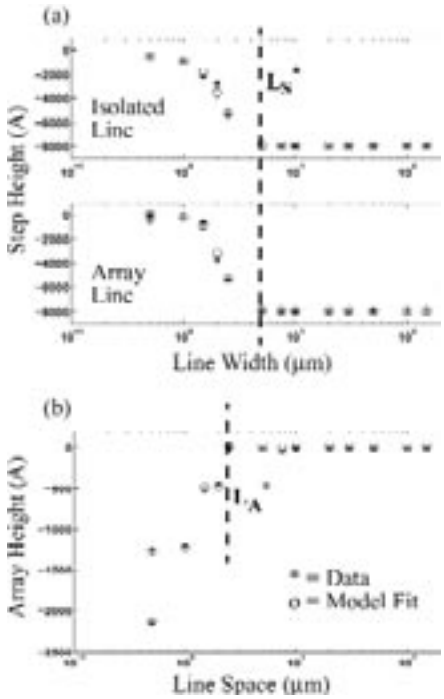

Fig. 5: Model fit compared to experimental data for the step height and array height as a function of pattern feature size, using a conventional electroplating process.

Modeling of Copper Chemical Mechanical Polishing

Personnel

T. Tugbawa and T. Park
(D. Boning)

Sponsorship

SEMATECH and Texas Instruments

The increased interest in copper CMP processes in IC manufacturing has raised the need for the development of predictive models for these processes. We have developed a modeling framework to predict the pattern dependencies observed in copper damascene processes. The model identifies three intrinsic stages in Cu CMP processes, and captures the dependencies in oxide and copper removal during these stages, including slurry selectivity, pattern density, line width, line space, and local step height dependence of removal rates.

A typical Cu CMP process is comprised of three intrinsic stages. Stage 1 deals with the removal of the overburden Cu. In this stage, we calculate the time it takes to reach the barrier material. The second intrinsic stage involves the removal of the barrier material. In this stage, we are interested in the time it takes to clear the barrier, as well as the Cu dishing that results when we have just cleared the barrier. Because of pattern differences within a die (pattern meaning pattern density, Cu line width, and oxide line space), we reach and clear the barrier at different times for different points on the die. Due to this, and due to nonuniform clearing across the wafer, we typically overpolish certain structures. We identify this overpolishing as the third intrinsic stage in a Cu CMP process, as illustrated in Figure 6. In this stage, we are interested in the amount of Cu dishing and oxide erosion. We define Cu dishing as the difference between the height of the oxide in the spaces and that of the Cu in the trenches, while oxide erosion is the difference between the oxide thickness before and after CMP.

In recent copper CMP processes, multiple steps are used where different slurry and pad may be used to modify the selectivity and minimize the dishing and

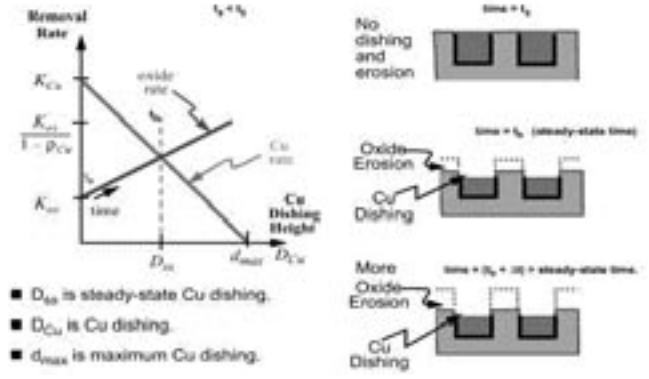

Fig. 6: The relative removal rates of oxide and copper during CMP, as a function of the dishing height.

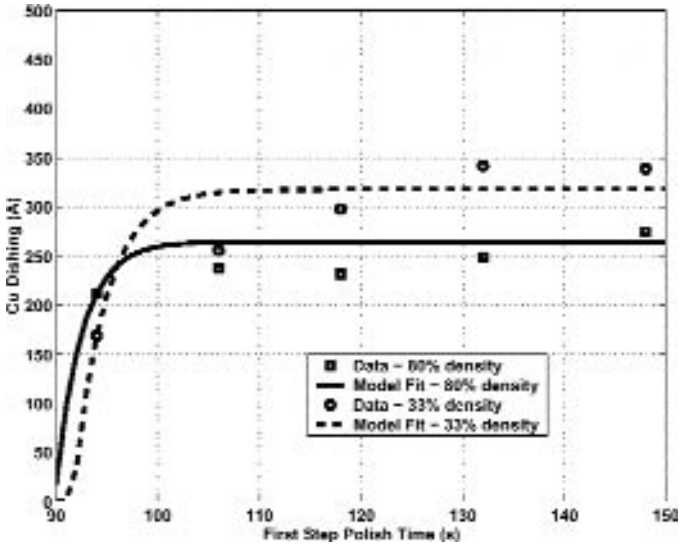

Fig. 7: Dishing versus polish time for step one (blanket copper rate is 135 Å/s and blanket dielectric rate is 1.5 Å/s in step one).

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erosion. We have developed model extensions to capture these effects. Shown in Figure 7 is the "creation" of dishing as a function of overpolish time, and Figure 8 shows the reduction of this dishing in a second CMP step where the oxide polishes more rapidly than does the copper. Current research is focusing on a model calibration methodology (particularly to ensure unique model parameter values), and extensions to handle multilevel and random layout polishing effects.

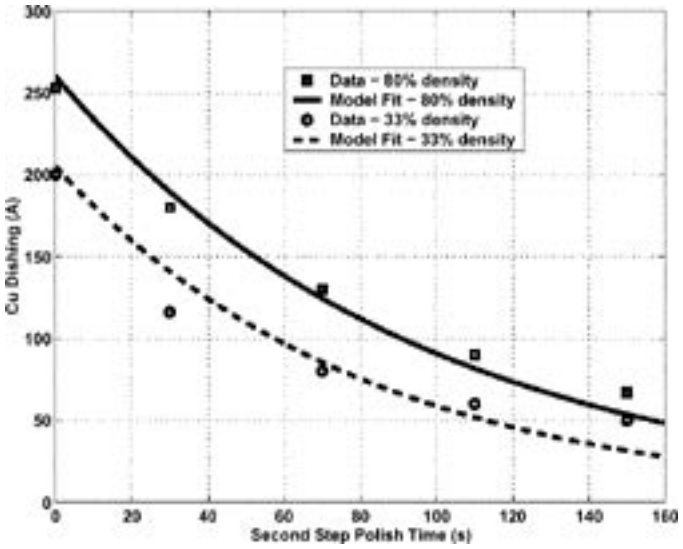

Fig. 8: Dishing versus second step polish time for two step CMP process (blanket copper and dielectric rates are 12 Å/s and 18 Å/s).

Variation in On-Chip Optical Clock Distribution

Personnel

S. L. Sam, M. Millis, and A. Lum
(D. Boning and A. Chandrakasan)

Sponsorship

MARCO Focused Research Center on Interconnect (SRC/DARPA) and NSF

On-chip optical clock distribution, as pictured in Figure 9, is being investigated as a future means to increase clock speed and reduce clock power. While extremely small skew in the arrival of an on-chip optical signal can be achieved, the conversion of the optical signal to a local electrical clock may be subject to substantial variation. In this work, we are studying the opportunities and challenges for on-chip clock and signal distribution.

A baseline receiver circuit, summarized in Figure 10, has been designed. Fabrication in a standard 0.35 μm CMOS process (using the MOSIS service) and die measurements indicated that the receiver circuit functioned as designed. Simulation studies were also performed to understand the sensitivity of the design to different sources of process and operating condition variations. For this simple baseline receiver design, we find that sensitivity to variation reintroduces substantial clock skew, as summaried in Table 1. Future optical on-chip clock design approaches must take such variation sources into account.

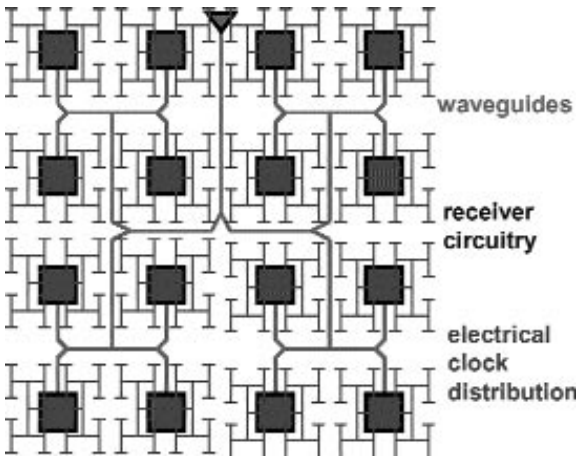

Fig. 9: On-chip optical clock distribution.

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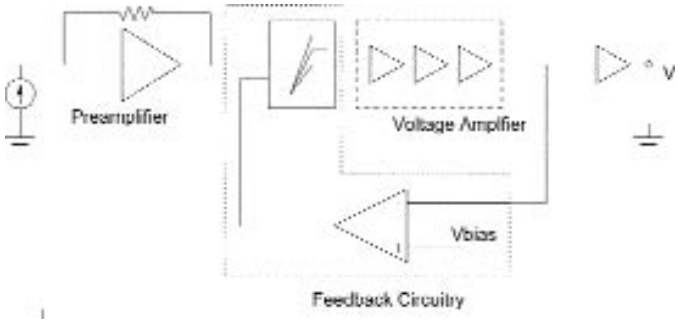

Fig. 10: Architecture of optical reciever circuit.

Parameter	Skew for 10% variation
Temperature	10ps
Power Supply	100ps
Threshold Voltage	20ps
Poly Length	80ps

Table 1. Clock skew in the optical receiver circuit due to 10% variations in selected parameters.

Investigating the Relationship Between Scaling and Mobility in Bulk and Fully-Depleted Single- and Double-Gate SOI MOSFETs

Personnel
A. Lochtefeld
(D. A. Antoniadis)

Sponsorship
DARPA

Discussions of the relative merits of Fully-Depleted Silicon-On-Insulator (FD)SOI vs. traditional bulk MOSFETs have typically emphasized scalability, extrinsic capacitances, and manufacturability. In this study we focus instead on the relationship between mobility and scaling for bulk MOSFETs and FDSOI alternatives, focusing on the 50 and 25 nm effective-channel length (L_{eff}) generations.

It has been projected that with aggressive channel dopant profile engineering, bulk MOS may scale down to ~25 nm L_{eff}. However this requires very heavy (~$1x10^{19}$ cm^{-3}) peak body doping to suppress short-channel effects, which results in a very high effective transverse electric field (E_{eff}) seen by electrons in the inversion layer. According to the well-verified universal mobility relationship, this can be expected to result in severely degraded low-field mobility for deeply scaled bulk MOS. In FDSOI devices, short channel effects are suppressed by limiting silicon and oxide film thicknesses. If alternative gate material processes can be developed such that gate workfunctions alone set an acceptable threshold voltage, body charge can be essentially zero, resulting in low E_{eff} and correspondingly superior mobility. Using 2D numerical simulations (Avant! Medici^{TM}) we have determined the uniform doping required for electrostatically sound bulk n-MOSFETs (at the L_{eff} = 50 and 25 nm generations), as well as the resulting E_{eff} seen by electrons in the inversion layer. In Figure 3 we show the corresponding range of mobility expected, based on the universal dependence of mobility on E_{eff}. Also shown are results for three FDSOI (and one additional bulk) MOSFET architectures. These results suggest that Single-Gate (SG)SOI is an attractive alternative to bulk at 50 nm L_{eff} (with greater than a 1.5X mobility advantage), beyond which it may not feasibly scale. Furthermore, at the 25 nm generation, Double-Gate (DG)SOI should have a 3-

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4X mobility advantage over aggressively designed bulk NMOS. Although modern devices operate in or near the velocity saturation regime, models that account for non-local transport effects predict significant drive-current benefits for superior low-field mobility.

L_{eff} (nm)	50	25
Tox_{eq} (nm)	1.9	1.2
Bulk Uniform Channel Doping	$9.4x10^{18}$ cm^{-3}	$2.4x10^{18}$ cm^{-3}

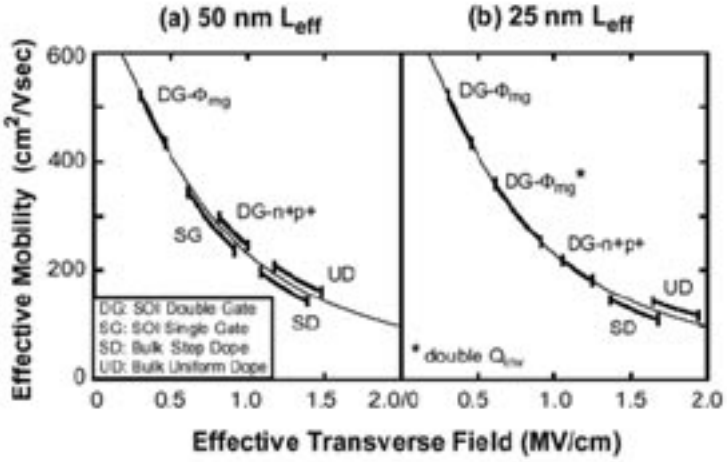

Fig. 12: Universal effective MOSFET mobility curves from [2], with regions of operation delineated for five different bulk and SOI device architectures. Figure 12a corresponds to the 50 nm L_{eff} generation, and Figure 12b to the 25 nm generation. "DG-Φ_{mg}" refers to double-gate SOI with midgap gate workfunctions. "DG-n+p+" refers to double-gate SOI with asymmetrical n+ / p+ poly gates. For each device architecture the range of E_{eff} is determined from 2D simulation, and corresponds to a range of inversion layer densities (Q_{inv}) from $0.8x10^{13}$ to $1.2x10^{13}$ cm^{-3}. In the case of DG-Φ_{mg} Q_{inv} is the sum of inversion charge in both inversion layers, except for special case noted in Figure 3b. DG-n+p+ has poorer mobility than DG-Φ_{mg} because of the large built-in transverse field due to the workfunction difference between top and bottom gates.

Gettering Design Diagram

Personnel

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A Time-Temperature-Transformation (TTT) diagram format has been developed for gettering to provide a comprehensive description of the wafer and for process design parameters for effective transition metal removal. The materials variables are p-type doping level, density of bulk Internal Gettering (IG) sites and backside IG site density. The process variables are time and temperature. The TTT diagram enables understanding of the interaction of the various gettering mechanisms with processing temperature. TTT diagrams convey process intuition in that they display a convolution of the thermodynamic driving forces for gettering with the system's kinetic ability to respond to those driving forces. TTT diagrams for Fe and Cu are presented, which demonstrate that uniformly doped wafers with Back Durface Damage (BSD) are able to remove near surface Fe and Cu more efficiently than those without.

The TTT diagram (Figure 13) is constructed from the family of isothermal heat treatment curves. The curve that joins the saturation points for each temperature is the curve that gives time to reach equilibrium as a function of temperature. After crossing the equilibration curve in time for a given temperature, there is no change in [Fe] as the solubility limit has been reached and there is no longer any driving force to remove Fe from the solid solution. In addition to the equilibration curve, isoconcentration curves are included. The isoconcentration curve gives the time to reach a specified final Fe concentration as a function of temperature. This curve can be used to estimate if the wafer/process system will meet Roadmap specifications.

In Figure 14 we present a comparison of two TTT diagrams, one for the case of no back surface treatment and one with an appreciable density of nucleation sites at the back surface. In the temperature range of 700-1000C, there is not much difference between the curves. For temperatures below 700C, the impact of BSD in reducing time to reach a particular residual Fe concentration becomes increasingly marked as temperature decreases. At higher temperatures, the gradient due to different equilibration rates in the bulk and back surface region is rapidly eroded because of the relatively high diffusivity. At lower temperatures, the greater degree of supersaturation partially compensates the reduction in diffusivity. However, the reduction in D at lower temperature will allow the BSD to generate a gradient that will significantly enhance mass transport from the front of the wafer relative to the no BSD case.

Figure 15 shows a comparison of the TTT diagram for wafers with and without segregation gettering. Both wafers have IG site density of $10^9/\mathrm{cm}^3$ and DZ width of 20μm. The epitaxial wafer has an epilayer thickness of 5μm and substrate doping of $10^{19}/\mathrm{cm}^3$. The diagram shows the time reduction for the various iso-concentration levels is significantly reduced at lower processing temperatures.

Figure 16 shows the TTT diagram for Cu in an intrinsic wafer with IG sites. IG site density is $10^9/\mathrm{cm}^3$ and DZ width is 20μm. Compared with Fe, Cu has high diffusivity and solubility even at low temperature. This makes the TTT diagram toward lower temperature, as shown in Figs. 3 (broken lines) and 4. This diagram quantitatively provides the fastest cooling curve of Cu internal gettering. The TTT diagram is even more essential for the case of p-type doping. Due to Cu-acceptor pairing, the time and temperature trade-offs become more complicated as low temperature solubility is effectively pinned at the doping concentration. We are currently in the process of calculating the TTT diagrams for Cu in a range of p-type doping levels.

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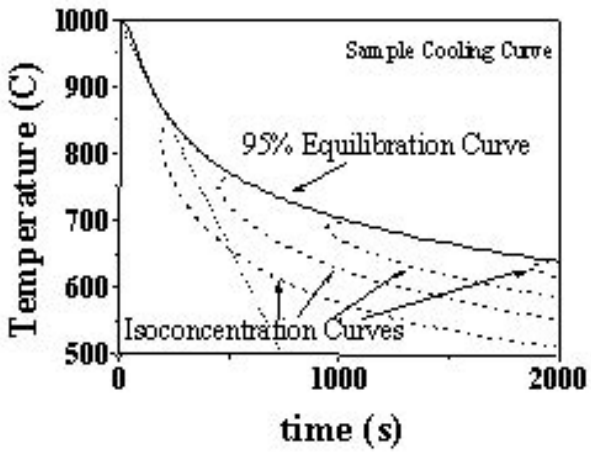

Fig. 13.

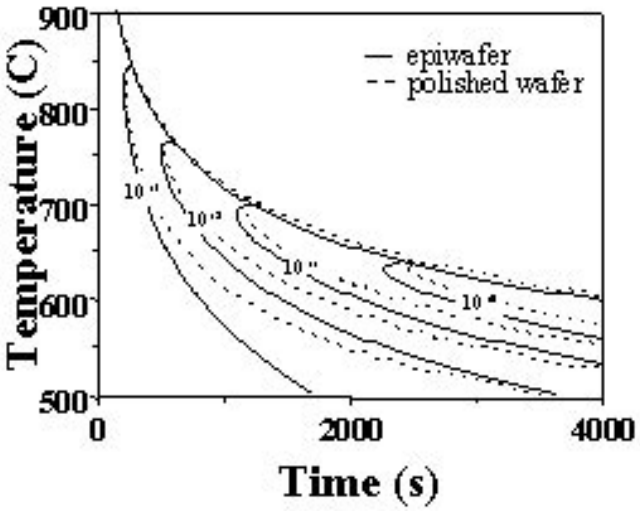

Fig. 14.

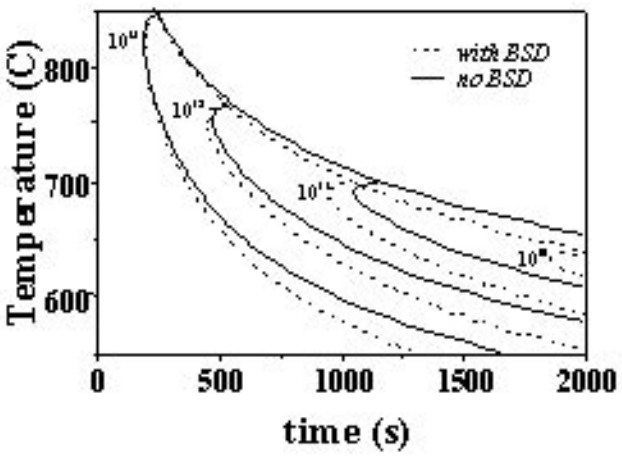

Fig. 15.

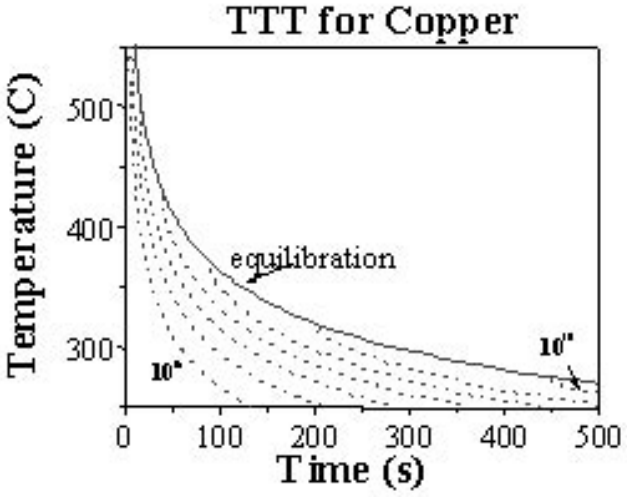

Fig. 16.

Electric Field Simulations for Field Emission Devices

Personnel

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(S. D. Senturia in collaboration with A. I. Akinwande)

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The goal of this project is to develop a CAD tool for prediction of electron emission from field emitter tips, their trajectory to the phosphor screen and the resulting spot size on the screen for an array of field emitters. The basic structure studied is shown in Figure 17. It consists of a a field emitter cone with a tip radius of 10 nm, a 0.2 μm thick gate with 1 μm aperture, a 0.5 μm thick focusing electrode located 0.5 μm above the gate. The anode is about 1 mm above the field emitter.

The project raises two key challenges: the very different dimensional scales surrounding the emitter tip (10 nm), the gate (1 μm) and the anode (1 mm) and the the need to adapt boundary element based solvers for (Dirichlet and Neumann) mixed boundary conditions. The potential gradient is calculated on surfaces with Dirichlet conditions and potential on surfaces with Neuman conditions using a Green's Theorem kernel. A source formula is used to calculate an equivqlent pseudo-charge distribution on all surfaces from which electric field is determined at any point of interest is determined.

Using this approach, the electric field at the tip surface is determined and the field emission current density is calculated using the Fowler-Nordheim equation. The electron trajectories are obtained by integrating the Lorentz equation from various points on the emission tip to the anode. The spot size and current distribution on the phosphor screen for an array of field emitters can be calculated using superposition using the trajectories weighted by the emission surface areas and the current densities.

Figure 18 shows a typical tip structure that was fabricated and characterized. Figure 19 shows a comparison of the experimental simulated current per tip as function of the gate voltage for a 60x60 Si tip FEA. The only adjustable parameter is the radius of curvature. The radius of curvature that matched the simulation is 8.4 nm while the experimentally measured radius is about 10 nm. Figure 20 shows a comparison between the spot size measured for a phosphor screen which is biased at 5000 V and is 1 cm away from the FEA. The experimental spot size is about 2 mm while the simulated spot size is 1.8 mm.

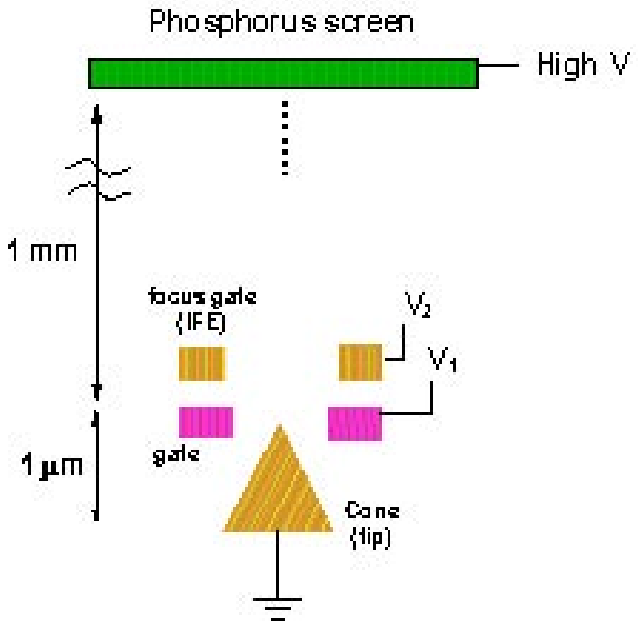

Fig. 17: The Integrated Focus Electrode Field Emitter Display structure.

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In the last year we explored the device parameter space for the design and operation of the field emission device with integrated focus using a design of experiment strategy. One major result of this study is that the optimal focus voltage is about 1/3 of the gate voltage. We also automated the device design and analysis of field emission devices using DOE.

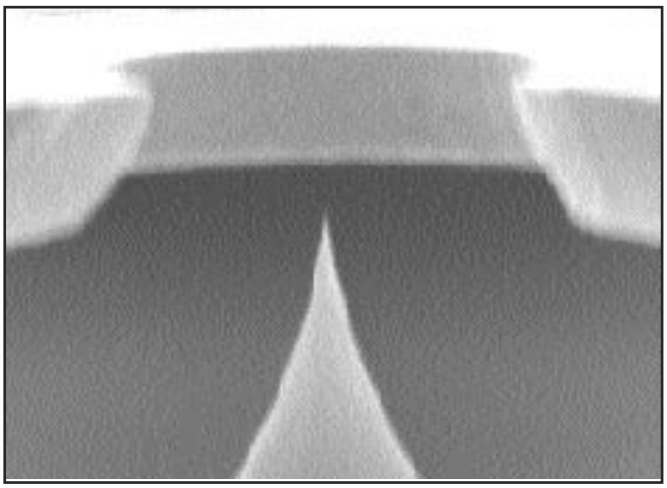

Fig. 18: SEM of the Si Field Emitter tip.

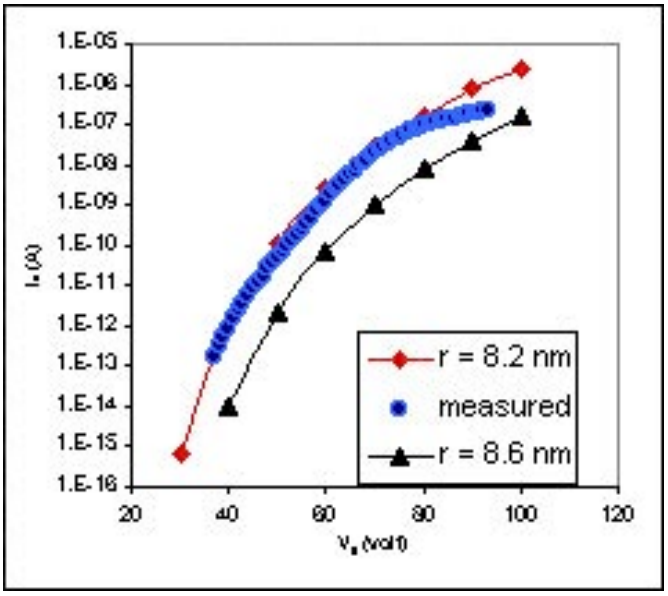

Fig. 19: Comparison between the experimental and simulated current density for a Si field emitter array. The only adjustable parameter was the tip radius.

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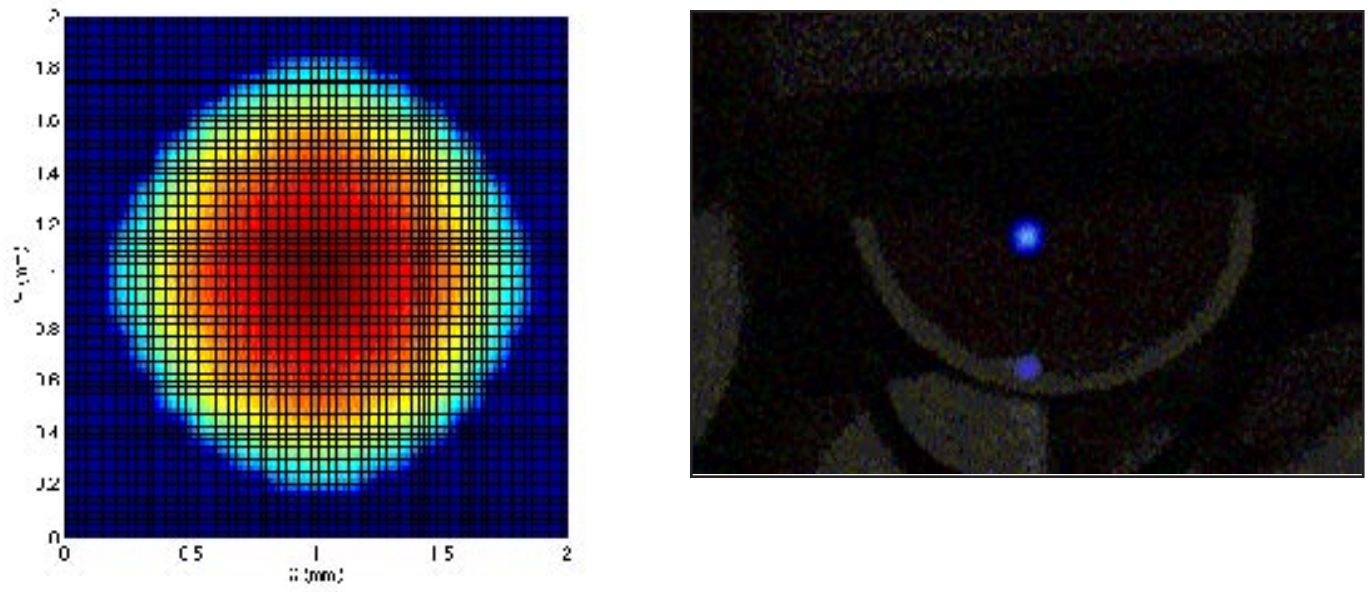

Fig. 20: Experimental and simulated spot size on phosphor screen for a 60x60 4μm-pitch FEA with the phosphor screen biased at 5000 V at a distance of 1 cm from the FEA.