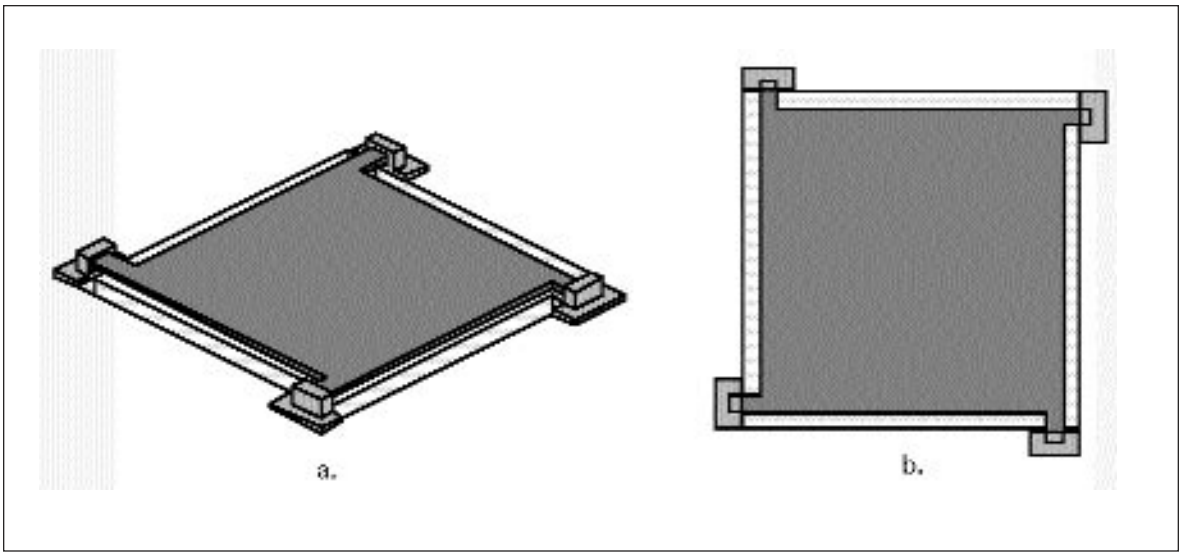
Materials



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Materials

- ***SiGeOI Fabricated Via Wafer-Bonding and Etch-back or Smart-cut***
- ***III-V/GeSi/Si Heterointegration***
- ***Ge/$Si_{1-x}Ge_x$ Quantum Well Infrared Photodetector***
- ***Ge Photodetectors for Si Microphotonic Circuits***
- ***Inelastic Deformation Polycrystalline Thin Films and Lines***
- ***Tensile Stress Generation During Growth of Volmer-Weber Thin Films***
- ***Ferroelectrics for High Strain Actuation***
- ***Microelectromechanical Test Structures (M-Test)***
- ***Use of polyoxymethylene as a Sacrificial Layer for Air Bridge Fabrication***
- ***Cluster Ion Beam Processing***
- ***Solventless Lithography***
- ***Laser-driven Liquid Phase Epitaxy***
- ***Molecular Beam Epitaxy of InP-based Heterostructures on Silicon Substrates and Membranes***
- ***Passivation of Copper Surfaces with Organic Monolayers***
- ***Semiconducting Gas Sensors***
- ***Resonant Gas Sensors***

Continued

SiGeOI Fabricated via Wafer-Bonding and Etch-back or Smart-cut

Personnel

G. Taraschi and Z-Y. Cheng (E. A. Fitzgerald, D. A. Antoniadis and J. L. Hoyt)

Sponsorship

Singapore-MIT Alliance program, and DARPA HGI

It is of great interest to combine the advantages of silicon-on-insulator (SOI) technology and high performance SiGe technologies. $Si_{1-x}Ge_x$-based heterostructure devices, such as field-effect-transistors (FET) and bipolar devices, with advantageous dc and rf performance, have been shown using modulation of electronic properties by strain engineering and heterojunction energy barriers. In addition to these benefits, it is also of interest to develop $Si_{1-x}Ge_x$ devices in a SOI configuration for Si-CMOS compatible processes. The advantages associated with an insulating substrate, namely reduced parasitic capacitances, improved isolation, reduced short-channel-effect, etc, can thus be combined with the improvements offered by $Si_{1-x}Ge_x$ devices. A general substrate for such devices is relaxed $Si_{1-x}Ge_x$-on-insulator (SiGeOI). On the top of such a versatile SiGeOI substrate, one or multiple device layers may be grown subsequently, such as strained Si, strained Ge, strained $Si_{1-y}Ge_y$ (with either x>y or x<y), InGaP, or GaAs layers (with x=1), for either electronic or optoelectronic applications.

Our research has focused on the fabrication of relaxed SiGeOI substrate via two different approaches, both of which incorporate wafer-bonding of SiGe (grown via UHV-CVD) to oxidized handle wafers. The first approach uses etch-back to remove the backside of the handle wafer, whereas the other method employs hydrogen-ion-implant-induced delamination. A low density of threads in the 10^5 cm^{-2} range (for 25% Ge) was confirmed via EPD (etch pit density) for both the as-grown and bonded SiGe, which proves that there is no substantial increase in threading dislocations due to the proposed process. This is in contrast to SIMOX, which can possibly introduce many additional defects depending on the material system being implanted.

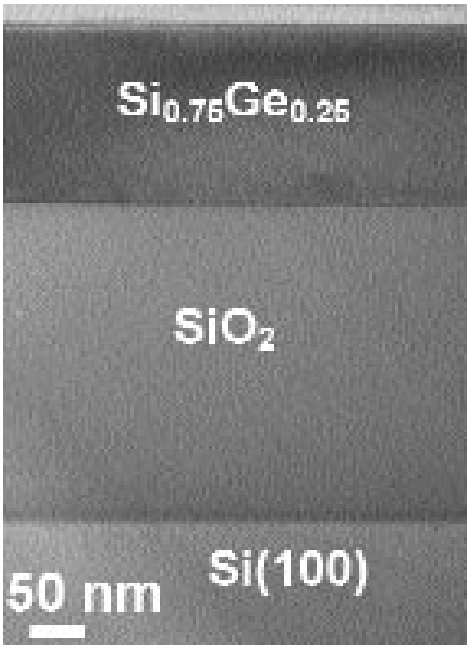

Fig. 1: Cross-sectional TEM of the SiGe on oxide structure fabricated using wafer bonding and tech-back.

III-V/GeSi/Si Heterointegration

Personnel

M.Groenert, V.Yang, N.Quitoriano, C.Leitz, and A.Pitera (E.A. Fitzgerald)

Sponsorship

NSF/MRSEC, ARO and MARCO Focused Research Center on Interconnect

The promises inherent in merging conventional silicon-based IC technology with the direct-gap optoelectronic capabilities of III-V semiconductor technology have inspired many different strategies for growing GaAs-based devices on silicon substrates. Minority carrier devices such as laser diodes are the most sensitive to defects resulting from the mismatched GaAs/Si heterojunction. Continuing work in this research group with relaxed graded buffer layers of Ge_xSi_{1-x} grown on silicon wafers have created device-quality substrates upon which GaAs-based light-emitting and laser diode structures can be grown and evaluated.

The mismatch in the thermal expansion coefficients of GaAs, Ge and Si can introduce additional strains into GaAs structures grown on graded Ge_xSi_{1-x} substrates. The introduction of compressive strain at the high temperatures needed for III-V film growth can have the effect of reducing the effective critical thickness for plastic relaxation in these GaAs films grown on Ge_xSi_{1-x} and must be accounted for when designing devices for integration. Deliberate compressive buffer layers have been investigated to force material relaxation below sensitive devices. Tensile strain developed during film cool-down can lead to microcrack formation in thin GaAs overlayers on Ge_xSi_{1-x}, and this phenomenon is currently being investigated to better define the optimum processing windows for GaAs on Ge_xSi_{1-x} integration.

$Al_xGa_{1-x}As$ visible light emitting diodes have been grown on graded Ge_xSi_{1-x} substrates with organometallic chemical vapor deposition (OMCVD), and these devices have been characterized and compared with identical structures grown on standard GaAs substrates. $In_xGa_{1-x}As$/GaAs strained quantum well diodes have also been grown and characterized on these substrates. $InxGa_{1-x}As$/GaAs quantum well laser diodes have been shown previously to be exceptionally resistant to dislocation-induced failures under a wide range of operating conditions. Work is continuing on the design and fabrication of $In_xGa_{1-x}As$/GaAs quantum well lasers on Ge_xSi_{1-x}, along with simple $In_xGa_{1-x}As$/GaAs/$Al_xGa_{1-x}As$ integrated optical links consisting of an LED-based emitter, an etched ridge waveguide, and a photodetector grown together on a Ge_xSi_{1-x}/Si substrate.

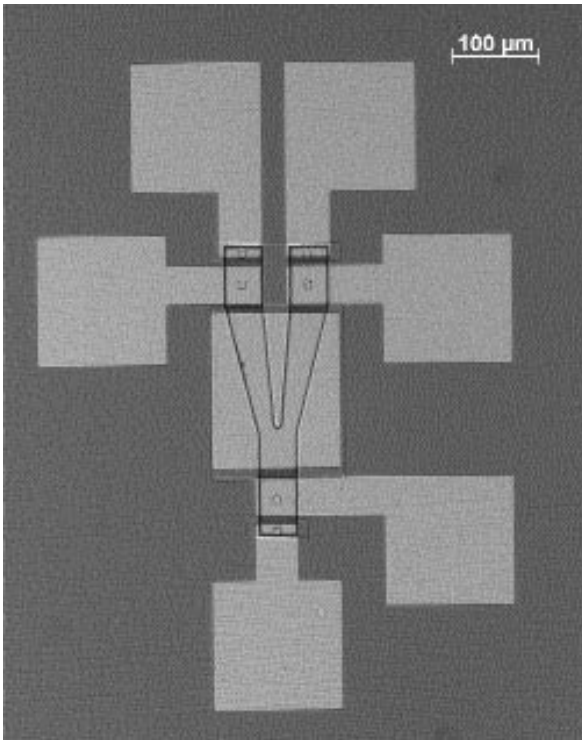

Fig. 2: Optical micrograph of a prototype Y-bend optical link structure fabricated on GaAs on Ge_xSi_{1-x}/Si.

Ge/Si1-xGex Quantum Well Infrared Photodetector

Personnel
M. L. Lee (E.A. Fitzgerald)

Sponsorship
Hanscom Airforce Base

Current state of the art long and mid-IR photodetectors utilize costly and difficult to process HgCdTe alloys. Germanium quantum wells grown epitaxially on $Si_{1-x}Ge_x$ can also be used for the absorption of mid to long infrared radiation (2-5μm) due to the large valence band offset between Ge and $Si_{1-x}Ge_x$. Compressive strain splits the valence band degeneracy of Ge, forming numerous discrete energy levels in the Ge quantum well which can be used to detect incident photons via intersubband transitions. Additionally, these discrete energy states can be engineered by varying the width and degree of strain in the quantum well, allowing much greater flexibility than possible with band-to-band processes. Richard Soref (Hanscom Airforce Base) has taken advantage of the $Si_{1-x}Ge_x$ optimized relaxed graded buffer of Fitzgerald et al to design a novel multiple quantum well infrared photodetector (QWIP) with 50Å germanium quantum wells and 400Å $Si_{0.45}Ge_{0.55}$ barriers on a $Si_{0.4}Ge_{0.6}$ virtual substrate (see Figure 3). For this QWIP, the compressive strain of the Ge quantum well is balanced by tensile strain in the barrier layers, and a theoretically limitless number of quantum well periods can be epitaxially grown without misfit dislocation nucleation and subsequent strain relaxation. The detectivity (D*) of a QWIP is directly proportional to the number of periods, giving the Ge/$Si_{1-x}Ge_x$ QWIP significant advantages over current-art silicon based QWIPs where compressive strain cannot be compensated.

With sufficient thermal energy, compressively strained layers tend to relax by undulation during epitaxial growth. Figure 3 shows a QWIP structure that was grown in Fitzgerald's UHVCVD at 450ºC with undulated germanium quantum wells. It is anticipated that lower temperature epitaxial growth will lead to fully planar strained layers.

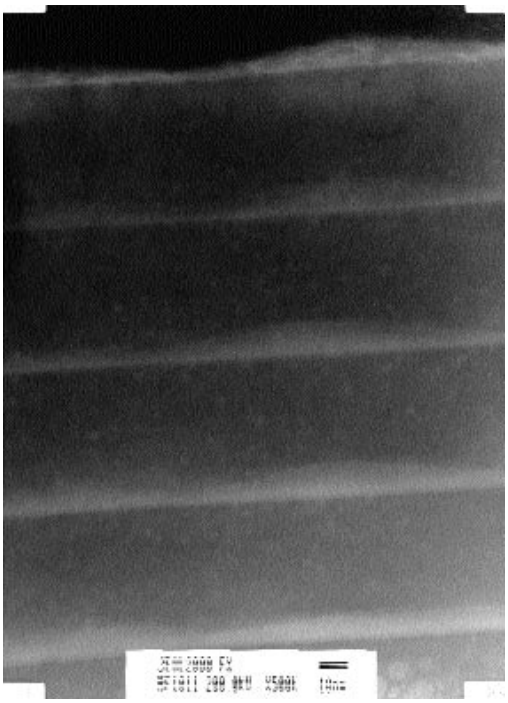

Fig. 3: Five-period QWIP. Bright layers are Ge quantum wells and dark layers are $Si_{0.45}Ge_{0.55}$.

Ge Photodetectors for Si Microphotonic Circuits

Personnel

H.-C. Luan, D. Lim, K. Lee, A. M. Agarwal, K. Wada, J. Michel, and (L. C. Kimerling)

Sponsorship

SRC and MARCO Focused Research Center on Interconnect

We are studying the UHV-CVD growth of high quality Ge on Si for the integration of Ge photodetectors with polySi waveguides and Si CMOS devices. Ge provides high absorption coefficient at 1.54 μm and is an ideal material for photodetection at optical communication wavelength. High quality Ge with low threading dislocation density can be grown directly on Si by a two-step growth technique followed by an annealing treatment. The electrical properties and optical properties of Ge films grown on Si are being characterized.
Based on our measurements, the effect of threading dislocations on the GHz operation of Ge photodetectors will be studied.

We are designing a process for the integration of Ge photodetectors with polySi waveguides and Si CMOS devices. This process technology makes use of our ability to grow Ge selectively on patterned Si wafers. SiO_2 is used to protect Ge materials from traditional Si CMOS process chemistries such as the RCA and Piranha cleans. The goal of this project is the demonstration of a functional Si microphotonics circuit.

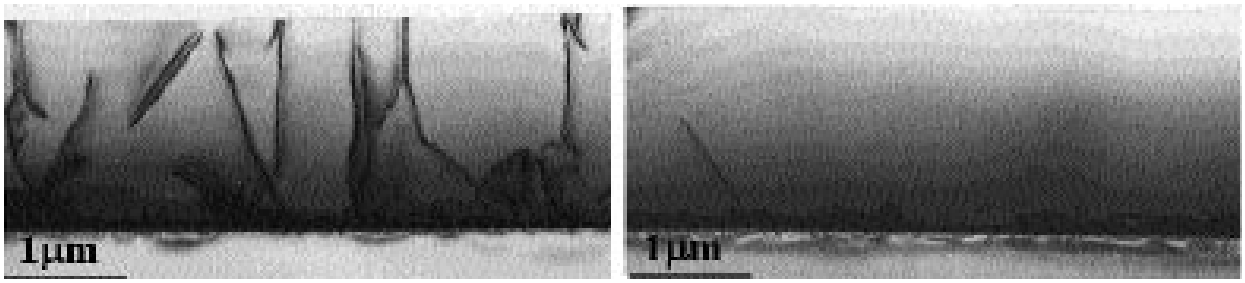

Fig. 4: (Left) Cross sectional TEM micrograph of 1mm of Ge grown on Si by UHV-CVD. (Right) Cross sectional TEM micrograph of 1 μm of Ge on Si after annealing.

Fig. 5: Cross sectional TEM micrograph of 1μm of Ge selectively grown on Si.

Inelastic Deformation of Polycrystalline Thin Films and Lines

Personnel
M. Kobrinsky, S. Seel, M. Gross (C.V. Thompson)

Sponsorship
NSF

Strain energy resulting from deformation is an important driving force for microstructural evolution in polycrystalline thin films and lines. However, the current knowledge of the deformation mechanisms is insufficient to accurately calculate the strain energy and its dependence on film thickness, grain size and orientation. We are performing experiments to characterize stress and structure evolution during film formation and during post-deposition annealing. The experimental studies are being carried out in films on wafers, in films on MEMS devices, and in films on micromachined membranes. The latter allows in-situ transmission electron microscope observations of dislocation motion. These experiments are used as the basis for development of modeling and simulation capabilities for engineering optimization of film stresses and structures.

In the past years we have shown that two different inelastic regimes exist in uncapped Ag and Cu films, as well as in Damascene Cu lines (see Figures 6 and 7): diffusional creep at high temperatures and dislocation plasticity at low temperatures. These results are expected to be representative of fcc metallic thin films, lines, and other small-volume structures. For the diffusional creep mechanism, we obtained an activation energy of 0.6 eV for the case of Ag. In addition, it was found that this inelastic mechanism can be suppressed using a capping layer. Diffusional creep occurs through diffusion over distances of the order of the grain size. Because the grain size often scales with the film thickness, diffusional creep can lead to a decrease in the flow stress with decreasing film thickness. This contrasts with the increasing flow stress with decreasing film thickness often observed in passivated films.

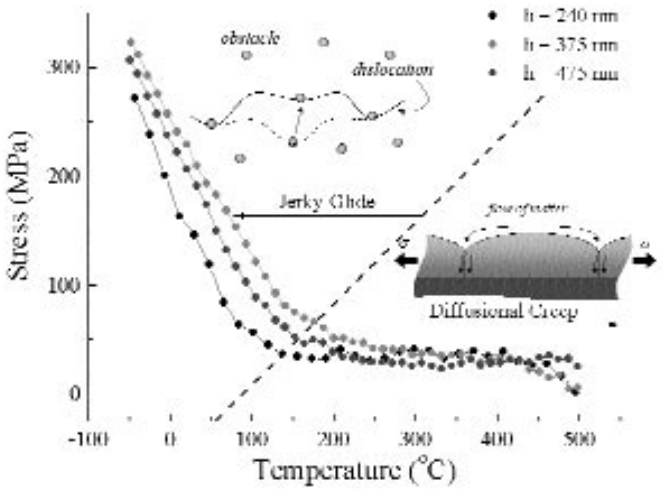

Fig. 6: Stress as a function of temperature in uncapped silver thin films. The inelastic regimes are shown.

Continued

At low temperatures, in-situ TEM and stress-relaxation experiments were used to study the mechanisms for inelastic deformations in uncapped Ag thin films. The values obtained for the activation volume and the presence of a jerky glide of dislocations (see figure 6) indicate that the dominant inelastic mechanism is the thermally-activated glide of dislocations through forest dislocation obstacles (pinning points). The mean distance between obstacles is the characteristic length scale that dictates the low-temperature strength of the films. It was found that this characteristic length scale is significantly smaller than the film thickness and the average grain size, which explains the origin of the superior strength of polycrystalline thin films.

In addition, the effects that grain size and film thickness have on the characteristic length scale of the dislocation-mediated inelastic mechanism are being explored to identify the origin of the thickness dependence of the strength of thin films.

Our experimental results, including direct observation of dislocation motion during thermal cycling, suggest that dislocation-mediated plasticity in metallic thin films occur in ways that differ substantially from those assumed in current energy-based models.

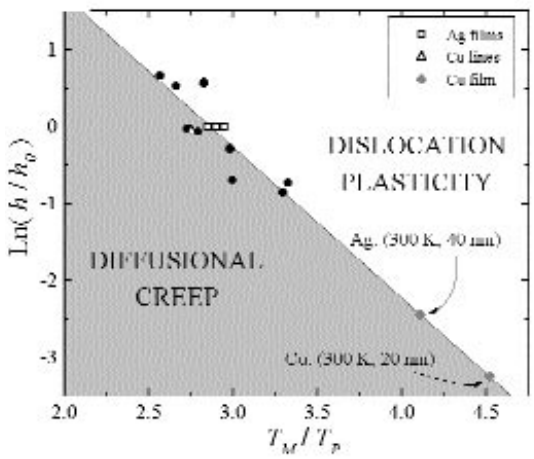

Fig. 7: Deformation map for thin metallic films on substrates subjected to thermal cycling. The boundary line between the diffusional creep and the dislocation-mediated plasticity regions was calculated for a strain rate of 1.7 X 10^{-6} s^{-1}. The use of different strain rates only produce a vertical shift of the boundary between inelastic regimes. The data shown in the figure corresponds to silver and copper films, as well as damascene copper lines. The diamond points were obtained by extrapolating the experimental data to room temperature and are consistent with observations of stress evolution during room temperature film formation. The normalization constant h_0 was taken as 0.5 μm. T_M is the melting temperature of silver or copper.

Tensile Stress Generation During Growth of Volmer-Weber Thin Films

Personnel
S. Seel, C. Friesen, A. Takahashi, and (C.V. Thompson)

Sponsorship
NSF

When thin films are deposited by thermal evaporation or sputtering, the initial stages of film growth occur by nucleation of isolated islands, which grow and eventually coalesce to form a continuous film. Experimental observations by our group and other researchers have correlated the process of island coalescence, viewed by transmission electron microscopy, with a significant tensile stress generation measured by monitoring the wafer substrate curvature during deposition. We are taking a multi-disciplinary approach to expose the physical origins of the tensile stress generation in order to quantitatively predict the magnitude of the resulting stresses. Our current research involves novel experimental techniques using patterned substrates to control island size and spacing, finite element methods to calculate stress generation due to island interaction, and molecular dynamics simulations of island coalescence.

Tensile stress generation during film formation is typically associated with island coalescence. If neighboring islands are within close proximity, they will stretch towards each other and zip up to form a grain boundary to reduce the interfacial energy at the expense of an associated strain energy. The magnitude of the stress depends strongly on the island size at impingement. Lithographic techniques will allow us to artificially control the placement and radii of the growing islands to further study their behavior.

During conventional film growth, islands of varying size coalesce. By modifying the substrate we can create a series of islands with monodispersed radii that will allow us to quantitatively measure the dependence of the stress at different stages of coalescence. In addition we can make sets of islands with different radii to study the effects on the stress evolution. These results will help us to better understand the zipping event, as well as provide us with data for the validation of our modeling efforts.

Island coalescence generates highly non-uniform stresses, leading to difficulties in analytically expressing the stress in the island. Consequently, we utilized finite element methods to calculate the strain energy and average stress resulting from island coalescence. Our more accurate FEM modeling yields average stresses more consistent with experimental observations of tensile stress generation during thin films deposition, as shown in Figure 8.

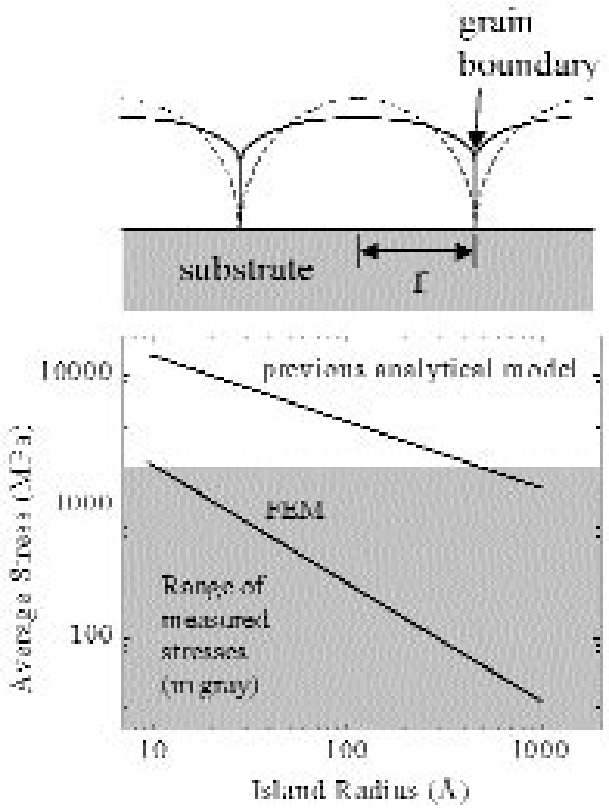

Fig. 8: Comparison of FEM calculations of island coalescence stress with results from previous analytical approximations. The gray region represents typical tensile stresses measured by monitoring wafer curvature during thin film deposition.

Continued

In order to investigate the coalescence process, we are in the process of performing molecular dynamics simulations. A direct experimental study of island coalescence is difficult due to the small length and time scales of the phenomena. As a guide for further experimental work, computer simulations generate a predictive model for island behavior. Since the position and velocity of each atom is tracked during the simulations, the possible atomistic mechanisms for island coalescence can be studied. A better understanding of the atomic processes that occur during island zipping should produce a better analytical model for the stress development during coalescence.

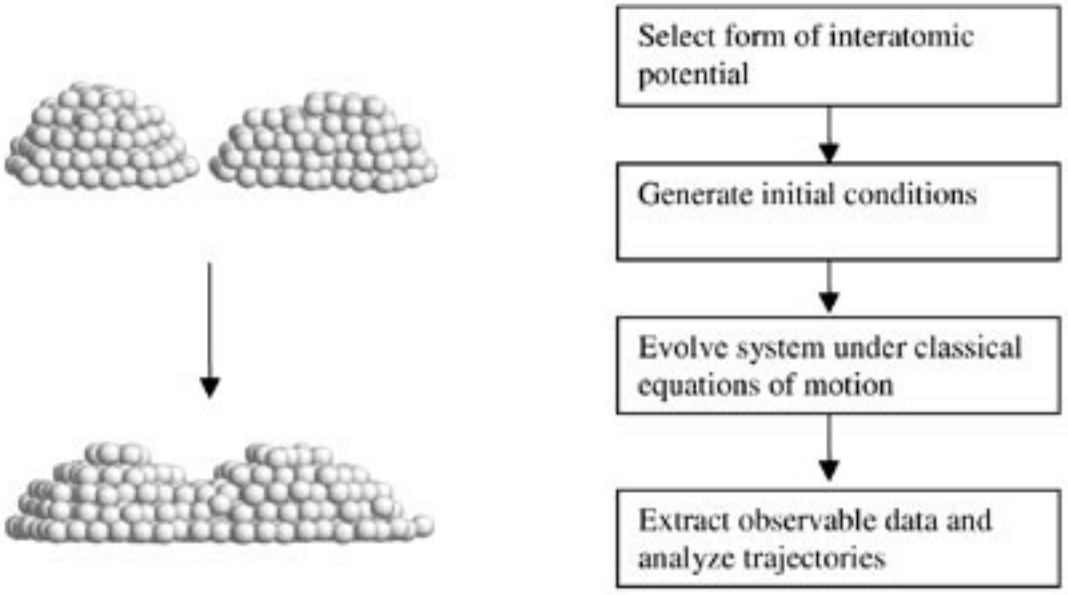

Fig. 9: General framework for molecular dynamics simulation. The subfigure on the left shows the initial and final state of an evolved Lennard-Jones system. The subfigure on the right presents a general flowchart for molecular dynamics simulations.

Ferroelectrics for High Strain Actuation

Personnel
Y. Avrahami (H. L. Tuller)

Sponsorship
ARO and MIT Microphotonics Center

Perovskite and related oxide systems are being explored as potential candidates for high strain actuators with good thermal stability and low hysteresis. Field-induced antiferroelectric-ferroelectric transitions show high strain levels in polycrystalline materials. Compositions have been identified which show a morphotropic phase boundary and consequently temperature insenstive strain-field characteristics. Efforts are currently focused on the preparation and characterization of non-lead based polycrystalline and single crystalline high strain ferroelectrics and their integration into MEMS and microphotonic devices.

Microelectromechanical Test Structures (M-Test)

Personnel
E. Deutsch and R. Sood (S. D. Senturia in collaboration with the research group of C. Thompson)

Sponsorship
SRC and DARPA

The goal of this project is the development of a micromechanical "drop-in" pattern, analogous to the set of test structures used in microelectronics for measuring transistor parameters, which can be used to monitor MEMS process uniformity and repeatability, and to determine the mechanical properties of micromechanical materials. The method used is called "M-Test", in which the dependence of electrostatic pull-in voltage on device geometry is used as the primary measurement.

This technique is accurate for ideal test structures, which have been fabricated in a wafer-bonded SOI process. The extracted modulus for these ideal single-crystal-silicon structures agreed with literature to better than 3%. In surface micromachined structures, support compliance, especially in combination with residual stress, as well as topography and other factors degrade accuracy of this technique.

For beams with compressive stress and compliant supports, a bistable buckling type of displacement is observed as shown in Figure 10. Experimentally, beams with both the "positive" bending and "negative" bend-

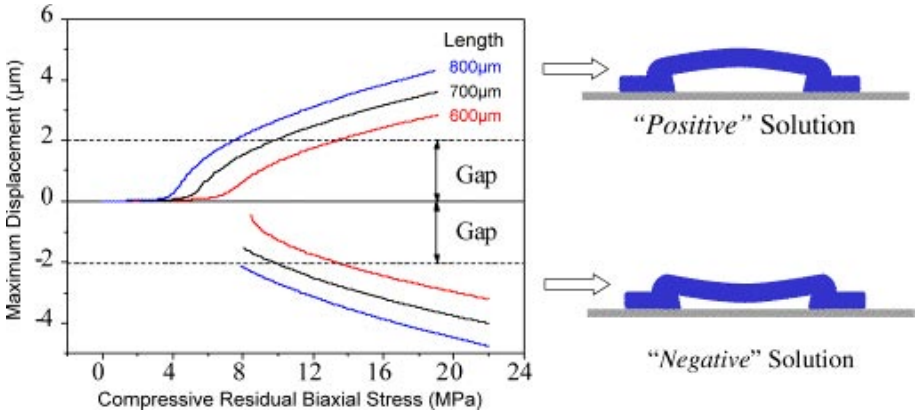

Fig. 10

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ing have been observed on the same die, demonstrating this bistability directly. If the support compliance is known from accurate FEM modeling, the buckling type of displacement of the beams can be used to measure the residual axial stress. For beams with tensile stress, support compliance causes a small pre-bending of unactuated beams. Furthermore, the pull-in voltage of the beams is greatly reduced because the compliant supports deform during the actuation. Efforts are currently focused on fabricating surface micromachined supports that have very small compliance in order to eliminate these effects.

In collaboration with Prof. Thompson's group, we have continued our work on M-Test structures that will permit the device to be operated inside a thin-film deposition system. This means that in-situ measurements of changes in total stress and stiffness can be determined, permitting study of the development of stress in very thin films deposited onto substrates.

Use of Polyoxymethylene as a Sacrificial Layer for Air Bridge Fabrication

Personnel

L. S. Loo (K. K. Gleason)

Sponsorship

MARCO Focused Research Center on Interconnect (SRC/DARPA)

As feature sizes in integrated circuits (IC) are diminishing in scale (0.13 microns and below), there is an increasing need to incorporate lower dielectric constant (k) materials in order to offset the corresponding increase in interconnect delay. New materials such as fluorocarbons and various spin-on-glasses have replaced conventional silicon dioxide as dielectric material thereby reducing the dielectric constant by a factor of about two. However, this improvement is still inadequate in view of anticipated reduction in feature sizes beyond 0.10 microns, whereby a material with dielectric constant of less than 1.5 is needed.

Air has the lowest dielectric constant of all know materials. As it is not possible to deposit or build structures on air, hence a sacrificial layer is needed in the deposition process, and would be removed in the final step leaving behind air gaps in the IC. Such a scheme is shown in Figure 11.

The criteria of a sacrificial material are: ease of synthesis with conventional deposition methods, does not affect and is not affected by deposition of other materials during the fabrication process, ease of removal and leaves behind negligible residue. Some of the current materials which are being used include carbon and a polynorbornene copolymer. However they suffer the disadvantages of requiring an oxygen atmosphere for removal, high decomposition temperature (400˚C) and slow rate of decomposition. We propose the synthesis via hot-filament chemical vapor deposition of a novel material, polyoxymethylene (POM) which meets the above requirements.

POM can be formed from the polymerization of its monomer, formaldehyde (CH_2O). First, the solid trioxane, a 6-membered ring trimer of formaldehyde, is vaporized and introduced into the reactor. It is cleanly decomposed by the hot filament process into 3 mole-

Continued

cules of formaldehyde which then polymerizes to POM under suitable conditions of pressure and substrate temperature. Fourier transform infra red (FTIR) technique is used to confirm the structure of the POM films, and thermogravimetric analysis (TGA) has shown that the films begins to decompose at temperatures below 300˚C. POM decomposes into formaldehyde via an unzipping mechanism in an inert atmosphere.

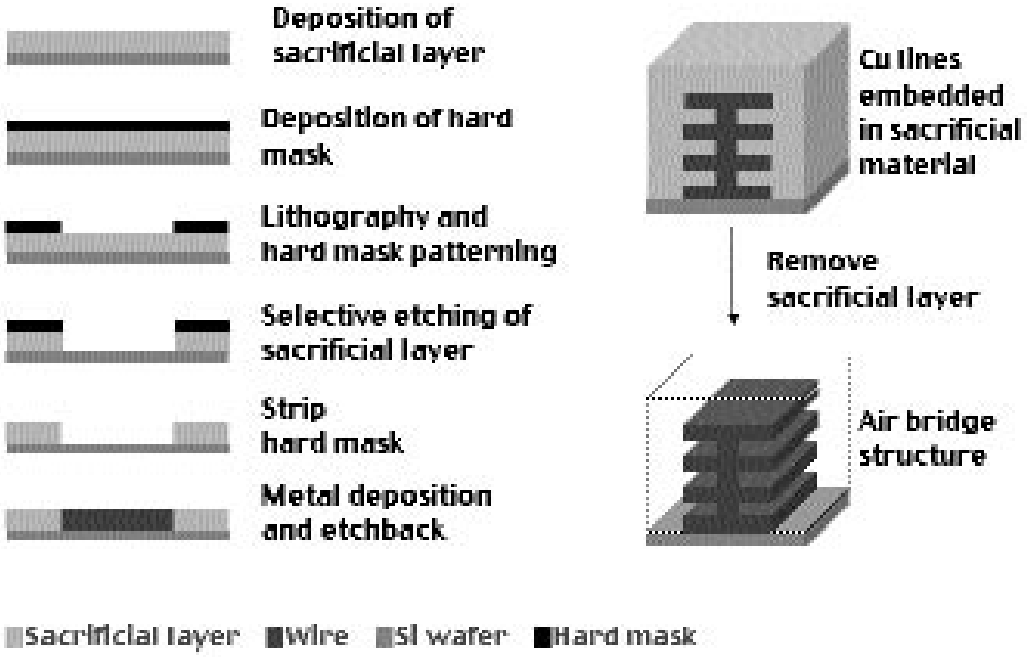

Fig. 11

Cluster Ion Beam Processing

Personnel
N. Toyoda, A. Agarwal and K. Wada (L.C.Kimerling)

Sponsorship
NSF, MRSEC and EPION

As shrinking the size of electronic, magnetic and photonic devices, it is urgent to address crucial material-related issues: interconnect materials, thin gate oxides, processing for ultra-fine structure and ultra-shallow junction formation. This project addresses two of the challenges, ultra-shallow junction and ultra-smooth processing with cluster ion beam.

For shallow implantations, a boron cluster with ten boron atoms ($B_{10}H_{14}$) is used. As the energy of individual boron atom is almost 1/10 of the total energy of $B_{10}H_{14}$ ion, boron atoms can be implanted into the very shallow region. Also, since a cluster contains 10 boron atoms, the total ion dose can be reduced by 1/10 of the B^+ implantations. Therefore, cluster ion implantation is a quite efficient method for the ultra-shallow implantation. The cluster ion implantation is successfully demonstrated to fabricate a 40nm PMOSFET as shown in Figure 12. This device has shown better electrical characteristics than current state-of-art technology.

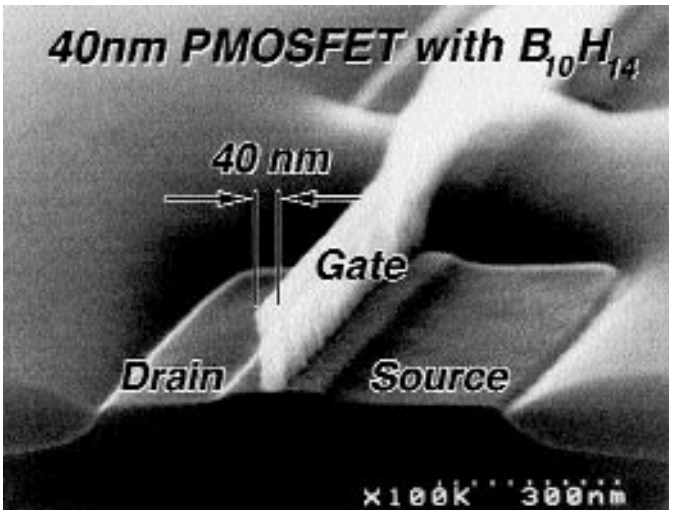

Fig. 12: SEM image of 40nm PMOSFET fabricated with $B_{10}H_{14}$ implantation.

As the impact process of cluster ion is completely different from that of monomer ion impact, defect reaction kinetics induced by cluster ion implantation have to be understand. The purpose of this project is to find the mechanism of these defects reaction kinetics from dose, energy and heat treatment dependence of defect formation. This new knowledge will be used to define an enhanced process window.

Another application of the cluster ion beam is surface smoothing. There are huge requirements to smooth various substrates or structures, where mechanical polishing cannot be employed. Cluster ion beam polishing is a low-damage and is easy to control polishing or etching conditions compared to the mechanical polishing. The smoothing with cluster ion beam is employed for various materials, such as poly-Si waveguide, giant magnetoresistive device, multi-layer optical filters, GaN films or diamond films.

Continued

Solventless Lithography

Personnel

H. G. Pryce Lewis (K. K. Gleason); G. L. Weibel and C. K. Ober, Cornell U.; M. Rothschild, MIT Lincoln Lab

Sponsorship

NSF/SRC Engineering Research Center for Environmentally Benign Semiconductor Manufacturing

Thin films produced by Chemical Vapor Deposition (CVD) show promise as materials capable of undergoing patterning by lithographic means. In this work, we consider the use of fluorocarbon and organosilicon films deposited by hot filament CVD (HFCVD) for producing nanometer-scale features. HFCVD is a non-plasma technique which offers the ability to tailor the chemistry of films with polymer-like structure.

Both fluorine- and silicon- containing polymeric materials are under consideration as candidates in next-generation microelectronics technologies. Their transparency makes them ideal resist candidates for 157-nm lithography, and their low dielectric constant makes them strong contenders as interconnect materials. Our collaboration is aimed at merging the role of resist and low-k dielectric. Specifically, we are investigating a direct dielectric patterning process in which a material is deposited by CVD, exposed, and developed using no wet chemistry, as illustrated in Figure 13.

The film is exposed using e-beam or a 157-nm source, and developed using supercritical CO_2 as a dry developing medium. The patterned film then serves as a low-k interconnect material. This technology would greatly simplify future device manufacture by reducing the number of steps involved in patterning. Furthermore, supercritical CO_2 offers many processing advantages over wet development, including improved resolution and the prevention of pattern collapse. This is due to its good selectivity, high diffusivity, and low surface tension. Supercritical CO_2 also offers many environmental, health and safety advantages over conventional spin-on technology, which typically results in large quantities of waste materials.

With such a scheme, we have demonstrated positive-tone contrast in fluorocarbon HFCVD films, and fully-developed images of 1-micron have been obtained from e-beam exposure. An AFM micrograph of these lines is shown in Figure 14.

Contrast can be optimized by adjusting film chemistry during the deposition process. We are currently investigating the incorporation of irradiation-sensitive moieties into film structure to increase sensitivity and improve resolution.

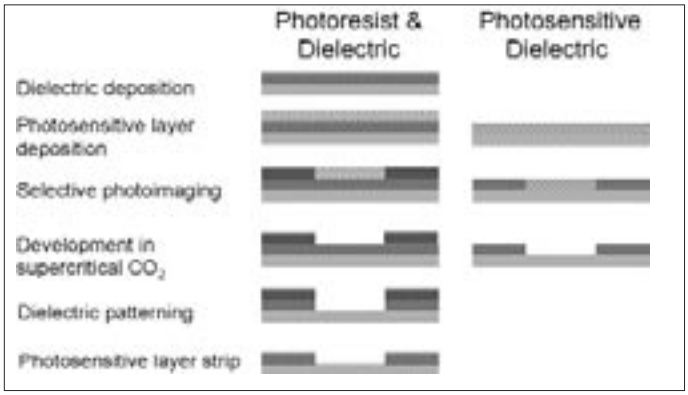

Fig. 13

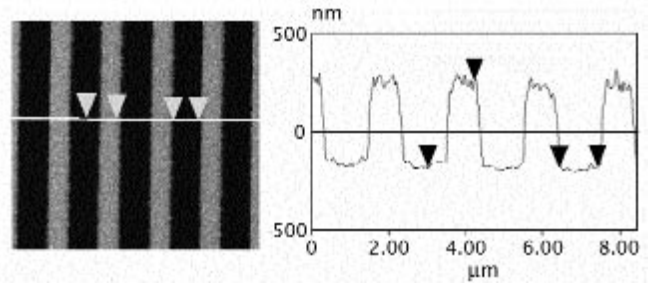

Fig. 14

Laser-driven Liquid Phase Epitaxy

Personnel

M. Reddy, J. Megursar (C. G. Fonstad, Jr. in collaboration with Dr. D. Ehrlich, Revise, Inc.)

Sponsorship

Revise, Inc.

We were approached by Revise, Inc. a manufacturer of precision laser-based patterned etching and deposition equipment for the semiconductor industry, to work with them on a DARPA-funded program they had to experimentally evaluate an idea to use their systems to do laser-driven liquid phase epitaxy (LD-LPE) as a possible approach to heterogeneous integration. This work was conducted for a one-year period starting in the fourth quarter of 1999, and led us to the conclusion that LD-LPE is not practical with the available equipment. None the less, the research program did result in the development of model systems with which to study LD-LPE and advanced our understanding of LD-LPE.

The model system developed for out LD-LPE studies consists of a sequence of layers deposited on the substrate of interest in our molecular beam epitaxy (MBE) system. The first layer is 1-2 μm of indium. On this a few-100 nm of InAs are deposited. The thickness of this layer is chosen such that the layer can be completely dissolved by the In at some target temperature. The InAs is then capped outside the MBE system by a deposited SiO_2 or Si_3N_4 encapsulating layer, and the sample is ready for laser radiation. The idea is that when the laser beam hits a spot it will melt the indium there and some of the InAs will go into solution. When the laser beam moves away from that spot, the In will cool from the substrate up, and the InAs will come out of solution epitaxially on the substrate. The encapsulating layer blocks the loss of arsenic and keeps the system planar.

Considerable effort was devoted to developing techniques to form these model structures. A conventional solid-source MBE system was used, but because of the low melting temperature of In, the substrate had to be kept as cold as possible (near room temperature, in this case). After the substrates are loaded and baked to desorb moisture, they are allowed to cool for an extended period before being transferred into the growth chamber. The substrate heater was not used and the substrates' exposure to hot effusion cells was minimized. With these precautions it was possible to obtain very smooth initial surfaces.

The laser system variables include the laser power, spot size, and scan rate and pattern. A large number of experiments were conducted to determine the combination of variables that melted the indium film but did not compromise the integrity of the encapsulating layer. Samples were then treated under conditions within this range with single and multiple passes. After exposure a variety of analytical techniques were used to assess the results.

No epitaxy was observed, but it was found that the InAs did go into solution, and in some cased there was evidence of the transport of InAs from the top layer to the vicinity of the substrate surface. After numerous experiments, it was concluded that successful LD-LPE will require that an ambient over pressure of the volatile group V component be provided (As in this case, N in the case of GaN, etc.), and this was not possible with the equipment available and the laboratory restrictions in place at Revise. Even then, it seems unlikely that LD-LPE will compete favorably with other laser-driven deposition techniques, such as laser-driven MOCVD. Consequently the program has been continued.

Molecular Beam Epitaxy of InP-based Heterostructures on Silicon Substrates and Membranes

Personnel
K. H. Choy (C. G. Fonstad, Jr.)

Sponsorship
3-D IC, Inc.

Epitaxial growth of III-V compound semiconductors on silicon is significant because, if successful, it can greatly simplify heterogeneous integration. It would, for example, enable dense arrays of optical sensors for infrared wavelengths in which the optically active elements are made of III-V materials and the read-out function is accomplished by silicon circuitry.

Generally, there are three hurdles for successful epitaxial growth of III-V materials on silicon: differences in lattice constants, thermal expansion coefficients, and lattice polarity (i.e. polar vs. non-polar) These differences yield a high density of threading dislocations and antiphase domains in the epitaxial films, which drastically reduce the efficiencies and lifetimes of devices made in them. For diodes and detector structures, these dislocations can also contribute to larger reverse-bias currents or dark currents, reducing speeds and sensitivities.

Antiphase domains can be suppressed by using silicon substrates tilted by a few degree from the (100) plane towards the (011) plane. Threading dislocations can in principle be reduced by annealing. However, additional defects can be generated in the annealing process, as well as during cool down after growth, due to the high mismatch in thermal expansion coefficients. In order to overcome this problem, we propose growing III-V materials on suspended silicon membranes, as illustrated in Figure 15. If a silicon membrane is much thinner than the epitaxial layer grown ontop of it, the membrane, rather than the epitaxial layer, will absorb most of the stress generated in the composite structure during the cool down cycle and during any annealing cycles.

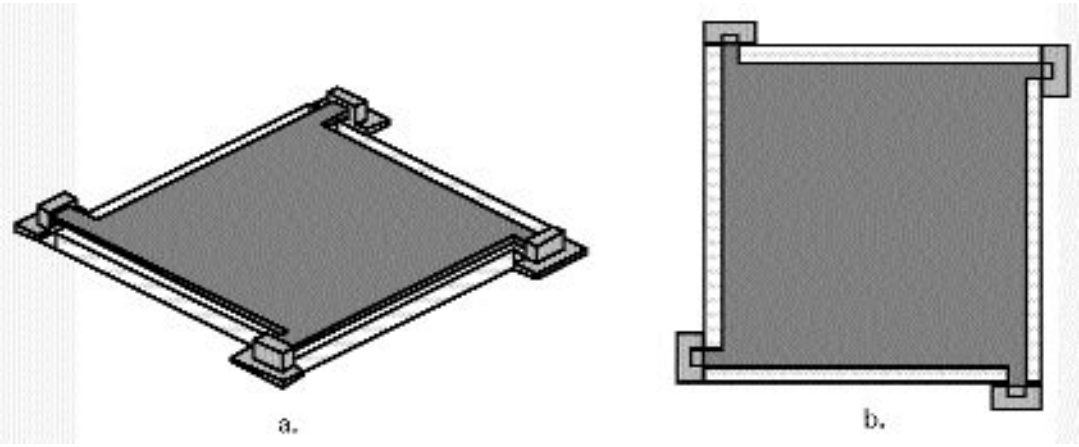

Fig. 15: Perspective (a) and top (b) views of a suspended silicon membrane on an SOI wafer made using MEMS selective etching techniques. The membrane is held at its four corners, and deep trenches are etched along the sides. so the growth on the membrane will be free from the deposition on the edges.

Continued

For our work, picked InP as the III-V material of interest, and we have first tried to achieve favorable conditions for its molecular beam epitaxial growth on bulk Si. Previous work growing InP on Si has used MOCVD, rather than MBE. Typically, Si substrates misoriented 2-3 degrees from (100) or (111) orientations have been used, because they were found to yield far better results than (100) substrates with no misorientation. Thick films, in the order of 2-4 μm were routinely grown due to the higher growth rate of MOCVD. A thin intermediate layer of GaAs was sometimes used between the InP layer and the silicon substrate.

In our work, we have used (100) silicon substrates without misorientation. The samples were treated in standard RCA cleaning process, with an added final quick hydrofluoric acid dip without rinsing. This leaves the surfaces terminated by hydrogen. Care was taken to minimize the time between the cleaning of the samples and their loading into the MBE system. All the ion gauges were turned off in the chambers where the sample resided. Complete oxide removal and surface cleaning were achieved by using a high temperature catalytic hydrogen cracker. The cracking and substrate temperatures were 2200˚C and 630˚C, respectively. After one hour of oxide removal process, the surfaces gave strong 2X2 reconstruction as observed by RHEED.

The growth was done in two steps: First, an initial 100 nm was grown at a slow growth rate of 0.2 μm/hr. Then, a 1 μm layer was deposited at 0.8 μm/hr under conditions we have found to be critical to overall success. In the second layer, all growth parameters are identical to those used in lattice-matched InP on InP growths.

The FWHM of InP X-ray peaks was 300 arcseconds, and the photoluminescence spectrum is comparable to that of InP on InP, 30 times less intense. These results are comparable to the best published results for MOCVD growth of InP on Si, which is particularly encouraging because:

1) these results are, to our knowledge, the first ever MBE heteroepitaxial growth of InP on Si,

2) the films in this study were of much thinner than those in the MOCVD work, and similarly thick films would be expected to give even better results in our case, and

3) we have found it unnecessary to use misoriented substrates.

We presently are in the process of measuring the threading dislocation density as a function of film thickness, and of investigating the use of GaAs, InP or GaP as intermediate layers between the InP layers and silicon substrates. Preparation of the membrane structures pictured above is also proceeding.

Passivation of Copper Surfaces with Organic Monolayers

Personnel

H. M. Lei (K. K. Gleason)

Sponsorship

MARCO Focused Research Center on Interconnect (SRC/DARPA)

In the microelectronics industry, there is a constant trend of increasing wafer size and decreasing feature size on the device wafers. The major consequence of smaller feature size devices fabricated on larger wafers is higher parasitics due to longer transmission lines and more closely spaced interconnects. These parasitics result in longer RC time delay. Because of its high electrical conductivity (65% higher than aluminum) and its greater resistance to electromigration, copper is replacing aluminum as the metal of choice in connecting millions of transistors on a chip. However, copper can diffuse readily into InterLayer Dielectrics (ILD), giving rise to unanticipated yield or reliability problems, and can diffuse into the Si substrate, causing excessive leakage current. Hence, a diffusion barrier layer is, so far, necessary to prevent copper movement into the Si-substrate and interlayer dielectrics. The very existence of these barrier layers, with thickness up to several hundred angstroms, will either increase effective resistivity or effective dielectric constant of the device, leading to overall increase in the RC time delay.

It is therefore our goal to find a solution towards the ultimate elimination of the physical barrier layer between Cu and low-k dielectric materials totally, thus realizing full benefits of using copper interconnects for its low resistivity. The main idea here is to modify the copper surface with organic ligand monolayer, hence passivating copper atom movement along its interface with ILD. A preliminary screening test identified BenzoTriAzole (BTA) as the model organic compound that can potentially passivate the copper surface with a monolayer. Atomistic simulation shows that each BTA molecule bonds to two Cu atoms through its nitrogen lone pairs, thus no surface Cu atoms are free to act as diffusion sites. The passivation capability of the BTA monolayer is tested under annealing conditions of 350^{o}C for 2 hours with N_2 ambient and is characterized using Variable Angle Spectroscopic Ellipsometry (VASE). The results show that, if delivered properly, BTA monolayer can indeed work as an effective passivation layer in inhibiting the movement of copper atoms under thermal stress. This is evidenced by the absence of change in the film structure's optical properties, before and after annealing. The preliminary success in proving the feasibility of the concept of organic monolayer passivation lends us promising directions for future research in this arena.

Semiconducting Gas Sensors

Personnel
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Sponsorship
NSF

Ceria-Praseodymia solid solutions show extensive deviations from stoichiometry, intermediate ordered structures, and a variety of transport mechanisms that render them of interest as the active component of gas sensors. These materials, are being systematically investigated by a variety of methods including impedance spectroscopy, coulometric titration and X-ray diffraction. The influence of grain size, down to the nanoscale, on device performance is under investigation.

Resonant Gas Sensors

Personnel
H. Seh and H. Fritze (H. L. Tuller)

Sponsorship
NSF and DAAD

Piezoelectric materials with ability to operate at elevated temperatures are being investigated as potential platforms for gas sensors. Measurements include resonant characteristics, electrical conductivity and oxygen diffusivity as functions of temperature and oxygen partial pressure. To date resonators have been successfully operated to 900^{o}C.