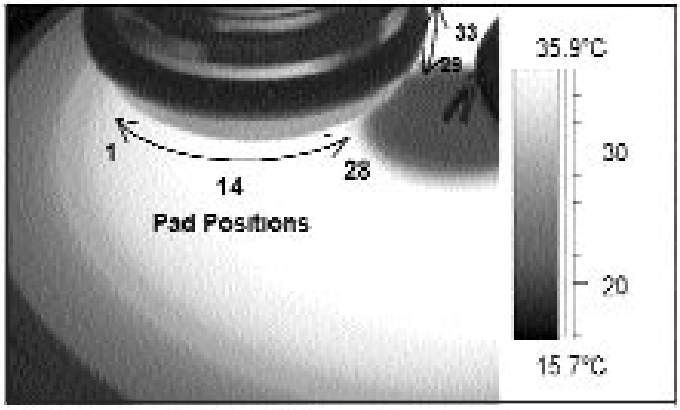
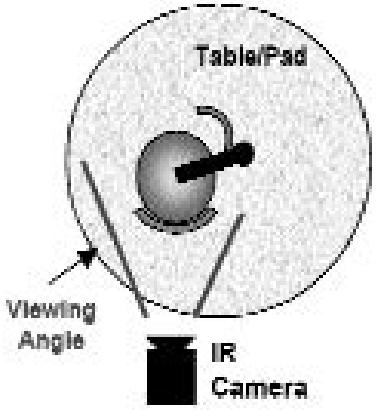
# Manufacturing

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# Manufacturing

- ***Advanced Run by Run Control for Epitaxial Silicon Deposition***
- ***Thermal Imaging Sensor for CMP Endpoint Detection and Uniformity Control***
- ***Characterization of Wafer Bonding in 3D Integrated Circuits***
- ***Alternative Process Chemistries and Chemical Recycling***
- ***Statistical Metrology - Quantifying, Modeling, and Assessing the Impact of Spatial Variation in Semiconductor Manufacturing***
- ***Test Masks for Characterization of Copper CMP Pattern Dependencies***
- ***Modeling the Effect of Interconnect Variation on Circuit Performance***
- ***Chemical Mechanical Polishing for Shallow Trench Isolation (STI)***
- ***Modeling of Fixed Abrasive CMP***
- ***Labnet Software***

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# Advanced Run by Run Control for Epitaxial Silicon Deposition

## Personnel
A. Gower (D. Boning and M. McIlrath)

## Sponsorship
NSF, NIST ATP (with On-Line Technologies and Applied Materials)

Silicon epitaxial deposition is typically the first step in a process flow, where the crystal lattice of the bulk silicon is extended through growth of a new silicon layer with a different doping level than the bulk. Matching target epi film thickness and resistivity parameters is difficult, but crucial, for the subsequent fabrication of properly functioning devices. Spatial nonuniformity of thickness or resistivity, and the drift over time of these results, may exist as illustrated in Figure 1. The availability of an in-line sensor for measuring epitaxial silicon (epi) film properties (by On-Line Technologies) provides crucial information to enable integrated run-to-run control of the epi deposition process.

A testbed system is under development with On-Line and Applied Materials using a Centura tool with an epi deposition chamber, an in-line epi film thickness measurement tool, and off-line thickness and resistivity measurement systems. We have previously demonstrated integrated, model-based run-to-run control of the deposited epi film thickness at the wafer's center via the in-line metrology tool and automatic updates of the deposition time. An advanced multi-objective controller is now under development which seeks to provide simultaneous epi thickness control on a run-to-run basis using the in-line sensor, as well as combined thickness and resistivity uniformity control on a lot-to-

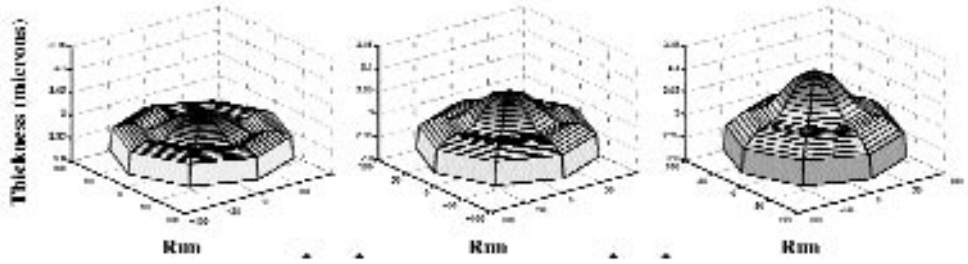


*Fig. 1: Spatial nonuniformity and run to run drift in silicon epitaxy film thickness.*

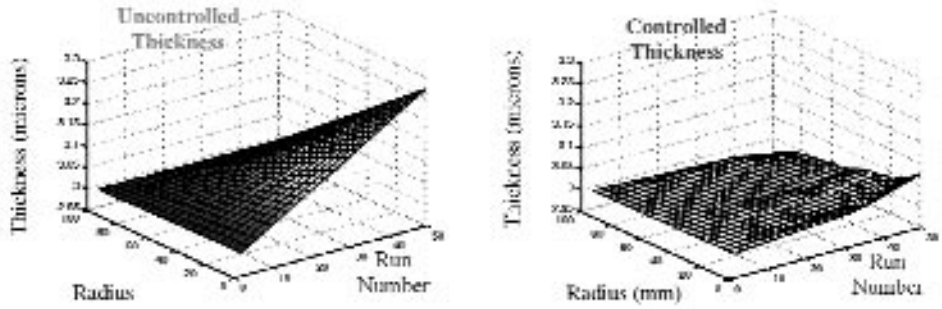


*Fig. 2: Simulated epi run by run control. The uncontrolled thickness on the left shows a rapid process drift where radial uniformity becomes successively worse. The controlled thickness on the right maintains thickness target and uniformity.*

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lot basis using the off-line thickness and resistivity sensors. A model-based controller updates multiple process settings between runs to control the radial uniformity (rather than simply the average) of thickness and resistivity. Enhancements to the "standard" linear EWMA-based control algorithm account for the time-based effects in controlling thickness, and handle the combination of run-to-run and lot-to-lot feedback loops. Fig. 2 shows a simulated control scenario, demonstrating the ability of this approach to achieve excellent control. Experimental validation of the multivariate controller is planned.

# Thermal Imaging Sensor for CMP Endpoint Detection and Uniformity Control

## Personnel

D. White (D. Boning)

## Sponsorship

NSF/SRC ERC for Environmentally Benign Semiconductor Manufacturing

Chemical-mechanical polishing is essential in present and future IC technology. The use of CMP places stress on water and slurry consumption, pad consumption, monitor and look-ahead wafer usage, and generation of waste and potentially hazardous materials. Most CMP process development is currently conducted without consideration of environmental issues. The objective of this project is to develop process control methods that incorporate environmental objectives as a key concern. The approach being developed is the practical control of the CMP process by integration of sensor, models, and feedback control technology, through which the process can be optimized for improved performance, minimal consumption, and elimination of monitor and look-ahead wafers.

One key barrier is the need for in-situ sensors to measure polishing uniformity across the wafer. We are developing an approach to indirectly sense and monitor the uniformity of a wafer being polished in-situ. The system incorporates an infrared (IR) sensor which is used to monitor the temperature of the polish pad immediately after it has been in contact with the wafer. An IR temperature profile can be obtained by monitoring a series of points corresponding to varying radii along the pad surface, as illustrated in Figure 3. This profile is then analyzed spatially to determine the non-uniformity of the polishing conditions. By understanding the correlation between the pad temperature and the spatial wafer temperature profile during polishing we hope to predict the nonuniformity of the wafer that has been polished in-situ eliminating the need for look-ahead wafers.

An especially interesting application of in-situ thermal imaging is the observation of end-point uniformity. In copper and other metal polishing processes, the bulk metal material must be removed completely across the entire wafer surface, leaving behind copper in patterned trenches to form interconnect lines or vias. The uniformity of clearing across the wafer is critical to

*Continued*

avoid overpolish induced dishing and erosion of the interconnect. Shown in Figure 4 are thermal time traces for a subset of spatial points across the pad. It appears that once the copper has cleared and the underlying barrier metal exposed, the temperature decreases (due to decreased friction with the barrier material). The detection of clearing at different times along various radial positions on the wafer is thus enabled, opening the possibility for improved endpoint detection and feedback control to improve uniformity.

Current work is focused on developing estimators for removal rate and endpoint uniformity, based on the thermal signatures. Comparison with in-situ optical reflectometry is also being pursued, with the goal of obtaining information so that the process can be better controlled on a run to run basis.

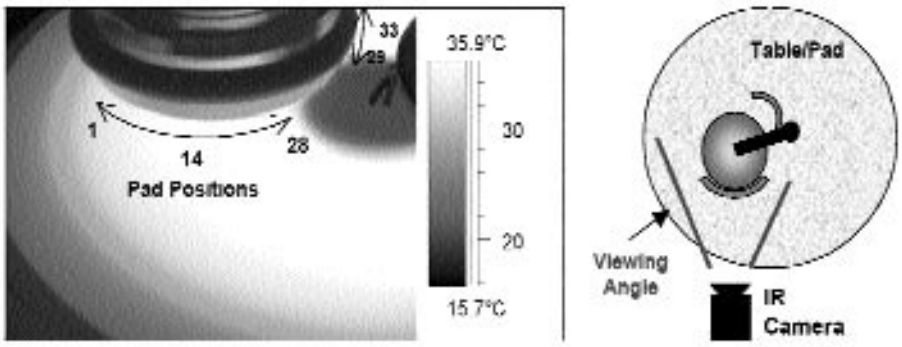


*Fig. 3: Thermal pad imaging in CMP. An Agema 550 infra-red camera is focused upon the polishing pad behind the trailing edge of the carrier. Temperature measurements at the indicated discrete pad positions in the image provide spatial information regarding polish uniformity and endpoint.*

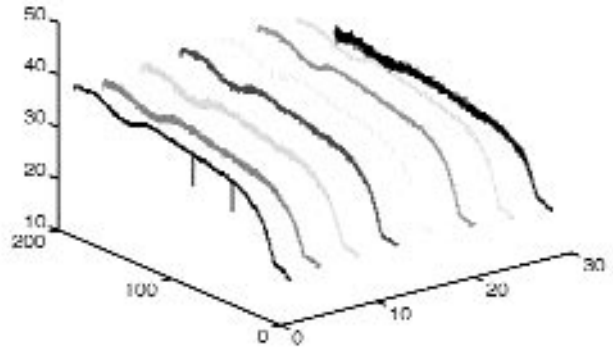


*Fig. 4: Temperature measurements for positions along the pad during copper CMP. The temperature changes at 140 seconds occur at slightly different times for different positions, capturing the nonuniformity of endpoint.*

# Characterization of Wafer Bonding in 3D Integrated Circuits

## Personnel

R. Tadepalli and R. Krishnan (L. R. Reif, M. A. Spearing, C. V. Thompson)

## Sponsorship

MARCO (through a subcontract from Georgia Institute of Technology)

3D integration in VLSI circuits provides a possible path to the achievement of high system performances. This technology enables devices to be placed on more than one layer and hence achieves higher device density and shorter critical interconnect paths. System performance is improved by the reduction of interconnect path lengths. 3D integration relies on the bonding of active device wafers , with the layers electrically interconnected using high aspect ratio vias. The device wafers have multiple layers of metallization and, in our work, are bonded through bonding of the topmost layers of copper interconnects.

One of the critical issues in the implementation of 3D integration is the evaluation of the bond strength and quality achieved through wafer bonding. Interface fracture failure is highly likely given the high thermal stresses developed during processing and also during service. Thus, robust methods have to be developed to determine the strength of the bonds by measurement of interface adhesion.

We have initiated a set of tests to evaluate the bond strength. First, we will investigate bonding of wafers with copper lines. Each wafer has parallel lines of Cu/Ta of varying widths, on a blanket $SiO_2$ layer. The oxide is deposited by thermal oxidation, while the Cu/Ta is deposited by evaporation and patterned using lift-off technique. The wafers are bonded in the EV bonder and annealed in $N_2$ atmosphere after bonding. We will vary the parameters in the bonding process, namely, temperature, time of anneal, to determine their effect on the bond strength and quality.

Measurement of interface adhesion is done by the 4-point bend test. The critical strain energy release rate obtained from this test is equal to the interface fracture toughness. Values of interface fracture toughness for various bonded pairs, bonded under different conditions , can be obtained. In this manner, we can quantify the bond strength under different bonding conditions and compare them to arrive at optimum parameters.

We are also developing techniques for fabrication of through wafer vias so that multiple device layers can be connected. This will also allow development of test structures for electrical characterization of bonded interfaces. We have also initiated basic studies on the nucleation and microstructure evolution that occurs during electromechanical deposition of copper. These studies would enable us to achieve void-free filling of high aspect ratio structures and reliable integration of 3-D devices.

# Alternative Process Chemistries and Chemical Recycling

## Personnel

J. Chan, A. Reddy, and J. Michel (L. C. Kimerling) in collaboration with Millipore (Bedford, MA) and IBM (Yorktown Heights, NY)

## Sponsorship

NSF/SRC Center for Environmentally Benign Semiconductor Manufacturing and Wafer Engineering and Defect Science Consortium

Decreasing feature size, low cost, and high yield continue to drive the silicon electronics industry. Perfect atomic surface silicon is therefore needed to manufacture high yield devices of submicron dimensions. In addition, there are rising environmental concerns, and EPA regulation is broadening its control over industrial environment. The solution to maintain traditional low cost wet cleaning is to investigate environmentally benign alternative chemistries and improve the effectiveness of this cleaning technology simultaneously.

To investigate atomistic perfection, our group has developed a measuring system, Radio-Frequency Photoconductance Decay, to measure surface defect in-situ. The sensitivity level of this measurement is 108 defects/cm2, which is corresponded to approximately100 parts per billion of surface coverage. This highly sensitive device assists the development of contaminant control in dilute hydrofluoric acid (HF) bath, and an alternative method of passivation (protecting) the bare silicon surface.

To achieve low cost and environmentally benign semiconductor manufacturing, the industry has been exploring the use of dilute chemistries. However, our studies show that copper (Cu) deposition on silicon surfaces increase dramatically with dilute hydrofluoric acid. Our results indicate, for the same concentration of Cu, a seventeen and a half times increase in the deposition rate for a 500:1 bath as compared to a standard 100:1 bath. We therefore conclude that tight control over metal contamination is required for dilute hydrofluoric acid bath.

With our expertise in surface characterization, we expand our capability to measure metal contamination in HF bath with our collaborators at Millipore. Our bath monitor converts metal deposition rate to the level metallic contamination in solution. This technique allows in-situ monitoring of the quality of HF bath with sensitivity about 20 parts per trillion (ppt) of Cu in 500:1 HF solution. This warns the operators when to change HF bath to meet the submicron technology environment.

The other problem with current industry standard using dilute hydrofluoric acid (DHF) as the last cleaning step to create hydrogen terminated silicon (Si-H) surface is that a perfect hydrophobic hydrogen terminated surface will never be achieved in wet processing because the surface is always left with some fluorine terminations. The amount of fluorine terminated silicon is proportional to the concentration of hydrofluoric acid used. Secondly, although Si-H is non-polar in nature, it degrades in water to form Si-OH. This problem has been improved with the Marangoni drying technique. While it is relatively stable because of its high covalent bonding character, queuing times longer than 10 min. degrade the surface.

To restore the degraded surface, re-clean steps are needed before further processing. These series of re-cleaning steps cause increasing yield loss, time loss, and chemical wastage. Therefore, we have developed a new surface preparation technique, which utilizes alkoxy to protect the bare silicon surface. The current alkoxy passivation is compatible with current industrial processing technique. We have optimized the alkoxy passivation for stability and particle rejection. An alkoxy-passivated surface is 50 times more stable than a hydrogen passivated surface (see Figure 5). The alkoxy-passivated surface therefore resists degradation and oxidation 50 times longer, making expensive re-cleans unnecessary.

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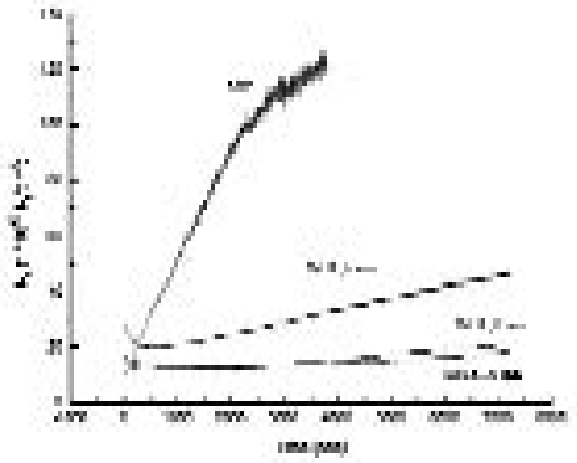

Fig. 5: Stability of H- and MeO-passivated Si surfaces in air.

# Statistical Metrology - Quantifying, Modeling, and Assessing the Impact of Spatial Variation in Semiconductor Manufacturing

## Personnel

R. Dutt, T. Gan, B. Lee, V. Mehrotra, T. Park, S. Sam, T. Tugbawa, K. Gonzalez-Valentin and J. Panganiban (D. Boning)

## Sponsorship

Interconnect Focus Center (MARCO/DARPA), PDF Solutions, SEMATECH

As device and interconnect dimensions continue to scale toward tenth-micron dimensions, maintaining process and structure uniformity at each processing step is increasing in importance and difficulty. Yield loss due to systematic sources of variation will begin to supersede loss due to particle defects and random sources of variation. Circuit performance will also become increasingly limited by device and interconnect variation.

We are developing statistical metrology methods to quantify, model, and understand the impact of spatial variation in semiconductor processes and device/interconnect structures. Key elements of the methodology include test structures, experimental designs, and measurement methods to gather the large volumes of data needed for statistical analysis; the development of algorithms and tools to decompose and identify variation sources; modeling methods to capture the systematic elements of device or interconnect variation (particularly as a function of layout parameters); and CAD tools and methods to understand the impact of such variation on circuit performance and yield.

The methods have been applied in two primary areas: pattern dependencies in chemical-mechanical polishing (CMP), and variation in polysilicon and metal linewidths. The following abstracts summarize work on methods for rapid characterization and modeling of CMP in several processes, including interlevel dielectric (oxide) polishing, shallow trench isolation (STI), and in copper damascene polishing. Finally, development and application of CAD tools which utilize variation models (such as those generated in the above experiments) to study the impact of variation on circuit performance is summarized. These studies are collaborative with partners at Applied Materials, Texas Instruments, Sandia National Laboratories, IBM, PDF Solutions, Lucent Technologies, TSMC, Conexant, and SEMATECH. Copper CMP suffers from well-known but poorly

# Test Masks for Characterization of Copper CMP Pattern Dependencies

## Personnel
T. Park, T. Tugbawa (D. Boning)

## Sponsorship
SEMATECH

understood dishing, erosion, and other pattern dependent problems. We are developing methods to support the systematic study and characterization of these pattern dependencies through the use of electrical and physical test structures and measurements. Three length scales must be recognized: a several mm "planarization length" related to as-deposited copper pattern density, a "transition length" on the order of 100-μm over which erosion profiles change as a function of the local neighborhood, and the feature scale (on the order of 1-μm) dependencies of dishing on line width and erosion on line space. As shown in Figure 6, the fundamental structure to explore these dependencies consists of large arrays of lines (~2 mm in size) with a corresponding nearby isolated line, designed as a function of the line width and line space (or metal pattern density and pitch). Electrical versions of these structures enable the extraction of metal line thickness from electrical data. Profilometry provides valuable data on oxide erosion (as well as dishing within individual copper lines), as illustrated in Figure 7.

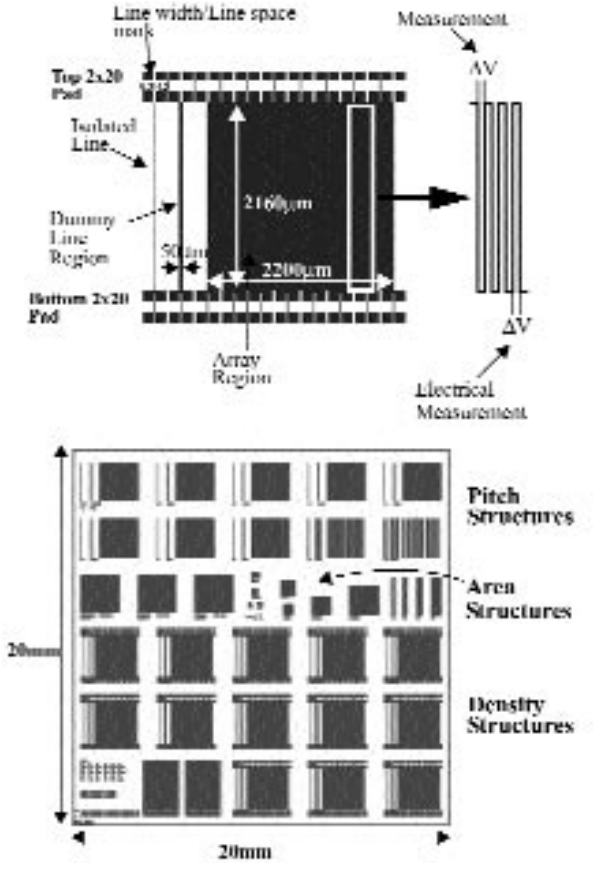


*Fig. 6: Test structure (above) and test mask (below) for characterization of pattern dependencies in the copper CMP.*

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*Fig. 7: Surface profilometry scans showing dishing and erosion for different copper line width (Lw) and line space (Ls) layout parameters.*

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These test structures and measurements enable the analysis of trends in dishing and erosion for process optimization, consumable or tool evaluation, and design rule generation. Multilevel polishing effects are also being studied, where the combination of electrical and profilometry data is crucial in order to assemble a complete picture of pattern effects. Results from the polish of overlapping test structures on metal 1 and metal 2 are shown in Figure 8. Further work is underway to explore the interaction between copper and low-K dielectric polishing, and to couple these experimental works to models of the copper process for circuit manufacturability and performance impact assessment.

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*Fig. 8: Surface topography and copper line thickness in metal 2 structures after CMP, as a function of overlap (illustrated at bottom) with metal 1 polished structures.*

# Modeling the Effect of Interconnect Variation on Circuit Performance

## Personnel

V. Mehrotra (D. Boning and A. Chandrakasan)

## Sponsorship

Interconnect Focus Center (MARCO/DARPA), PDF Solutions, IBM

In order to study the impact of long range spatial and pattern dependent variation on circuit performance, CAD tools must be extended and integrated in innovative ways. In this work, we are developing the CAD infrastructure and applying these tools to study device and interconnect variation impact on circuit performance.

Several case studies are under investigation, including skew in clock distribution circuits, optimally buffered signal paths, delay in parallel data or bus lines, and cross-talk coupling in interconnect, all as a function of variation. In addition, we are examining how variation impact affects technology as we scale to the 50 nm node.

First, we consider a balanced H clock tree configuration. Without any variation, some load imbalance (from the tree design) can be expected. We considered the skew introduced due to copper line thickness variation from systematic pattern dependencies, as well as skew from random and systematic device matching variations. The results are summarized in Table 1, where we see that an increasing portion of the clock cycle will be consumed by variation induced skew (nearly 30% at the 50 nm technology generation).

We also examine the effect of variation on optimally buffered interconnect. We choose a desired clock frequency constraint and compute the impact of variation on the maximum interconnect length, Lmax. We find that Lmax degrades due to variation in the geometric interconnect parameters, as summarized in Figure 9. As technology scales, variation modeling of both interconnect and device parameters will become increasingly important in reducing uncertainty.

*Fig. 9: Effect of metal thickness and metal linewidth*

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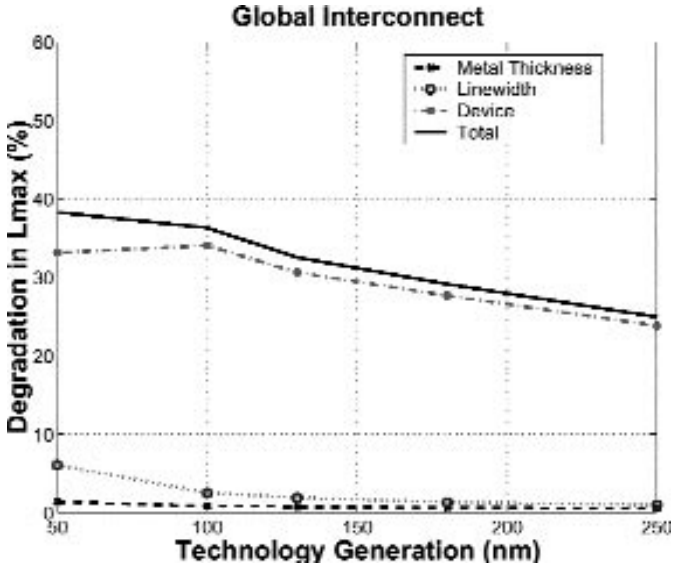
| Variation Source | 180nm | 50nm | 180nm | 50nm |
|---|---|---|---|---|
| None | 45.53 | 22.12 | 4.55 | 6.62 |
| Cu CMP (systematic model) | 36.85 | 14.83 | 3.69 | 4.44 |
| Devices & $V_{DD}$ | 116.58 | 71.28 | 11.66 | 21.34 |
| Devices & $V_{DD}$ (tighter $L_{eff}$ tolerance) | 96.96 | 53.40 | 9.70 | 15.59 |
| Total Skew (worst-case device & $V_{DD}$ tolerances) | 162.11 | 93.40 | 16.21 | 27.96 |
| Total Skew (systematic model for metal thickness & tighter $L_{eff}$ tolerance) | 133.81 | 68.23 | 13.38 | 20.43 |
| **Skew Reduction (systematic models)** | **28.30** | **25.17** | **2.83** | **7.53** |
| **Units** | **psec** | | **% of clock period** | |

*Table 1. Effect of interconnect and device variations on clock skew, at the 180 nm and 50 nm technology nodes.*




*variations on the maximum global interconnect length, for different technology generations.*

# Chemical Mechanical Polishing for Shallow Trench Isolation (STI)

## Personnel
T. Gan, B. Lee (D. Boning)

## Sponsorship
PDF Solutions, IBM, Sandia National Laboratories, TSMC

Shallow trench isolation (STI) is a critical isolation technology as the drive for device density intensifies. However, solution of layout pattern effects at the CMP planarization phase is critical to cost-effective single-mask STI processes. Pattern effects in STI are particularly severe and complex; it is first manifest at the overburden oxide polish phase resulting in a nonuniform time-to-reach the nitride polish stop layer across the die. This necessitates over polishing to fully remove the oxide and ensure complete nitride stripping. The over polishing together with higher oxide polish rate results in substantial dishing of the trench oxide in dense trench regions and erosion of silicon nitride in the active device regions. In order to control and account for these pattern dependencies, understanding of the polish mechanism in both phases is needed.
In this project, we are exploring a variety of issues and alternatives to understand and optimize the STI CMP process. Pattern test masks have been designed and experiments performed to study polishing as a function of layout pattern, deposition style (e.g. HDP vs. conformal CVD, or combinations), slurry type (e.g. high selectivity cerium oxide slurries), and pad type (e.g. conventional stacked pad versus fixed abrasive). These efforts are coupled into an effort to develop extensions to our integrated pattern density and step-height CMP model for STI.

For the important case of a reverse-tone etchback STI structure as pictured in Figure 10, we have modeled the effect of overpolish time on oxide dishing and nitride erosion. The degree of dishing (a negative step height) and erosion are pictured in Figure 11, for different pattern densities. A tradeoff is apparent between the dishing and erosion, and an optimal polish time can be identified for a given process.

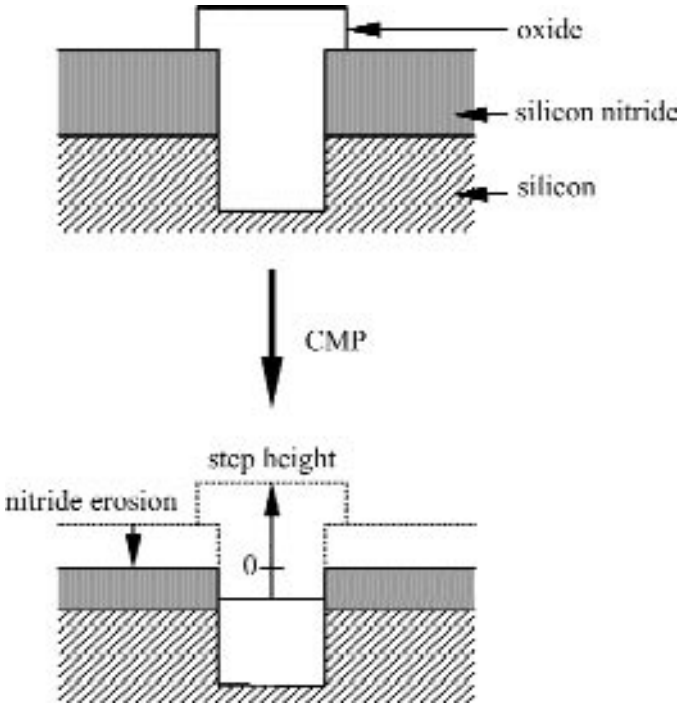



*Fig. 10: Change in step height and nitride erosion in an STI CMP process. The initial profile consists of oxide in the trench, where excess oxide over the active area (nitride regions) has been patterned and etched away prior to CMP.*

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# Modeling of Fixed Abrasive CMP

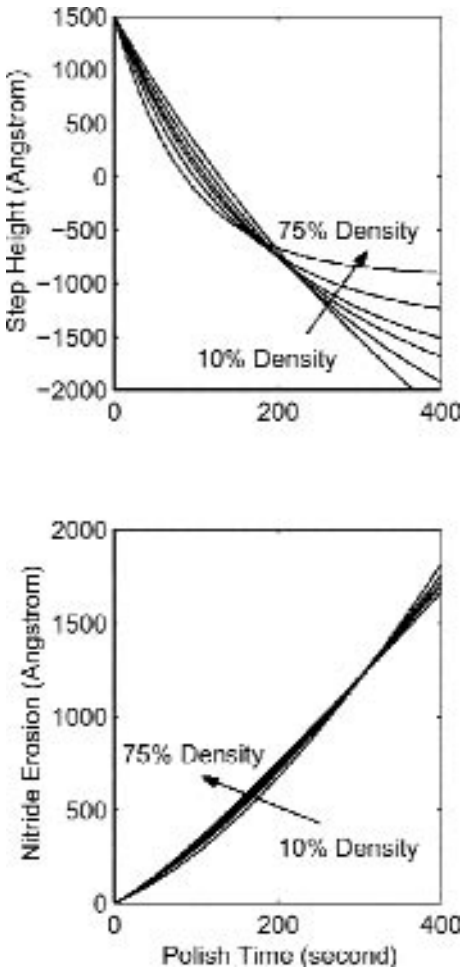


*Fig. 11: Step height (negative values indicate oxide dishing) and nitride erosion, for different STI pattern densities, as a function of polish time.*

## Personnel

B. Lee, R. Dutt (D. Boning)

## Sponsorship

IBM, Sandia National Laboratories

In order to reduce the amount of "down area" polish that occurs in STI and other CMP processes, the industry is investigating the use of "fixed abrasive" polishing pads. These pads incorporate the polishing particle (e.g. cerium oxide) into the pad structure. In this project, we have developed a layout dependent model to predict the amount of oxide polish one would expect on patterned wafers.

The first effect that must be captured is an unusual pattern density dependence of the removal rate. It is observed that the unpatterned (100% or "blanket") removal rate is very low, while the patterned rate increases dramatically as density decreases. We modify the traditional $1/\rho$ dependence to capture this effect, as pictured in Figure 12. Second, we find that the "up area" patterned rate (as in Figure 12) decreases linearly as a function of step height, approaching the low blanket rate. Combining these two effects, we have found good matching between experimental data and the model.

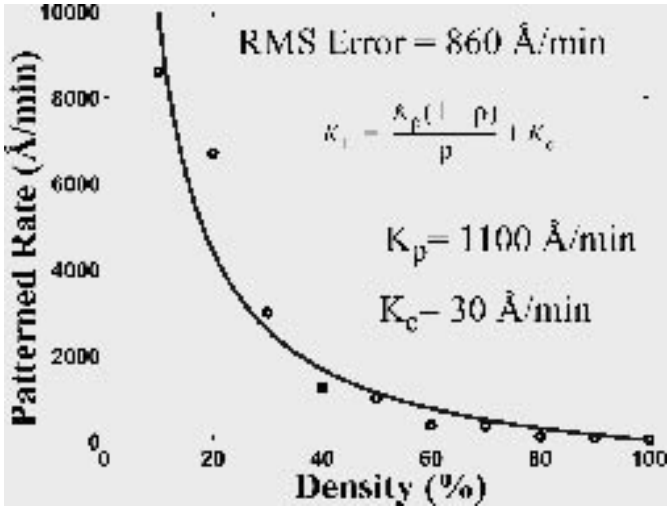


*Fig. 12: Patterned feature polish rate with a fixed abrasive CMP pad, as a function of pattern density.*

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As shown in Figure 13, one sees that rapid planarization of low density regions compared to the high density regions, followed by very little additional oxide removal after planarization. This has important implications for STI polishing: one must very carefully control the amount of oxide overfill if one is to planarize and fully clear oxide over nitride.

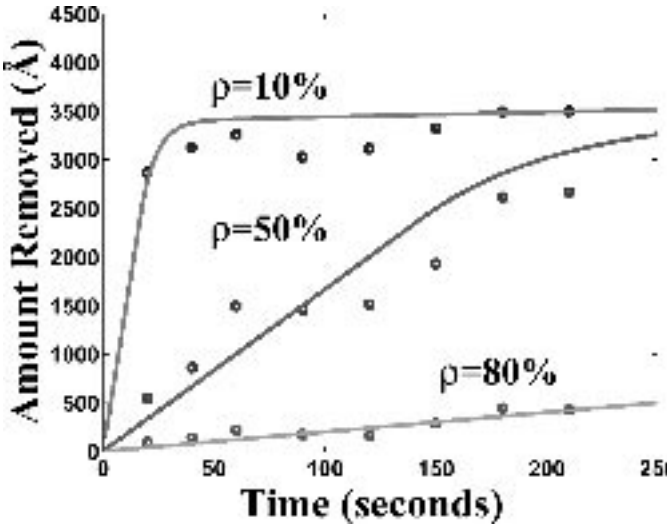


*Fig. 13: Amount of oxide removed, for different density regions, during polish with a fixed abrasive CMP pad. Circles are measured values; solid line is the model fit.*

## Labnet Software

### Personnel
T. Lohman, J. F. Cen (D. Boning, D. Troxel)

### Sponsorship
Dell

University microfabrication laboratories are facing many new challenges and opportunities: facilities are becoming more expensive and difficult to manage; resources and expertise need be shared and made available to a wider community; education and research are becoming more dependent on multi-institutional collaboration. Given the above challenges, there is a growing need for a new distributed information infrastructure to enable remote collaboration, access to remote sites' data and sharing of end-user software applications, in the face of differences between remote sites in computer platforms, operating systems, and technical resources. Past research has been done within this application domain but most working systems are too tightly coupled to their local facilities, suffer from portability problems and have never addressed the issue of data distribution and remote site interaction.

The Labnet Software Project was initiated in recognition of a need for universities to share the development and support effort required to develop and maintain new distributed laboratory information systems. With leadership by Stanford University, three schools – MIT, UC Berkeley, and Stanford – are working to specify and implement the new web-based Labnet Software information system. Key elements of the joint development effort are:

- Standard distributed computing interfaces, including the Object Management Group's (OMG) Common Object Request Broker Architecture (CORBA), OMG's Interface Definition Language (IDL), Sun Microsystem's Java language, and modern relational and object databases.

- Laboratory support software modules that run via a web interface, enabling distributed and remote access to laboratory information.

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- Focused development of critical support functions: equipment reservation, equipment interlock and management, and accounting data collection modules are the initial focus.

Deployment of key modules is expected to take place within the Stanford, MIT, and UC Berkeley microfabrication laboratories. The Labnet Software will also be made available to other laboratories in order to help support the university community's need for portable, distributed, and collaborative laboratory information system support.

*Opposit Page:*

*Perspective (a) and top (b) views of a suspended silicon membrane on an SOI wafer made using MEMS selective etching techniques. The membrane is held at its four corners, and deep trenches are etched along the sides. so the growth on the membrane will be free from the deposition on the edges.*
*Courtesy: K. H. Choy (C. G. Fonstad, Jr.).*
*Research sponsored by 3-D IC, Inc.*