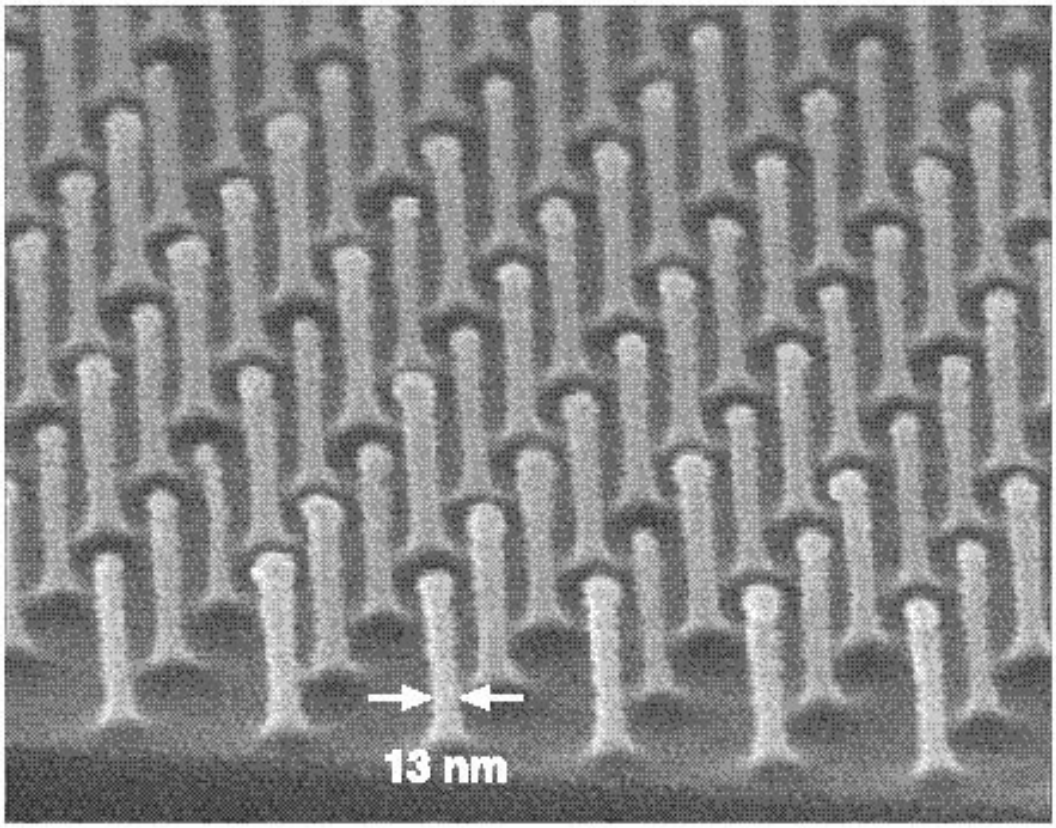
Opposite Page:

Scanning electron micrograph of a 100 nm-period grid, exposed in PMMA on top of an antireflection coating, and transferred into Si by reactive ion etching.
Courtesy: J. M. Carter, M. Farhoud, R. C. Fleming, T. A. Savas, and M. Walsh (M. L. Schattenburg and H. I. Smith)
Research sponsored by AFOSR and U.S. ARO

Fabrication Technology



100nm-period posts in Si

Fabrication Technology

- *Nanometer-level Feedback-Stabilized Interferometric Aligning and Gapping X-ray Exposure System*
- *Deep-Ultraviolet Contact Photolithography*
- *Scanning-Electron-Beam Lithography*
- *Spatial-Phase-Locked Electron-Beam Lithography*
- *Sub-100 nm Metrology Using Interferometrically Produced Fiducial Grids*
- *X-Ray Nanolithography*
- *Zone-Plate-Array Lithography (ZPAL)*
- *Improved Mask Technology for X-Ray Lithography*
- *Interference Lithography*
- *Alternative Chemistries for Wafer Patterning*
- *Development of Fabrication Techniques for Building Integrated-Optical Grating-Based Filters*
- *Double-Sided Interconnect Technology for 3-D Integration*
- *Three-dimensional Integration of GaAs and Si Circuitry using Silicon-on-Gallium Arsenide Techniques*
- *Fabrication and Characterization of Er2O3 Thin Films*
- *Diffusion and Activation of N-type Dopants in Silicon Germanium Alloys*
- *Magnetically-Assisted Self Assembly - a New Heterogeneous Integration Technique*
- *Selective Self-Organization of Colloidal Particles Silicon Field Emitters with Integrated Focusing Electrode (IFE-FEA's)*
- *Silicon Field Emitter Array Fabrication and Characterization*
- *Field Emission from Thin Films*

Nanometer-level Feedback-Stabilized Interferometric Aligning and Gapping X-ray Exposure System

Personnel

E. E. Moon and P. N. Everett
(H. I. Smith)

Sponsorship

Naval Air System Command and SAL Incorporated

An experimental high-precision, X-ray exposure system has been constructed that employs Interferometric Broad-Band Imaging (IBBI) for alignment (Fig. 1(a)). The IBBI scheme utilizes grating and checkerboard type alignment marks on mask and substrate, respectively, which are viewed through the mask from outside the X-ray beam at a Littrow angle of 20 degrees with f/10 optics and a 110 mm working distance (Fig. 1(b)). Each mark consists of two gratings (or checkerboards) of slightly different periods, p_1 and p_2, arranged so that p_1 is superimposed over p_2, and p_2 over p_1 during alignment. Alignment is measured from two identical sets of moiré fringes, imaged onto a CCD, that move in opposite directions as the mask is moved relative to the substrate. Alignment is determined from the relative spatial phase of the two fringe sets, measured with a high-sensitivity frequency-domain algorithm.
When a point X-ray source is employed, image placement errors can be significantly larger than the feature

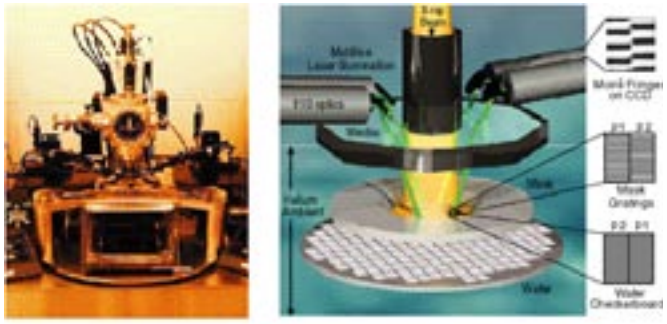


Fig. 1: (a) X-ray exposure and alignment system. Mask and wafer are located in a helium ambient and exposed to X-rays. (b) Schematic of IBBI scheme which enables an alignment beam to enter at a 20 deg. angle through a viewport before and during exposure. Fringes result from interference between mask gratings and wafer checkerboards of similar periods. The fringes are imaged onto a CCD camera and analyzed in the frequency domain. The relative mask-wafer position is controlled by piezos with integral capacitive sensors.

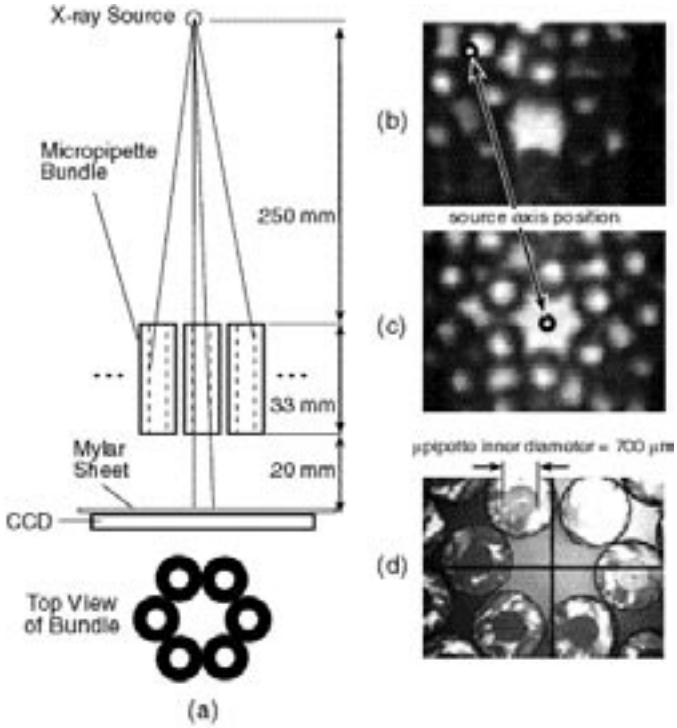


Fig. 2: (a) Schematic of point source alignment apparatus. Divergent X-rays are radially obscured by the micropipette bundle and observed with an X-ray-sensitive CCD camera. (b) Image from the CCD with the perpendicular to the source misaligned and (c) aligned to the center of the micropipette bundle. (d) Image of the micropipette bundle with a normal-incidence optical microscope illuminated with white light and the center denoted with crosshairs. A point on an X-ray mask is aligned to the crosshairs to complete the mask-source alignment.

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dimension if the position of the source is unknown. Specifically, the requirements for nanometer overlay are: (1) the gap must be known and controlled to < 0.1 μm and (2) the source axis (i.e., the perpendicular from the source to the mask) must be known to about 100 μm.

The gap can be determined and controlled with a previously described Transverse Chirp Gapping (TCG) scheme, which permits interferometric sensitivity to gap using a single mark on the mask. The gap information is encoded into the spatial phase of a pair of fringes, which are observed with the same microscope as IBBI fringes.

A straightforward means of determining the source axis is to directly observe the X-rays from the point source passing through an array of circularly symmetric, tubular absorbers. As shown in Fig. 2(a), the source axis detection apparatus consists of an X-ray-sensitive CCD camera and a close-packed bundle of micropipettes (inner diameter=700 μm, length=33 mm). The divergence of the X-ray point source results in obscuration of the X-ray flux by the micropipettes, in proportion to the distance away from the system axis. This radially-dependent obscuration yields a pattern detected by the CCD, shown in Fig. 2(b), in which the source axis intercepts the image in its upper left corner. In the source alignment procedure: (1) the micropipette bundle is translated to the point of maximum pattern symmetry (Fig. 2(c)), (2) the center of the bundle is observed with an optical microscope and denoted with crosshairs (Fig. 2(d)), and (3) a point on the X-ray mask, observed with the microscope, is aligned to the crosshairs. This scheme enables alignment of the mask to the source axis within 100 μm, corresponding to overlay runout <1 nm (using a 3 μm gap and a source-mask separation of 250 mm.).
Prior to finding the source axis, the axis of the micropipette bundle is adjusted such that it is parallel to the wafer normal. For this purpose a 3x normal-incidence

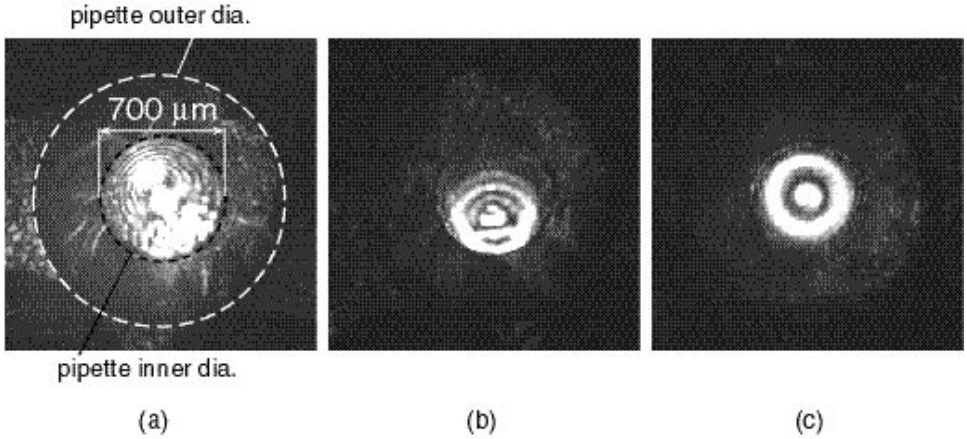

Fig. 3: Images of laser light retroreflected from a wafer passing through a micropipette adjusted to three different angles: (a) misaligned with wafer normal, (b) approaching wafer normal, and (c) aligned with wafer normal (within a few microradians), as indicated by a single optical mode within the micropipette.

Continued

microscope images a laser beam which passes through one of the micropipettes, retroreflects from a surface parallel to the CCD camera and the wafer, and returns through the micropipette. The micropipette angles are adjusted (Figure 3(a), (b)) until a single optical mode is observed within the micropipette (Figure 3(c)), indicating alignment of the micropipette to the wafer normal within a few microradians.

Conventional metrological methods are inadequate for measuring the overlay accuracy of IBBI. For this purpose we employ the Moiré fringes formed by the superposition of the exposed resist pattern (250 nm thick) on top of the IBBI alignment mark (etched 200 nm into the wafer). The relative spatial phase of these fringes is examined with a normal incidence optical microscope and analyzed with the IBBI algorithm.
A normal-incidence optical micrograph of such fringes is shown in Figure 4(a) and a closer view of aligned dual-gate transistors is shown in Figure 4(b). The phase analysis was performed on a Y alignment mark directly underneath the X-ray point source. The data for three sequential exposures on the same mark indicates misalignment of 2.5, -3.1 and 6.0 nm. Each exposure was performed several days apart, without realigning the source-mask axis. The variation in overlay is attributed to mechanical drift of the X-ray source position, since in each exposure the feedback system recorded a mean misalignment of <1 nm, such as in Figure 4(c). In normal operation the source axis alignment will be ascertained before each exposure.

The unique collection of capabilities of IBBI alignment, TCG gapping, and X-ray axis alignment are being employed in the fabrication of a variety of electronic and optical devices, including 25 nm effective-channel-length n-MOS transistors.

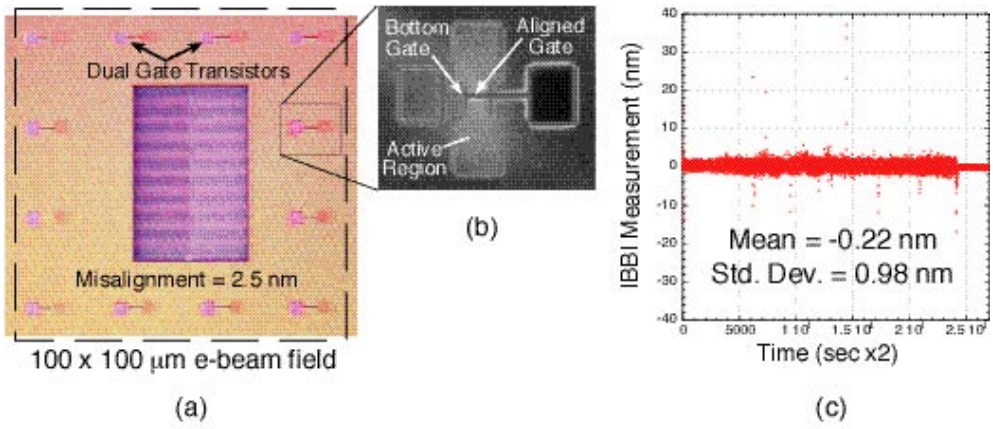

Fig. 4: (a) Optical micrograph of aligned dual-gate nMOS transistors and fringes printed in resist. Top and bottom gates as well as the IBBI mark were written within a single 100x100 mm e-beam field. (b) Optical micrograph of aligned gates. (c) Feedback data from Y IBBI microscope during exposure.

Deep-Ultraviolet Contact Photolithography

Personnel
Dr. J. G. Goodberlet, J. M. Daley, H. Kavak, and M. K. Mondol
(H. I. Smith)

Sponsorship
DARPA
Deep-ultraviolet contact photolithography, now called Conformable-Contact

Photolithography (CCP), offers low-cost replication of sub-100-nm patterns at modest printing rates. For this technique, a patterned light-absorbing mask, less than 200 μm thick, is brought into intimate contact with a resist-coated substrate and then exposed with deep ultraviolet radiation,e.g. 220-nm wavelength from an arc lamp in our experiments. Because the mask is thin, intimate contact can be achieved over the entire substrate. In this manner, the substrate can be patterned with a single exposure, without the use of expensive relaying optics or laser radiation.

Multilevel alignment was demonstrated on a custom contact nano-aligner. The mask size was increased from one-inch diameter to three inches, and high-speed photoresists were used to reduce exposure times. Additionally, a numerical simulation of in-plane pattern displacements resulting from printing on spherical surfaces was completed.

Figure 5 shows the contact nano-aligner designed for conformable-contact photolithography. The aligner handles three-inch-diameter masks and wafers, and has nanometer-precision positioning actuators for X, Y, θ movement of the wafer. It also has electronic sensors and differential micrometers to adjust mask-to-wafer parallelism. A dual-field optical microscope is used to view fine alignment marks on the mask and wafer, while bringing the mask into intimate contact with the wafer. After alignment and contact are made, the assembly is moved under an exposure lamp. This contact nano-aligner has been used recently in two multi-level alignment experiments. These are the first of a series of multi-level patterning experiments that will be used to evaluate overlay accuracy in CCP.
The best result from the first two multi-level alignment trials is summarized in Figure 6. This vector graph represents overlay errors at different locations on the printed wafer. The length of the arrow corresponds to the magnitude of the displacement, i.e. compare with the 1 μm scale marker. For a 40mm x 40mm patterned area, the mean alignment error was below 175 nm, and the standard deviation was less than 150 nm. For a quarter of the area, enclosed by the dashed box, the mean alignment error reduced to about 50 nm. Much of the overlay error is attributed to the mask holder and intimate-contact process. The errors are expected to reduce with further modifications to the aligner.
To increase the patterning rate for CCP, several resists were investigated and compared to Poly (MethylMethAcralate) (PMMA), and the mask size was increased from one-inch diameter to three-inch diameter. Sub-100-nm patterning resolution was demonstrated with the larger mask and PMMA resist, although

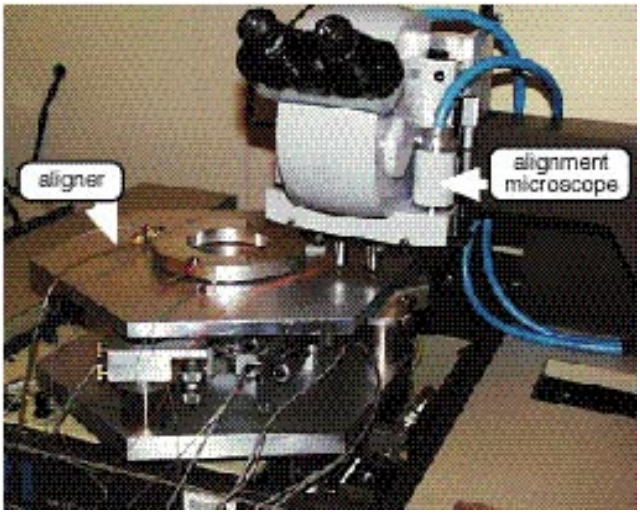

Fig. 5: The contact nano-aligner. This apparatus was designed and built to achieve sub-50-nm mask-to-substrate multi-level alignment for conformable-contact photolithography.

Continued

exposure times were several minutes for our lamp source. For high-speed photoresists such as Shipley Company's 1813, UV-5 and UV-113, the exposure time was reduced to a few seconds. However, the patterning fidelity was not as good as with the slower PMMA resist. We are currently attempting to understand and improve the patterning fidelity with these fast resists.

Conformable-contact photolithography was originally proposed as a low-cost, high-resolution method for patterning on non-conventional surfaces such as cylinders and spheres. Previously we demonstrated that CCP could be used to pattern on spheres, since the mask is thin and flexible. A numerical code was written to estimate the magnitude of in-plane pattern displacements that would result when a thin conformable mask is brought into intimate contact with a sphere. The radius of curvature of the spherical substrate was 10 mm, determined by a specific application, and the mask diameter was taken as 75mm. The estimated in-plane displacements were determined to be greater than 100 μm. This amount of displacement will likely require pattern pre-biasing and careful metrology to determine overlay accuracy of the printed pattern.

Under renewed sponsorship, this research program will be extended to evaluate overlay accuracy, and to fabricate micro devices using conformable-contact photolithography.

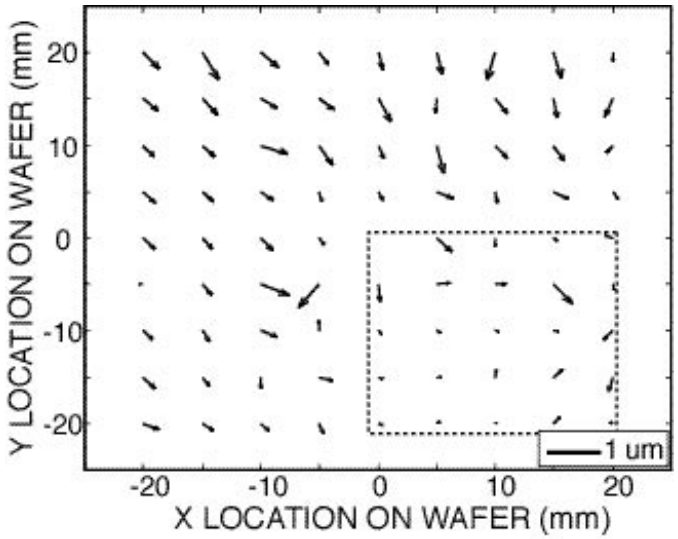

Fig. 6: Multi-level alignment results. The vectors represent the magnitude and direction of overlay errors measured after a second-level patterning step with conformable-contact photolithography. The contact nano-aligner, shown in Figure 5, was used to align the first and second levels.

Scanning-Electron-Beam Lithography

Personnel

M. K. Mondol and J. Goodberlet
(H. I. Smith)

Sponsorship

NSF, ARO, and AFOSR

Figure 7 is a photograph of the Scanning-Electron-Beam Lithography (SEBL) system (VS-2A) located in the Scanning-Electron-Beam Lithography (SEBL) facility, Room 38-165. This instrument was obtained as a donation from IBM in 1993. Its digital pattern generator is based on a commercial high-performance array processor, which uses dual RISC processors. The system is capable of creating large-area patterns composed of multiple stitched fields. Conversion software has been developed which allows a CAD data file to be fractured and translated prior to exposure by the electron-beam tool.

The VS-2A can expose substrates up to 20 cm diameter, at linewidths down to 70 nm. The goals of the SEBL facility are to: (1) provide the MIT research community with an in-house SEBL capability for writing directly on experimental device substrates; (2) advance the state-of-the-art in SEBL, particularly with regards to pattern placement accuracy and long-range spatial-phase coherence; and (3) pattern X-ray nanolithography masks for in-house use. In order to write concentric circular patterns, such as Freznel zone plates, software was developed to generate arbitrary arcs of an annulus with user-specified start and finish radii and angles.

The VS2A is heavily used in a variety of projects, both mask making and direct write. These have included: 3-D, 2-D, and 1-D photonic bandgap structures; optical-communication filters; arrays of Fresnel zone plates; electrical contacts to bismuth nanowires; high-density magnetic nanodots for information storage; distributed-feedback lasers; sub-100 nm electronic devices; dual-gate sub-100nm MOSFETs; diffractive optical elements; and magnetic random access memory devices. Masks have been made for X-ray nanolithography and intimate-contact photolithography.
VS-2A is also used extensively in experiments on spatial-phase-locked e-beam lithography, in a program aimed at achieving nanometer-level pattern placement accuracy. A new method for high-precision measurement of interfield stitching errors was also developed based on a modified moire' technique.

The scanning-electron-beam lithography facilities of the NSL has been augmented with the acquisition of a Raith Turnkey 150. This system features a beam diameter as fine as 5nm. Feature sizes down to 17nm have been achieved. The primary utilization of the Raith system will be in a program to develop Spatial-Phase-Locked E-beam Lithography (SPLEBL)

Fig. 7: Photograph of the VS-2A Scanning-Electron-Beam Lithography System (SEBL). The operator is Research Specialist Mark Mondol.

Spatial-Phase-Locked Electron-Beam Lithography

Personnel

M. A. Finlayson, J. G. Goodberlet, J. Todd Hastings, M. K. Mondol, and F. Zhang
(H. I. Smith)

Sponsorship

ARO

Spatial-Phase-Locked Electron-Beam Lithography (SPLEBL) promises to reduce pattern-placement errors in electron-beam-lithography systems to the nanometer level. Such high precision is essential for a variety of future lithographic applications. SPLEBL is currently the only approach capable of achieving such accuracy. In SPLEBL, a low-level, periodic signal, derived from the interaction of the scanning e-beam with a fiducial grid on the substrate, is used to continuously track the position of the e-beam while patterns are being written. Any deviation of the beam from its intended location on the substrate is sensed, and corrections are fed back to the beam-control electronics to cancel errors in the beam's position. In this manner, the locations of patterns are directly registered to the fiducial grid on the substrate.

Considerable effort has been devoted to the installation and testing of a Raith-150 Electron-Beam Lithography (EBL) system, a new tool which provides sub-20-nm patterning resolution. A systematic study of fluorescent polymers has been carried out to identify suitable polymers for patterning a scintillating fiducial grid. Also, a bench-top electron-beam test column has been operated with electrostatic lenses, and is undergoing further modifications for the installation of a high-speed electron-beam dose modulator.

Figure 8 shows a Raith-150 EBL system, a sub-20-nm-resolution, nanometer-placement-accuracy tool which was purchased for the SPLEBL research. This system has been used to pattern 18-nm holes, 17-nm gates, and 42-nm-pitch gratings. After installation at MIT, the field-stitching accuracy and pattern overlay accuracy were measured to be 21 nm and 27 nm respectively, where both values are mean plus 2s . Subsequent experiments have been carried out to measure the tool's intrafield distortion, and initial results indicated systematic distortion, about 20 nm in magnitude, near two field boundaries. We are currently evaluating methods to eliminate this distortion. Software for the sparse-sampling mode of SPLEBL (details reported last year) has been transferred to the Raith system. This software will be tested on the system once a sensitive photodetection system is installed in the tool's vacuum chamber. The photodetector consists of an optical light-collection assembly and an external photomultiplier tube. This will be used to detect a faint optical signal from the scintillating fiducial grid. With SPLEBL, the patterning accuracy and resolution of the Raith tool will be unmatched.

Significant work has also been carried out to improve the quality of the scintillating fiducial grid. Drawing on the extensive literature concerning scintillating detectors used in particle physics, and through our collaboration with Professor Swager of the Chemistry Department, we have identified and tested over thirty different scintillating systems. The best of these with regard to brightness, process compatibility, high contrast patternability (quenchability) via UV interference

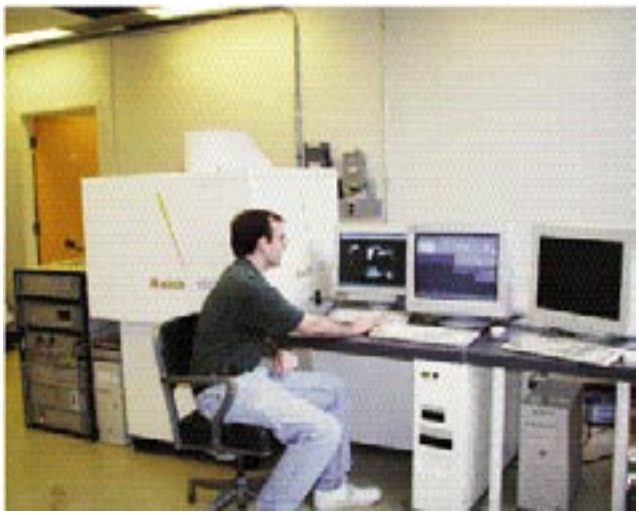

Fig. 8: The Raith-150 electron-beam lithography system. This tool provides sub-20-nm patterning resolution, and will be used to demonstrate nanometer pattern-placement accuracy via spatial phase locking.

Continued

lithography, and resistance to damage by the electron beam, have been retained for further testing and modification. In general the systems contain a methyl or dimethyl styrene polymer as the base, along with a strong scintillator (anthracene with naphthalene, or p-terphenyl) for the primary emission source, and an efficient secondary scintillator (POPOP) to act as a wavelength shifter to match to the SPLEBL detector. An example system, along with the energy pathway, is illustrated in Figure 9. The scintillator and polymer are dissolved in chlorobenzene and spun onto the wafer, and patterned with UV interference lithography. Future scintillation work will investigate the use of additives and additional bleaching layers to improve the scintillator's UV-quenching contrast.

Initial electron-emission tests were carried out in the bench-top electron-beam column. A tungsten filament was used as the electron source, and an electrostatic lens was incorporated into the column. The electron beam was colimated with the electrostatic lens and two beam-line apertures. The e-beam was viewed on a phosphor screen, and the current was measured to be over 100 nA at maximum voltage settings. The acceleration voltage used was 5 kV. After introducing the quadra-deflector plates into the beam line, the e-beam was severely perturbed. This was due to charging of insulators supporting the deflectors. The deflector is currently being modified, and a numerical simulation is being developed to trace the electron paths through the deflection apparatus. The simulation will provide information about beam-shape distortions, deflection magnitude, and chromatic abberations introduced by the deflection apparatus.
In the next phase of this program, the sparse-sampling SPLEBL algorithm will be fully integrated into the Raith-150 system, and tested using our most recently developed scintillating polymer and photomultiplier detector. We expect pattern-placement errors to be reduced to less than 5 nm, mean plus sigma, in this demonstration of SPLEBL. We will also begin to investigate real-time modes of SPLEBL on the Raith system.

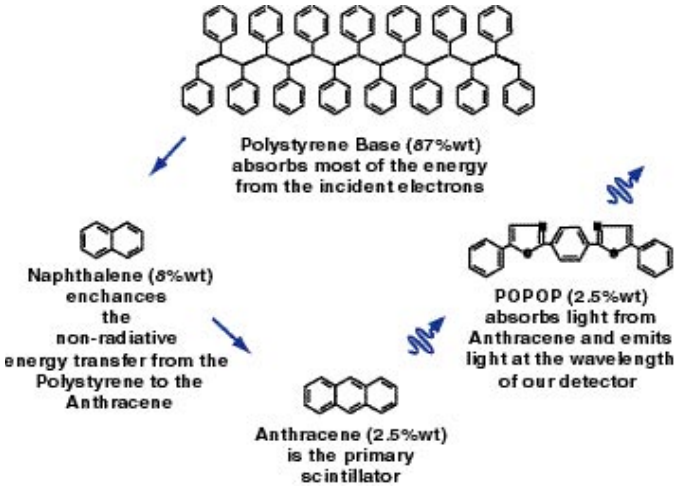

Fig. 9: Example scintillating system with polystyrene as the base, anthracene as the primary scintillator, and POPOP as the wavelength shifter. Naphthalene is an energy-transfer-enhancing additive. The polystyrene absorbs most of the energy from the incident electrons, and the energy is passed along as indicated.

Sub-100 nm Metrology Using Interferometrically Produced Fiducial Grids

Personnel

C. Chen, P. Konkola, and R. Heilmann
(M. L. Schattenburg and H. I. Smith)

Sponsorship

DARPA / ARO

The ability to see and measure the results of a process is critical to advancing fabrication technology.

Historically, the development of improved microscopy techniques led to rapid progress in microfabrication. Thus, the scanning-electron microscope was essential to the microelectronics revolution. Similarly, the scanning-tunnelling microscope is creating a revolution in the study of interfaces and nanostructures.

In the past, metrology of microstructures and the measurement of workpiece distortion (e.g., a photolithographic reticle or X-ray mask) has been based on point-by-point measurement through an optical microscope using an X-Y table monitored by a laser interferometer. Although this approach enables relative distances in a plane to be measured with 1 nm-level detectivity, it is expensive, tedious, and subject to a number of shortcomings, including the necessity of placing rather perturbative marks on a workpiece. We have initiated a new approach to metrology for the sub-100 nm domain that is based on large-area fiducial grids produced by interference lithography. This new approach is complementary to the point-by-point approach in much the same way that aerial photogrammetry is complementary to ground-based land surveying for the mapping of terrain.

A key element in this new initiative is the Holographic-Phase-Shifting Interferometer (HPSI), illustrated in Figure 10. This system, once it is fully developed, will enable us to measure in a global manner the in-plane distortion of a workpiece, provided one of its surfaces contains a shallow fiducial grid. Ideally, the grid on the workpiece will be created by interference lithography or a derivative thereof, such as near-field holography.

The Semiconductor Industry Association (SIA) Roadmap calls for minimum features to shrink below 35 nm over the next 15 years, implying that planar metrology tools with errors below 1.0 nm will be required in the next decade (see Figure 11). We propose that interferometrically patterned grids are nearly ideal vehicles to this end. As part of this new initiative in sub-100 nm metrology, we are pursuing a variety of approaches to eliminate the distortion in interferometrically produced grids, decreasing the coefficient of the hyperbolic phase progression (a consequence of creating a grid by interfering spherical wavefronts), and increasing the useful area of fiducial grids.

One such approach is Scanning-Beam-Interference Lithography (SBIL), depicted schematically in Figure 12. The concept here is to combine the sub-1 nm dis-

Fig. 10: Schematic of the Holographic Phase-Shifting Interferometer (HPSI). A spherical wave back-diffracted from a shallow substrate grid, and a second wave specularly reflected, interfere on a fluorescent screen at the spatial filter. The fringes are imaged onto a CCD. By shifting the beam splitter with a piezo, a computer generates an X-Y map of phase error.

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placement measuring capability of laser interferometry with the interference of narrow coherent beams to produce coherent, large-area, linear gratings and grids. Our ultimate goal is to produce gratings over areas many tens of centimeters in diameter with sub-nm distortion. These would be used to calibrate lithography tools or used directly as optical encoder scales, eliminating the laser interferometer and significantly improving performance while reducing cost.

SBIL requires sophisticated environmental controls to mitigate the effects of disturbances such as acoustics, vibration, and air turbulence, and variations of temperature, pressure, and humidity. The system also features real-time measurement and control of image phase using heterodyne fringe detection, acousto-optic modulator phase locking (see Figure 13), and a high-speed Digital Signal Processor (DSP) controller (see Figure 14).

Fig. 12: Schematic of the Scanning Beam Interference Lithography (SBIL) system. A pair of narrow, distortion-free beams overlap and interfere at the substrate, producing a small grating "image." The substrate is moved under the beams, writing a large area grating. Tightly overlapped scans ensure a uniform dose.

Fig. 11: Semiconductor Industry Association (SIA) roadmap tracking Critical Dimension (CD) or minimum feature size, overlay error, mask image placement error, and metrology tool error. The MIT effort seeks to produce grating metrology standards with sub-nm errors, which would be used as planar metrology length scales or optical encoders in lithographic equipment, eliminating the laser interferometer.

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Fig. 13: Schematic of SBIL Acousto-Optic (AO) modulator phase locking system. The phase of the grating image is measured by the small inner interferometer close to the writing surface. This information is processed by a digital signal processor and used to control RF frequency synthesizers which drive the AO modulators, thus locking the image phase to the moving substrate.

Fig. 14: Schematic of SBIL system architecture. The system utilizes a frequency stabilized HeNe laser l=632 nm) and heterodyne interferometry to measure substrate position, and argon ion (l=351.1) heterodyne interferometry to measure image fringe phase. Phase error signals are processed by an IXTHOS 4x167 MHz DSP board, which then drives the stage DC motors and the RF frequency synthesizer that controls the fringe-locking AO modulators.

X-Ray Nanolithography

Personnel

J. M. Daley, M. H. Lim, and E. E. Moon
(H. I. Smith)

Sponsorship

DARPA/U.S. Navy – Naval Air Systems Command

For several years, we have been developing the tools and methods of X-ray nanolithography. We have explored the theoretical and practical limitations, and endeavored to make its various components (*e.g.* mask-making, resists, electroplating, sources, alignment, etc.) reliable and "user-friendly." Because of the critical importance of X-ray mask technology, we discuss this in a separate section.

Our sources for X-ray nanolithography are simple, low-cost electron-bombardment targets. We utilize the L line of copper at $\lambda = 1.32$ nm. The sources are separated by a 1.5 μm-thick SiN_x vacuum window from a helium-filled exposure chamber. In the future, we hope to replace the Cu_L sources with a higher-flux plasma-focus source.

In earlier research, we showed that for wavelengths longer than 0.8 nm, the important limit on resolution is diffraction in the gap between mask and substrate. With a Cu_L source, a 50 nm feature must be exposed at a mask-to-substrate gap of less than about 4 μm in order to maintain good process latitude. A 25 nm feature would require a gap of 1 μm. For very small features, we eliminate the gap and use contact between the substrate and the flexible membrane mask. This technique has enabled us to replicate features as small as 20 nm in a practical, reproducible way. Figure 15 shows scanning electron micrographs of device patterns with feature sizes less than 40 nm.

To create the X-ray masks, the pattern is first written by electron-beam lithography onto an X-ray "mother" mask, using either one of our two in-house e-beam system. The e-beam written pattern is developed, and gold is electroplated into the resist mold. A negative replica, or "daughter" mask is created by exposing with the mother mask using soft-contact X-ray nanolithography. Finally, the daughter mask is exposed onto the device substrate.

We have investigated process latitude at these extremely fine feature sizes. Figure 16 shows how developed

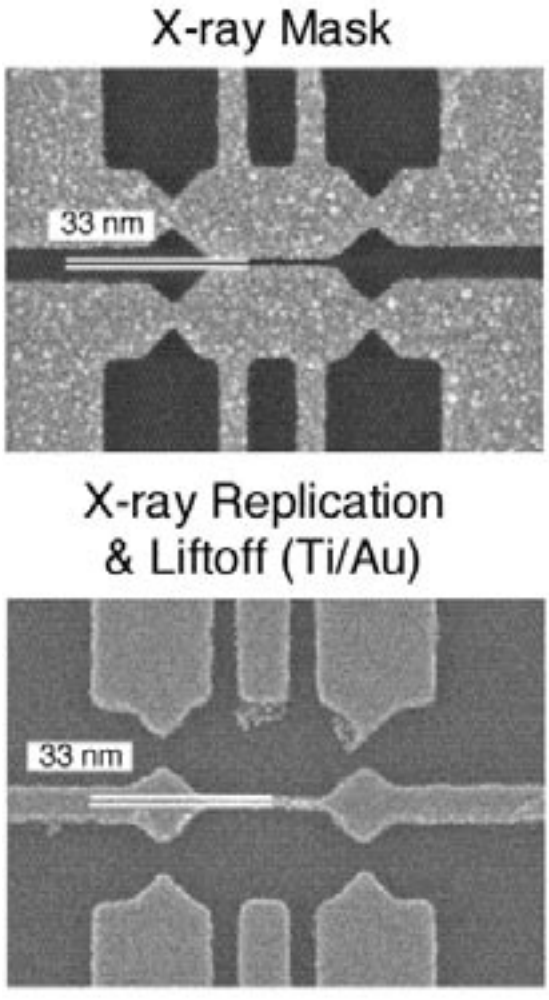

Fig. 15: Scanning electron micrographs of device patterns with feature sizes less than 40 nm achieved by X-ray nanolithography followed by liftoff. The X-ray mask is shown on top and the lifted-off pattern is on the bottom.

Continued

linewidth changes for up to 50% overdevelopment (*i.e.* developing for 50% longer than it takes for the feature to clear) as a function of linewidth. As can be seen from the plot, the measured feature on the substrate remains within a +/- 10% process window (within the accuracy of the measurement) for isolated features as small as 30 nm and for dense features (greater than 1:3 line:space ratio) as small as 45 nm. This data indicates that soft-contact X-ray lithography is extremely robust and offers very wide process latitude.

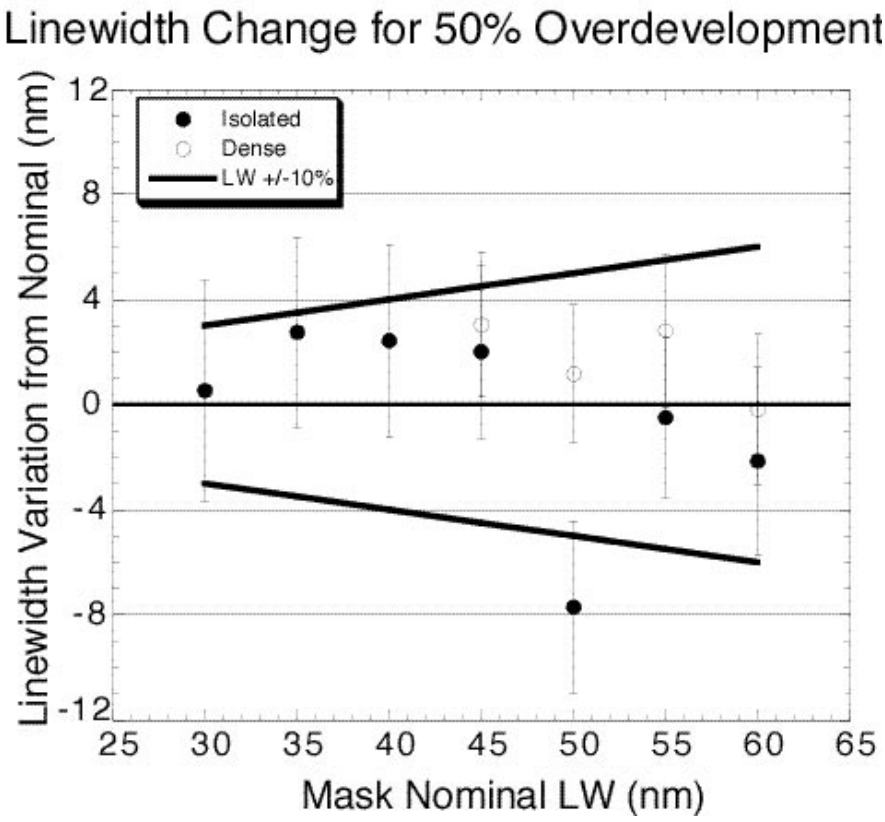

Fig. 16: Plot of linewidth variation from nominal (i.e. developed for the time required to clear features) for up to 50% overdevelopment. Isolated features stay within a +/-10% process window for features as small as 30 nm. Dense (line:space ratio of 1:3 or greater) features remain in the process window for features as small as 45 nm.

Zone-Plate-Array Lithography (ZPAL)

Personnel

each focusing a beam of light onto the substrate. A computer-controlled array of micromechanical mirrors turns the light to each lens on or off as the stage is scanned under the array, thereby printing the desired pattern in a dot-matrix fashion. No mask is required, enabling designers to rapidly change circuit designs. A schematic of

ZPAL is shown in Figure 17.

ZPAL leverages advances in nanofabrication, micromechanics, laser-controlled stages, and high-speed, low-cost computation to create a new form of lithography. We are developing ZPAL at UV, Deep UV (DUV), EUV and X-ray wavelengths. Our experimental UV ZPAL system is currently operated at a wavelength of 442 nm. The system presently prints with an array of zone plates, fabricated at MIT, in conjunction with a micromirror array made by Texas Instruments.

Lithography Results
Figure 18 shows an array of nine pattern exposed in parallel with this system. Figure 19 shows a closer view of a nested L pattern. The image quality is very good, showing dense 350 nm lines and spaces. Future research will push to shorter wavelength and therefore finer feature size. For a DUV ZPAL system operating at λ=157 nm, we expect to be able to produce 90 nm feature sizes.

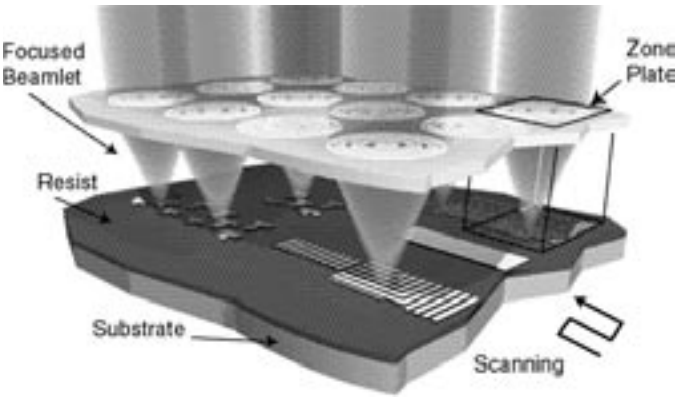

Fig. 17: Schematic of Zone-Plate-Array Lithography (ZPAL). An array of Fresnel zone plates focuses radiation beamlets onto a substrate. The individual beamlets are turned on and off by upstream micromechanics as the substrate is scanned under the array. In this way, patterns of arbitrary geometry can be created in a dot-matrix fashion. The minimum linewidth is equal to the minimum width of the outermost zone of the zone plates

For most applications of lithography, it is desirable to control the linewidth to a fraction of the minimum feature size. Figure 20 shows how this is done with gray-scaling in ZPAL exposures. In this case, 330 nm-wide pixels were exposed on a 110 nm grid. In the left-most micrograph, a single column of pixels was exposed. To widen the line, a second column was exposed at increasing doses Then a third column was exposed (as shown in subsequent micrographs).

Because zone plates are diffractive optical elements, ZPAL can operate at EUV wavelengths (13.4 nm) or even in the soft X-ray regime (λ~1-5 nm). EUV or soft X-ray ZPAL should enable us to achieve feature sizes of about 20 nanometers at relatively low cost. We are developing a soft X-ray ZPAL system (λ=4.5 nm) to demonstrate the extendibility of ZPAL. Figure 21 shows a simulated pattern produced with such a system.

Microscopy Results
An array of zone plates can also be used as a massively parallel confocal microscope, allowing imaging over a large field of view. In addition, since zone plates can be inexpensively fabricated to work at deep-UV wavelengths, low-cost, high-resolution imaging is possible with Zone-Plate-Array Scanning-confocal microscopy (ZPAM).

ZPAM is similar to conventional Scanning Confocal Microscopy (SCM), but with a few differences, as shown in Figure 22. First, the objective lens in the traditional SCM is replaced by an array of zone-plate objective lenses. Second, the detector (in this case a CCD array) is placed at the *image* plane of the zone-plate array, allowing the reflected light from each zone plate to be analyzed independently. In order to accomplish this, the confocal aperture must be somewhat larger than in conventional SCM, to pass enough dif-

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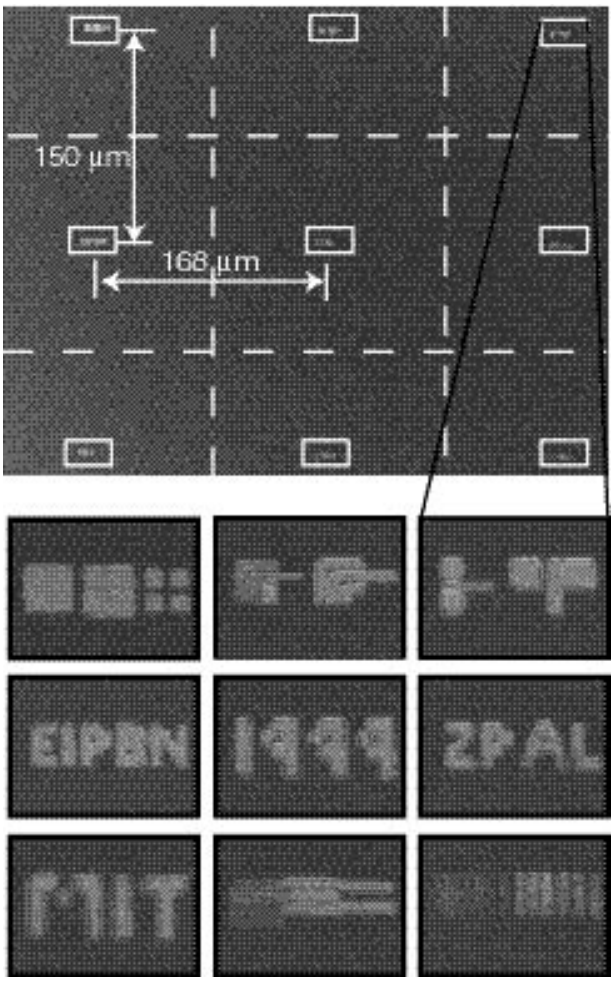

Fig. 18: Scanning-electron micrograph of nine different patterns exposed in parallel with a UV ZPAL system. A micromirror array, manufactured by Texas Instruments, was used to multiplex the laser light to each zone plate. As the wafer stage was scanned, the zone-plate illumination pattern was changed to write the patterns in a dot-matrix fashion.

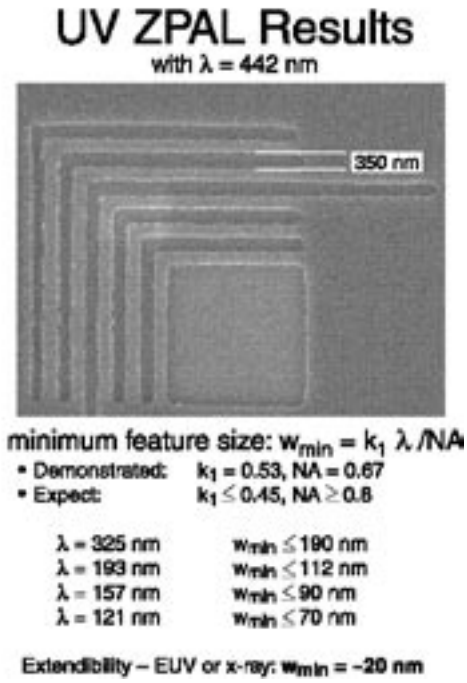

Fig. 19: Scanning-electron micrograph of nested-L patterns produced at ZPAL. The minimum feature size of an optical projection system can be described as . In this case the linewidth is 350 nm, the numerical aperture (NA) of the zone plates was 0.67, corresponding to a factor of 0.55. With modest improvements to NA and , and using DUV radiation (λ=157nm), we expect to be able to print sub-100 nm features.

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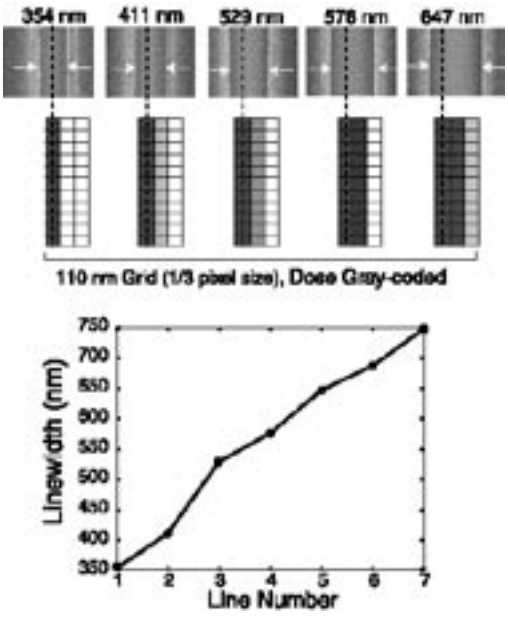

Fig. 20: Lines of varying width printed with grayscaling. Pixels (~330 nm in size) were exposed on a 110 nm grid. To widen the lines, a second column of pixels was exposed at increasing doses, then a third line was added. TOP: Scanning-electron micrographs of lines. CENTER: Schematic of exposure conditions for each line. BOTTOM: Plot of linewidth vs. line number.

Dr. D. J. D. Carter, D. Gil, and R. Menon
(H. I. Smith)

Sponsorship

DARPA and MIT Lincoln Laboratory under Air Force Contract

In semiconductor lithography, glass masks are illuminated with deep UV laser light and their image is reduced through a lens onto the substrate to define circuitry. As feature sizes are pushed toward 100 nm, lithography is becoming increasingly costly and difficult, and may soon limit the industry juggernaut.

At the MIT Nanostructures Laboratory, a considerably simpler approach is showing great promise. The new scheme, called Zone-Plate-Array Lithography (ZPAL) is made possible by inexpensive, high-speed computation and micromechanics. ZPAL replaces the "printing press" of traditional lithography with a technology more akin to that of a laser printer.

Instead of a single, massive lens, an array of hundreds of microfabricated Fresnel-zone-plate lenses is used,

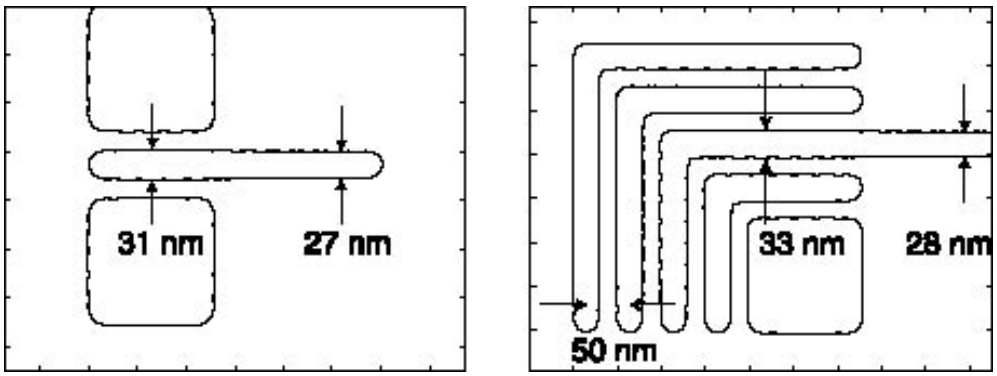

Fig. 21: Simulated patterns assuming λ=4.5 nm and an outer zone width of 25 nm. The slight proximity effect shown could be eliminated with a narrower-bandwidth source and/or by using an order-sorting aperture.

Continued

fracted orders to properly reconstruct the zone-plate array.

Figure 23 shows an image obtained with ZPAM. The sample is a silicon substrate with etched grating lines. The rough patterns in the center of the image were present in the sample. A close-up of the ZPAM image of a region of the sample is compared with a conventional optical micrograph of the same region. Note the large filed-of-view at very high (~620 nm) resolution. Higher-NA zone plates and deep-UV illumination should allow sub-100 nm resolution, while a larger zone-plate array would allow a much larger field of view. This technology can be used for level-to-level alignment and placing the substrate at proper focus in ZPAL. ZPAM may also be suitable as a stand-alone technology for mask or wafer inspection.

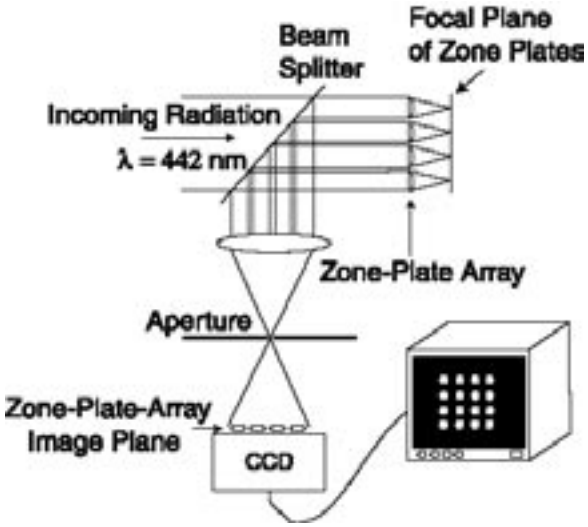

Fig. 22: Schematic of Zone-Plate-Array Scanning-confocal microscopy (ZPAM). The zone plates are used as an array of objective lenses. The CCD detector is placed at the image plane of the zone-plate array, after the confocal aperture, allowing the reflected light from each zone plate to be analyzed independently. ZPAM can be used for placing the substrate at the zone-plate focal plane and for imaging the substrate.

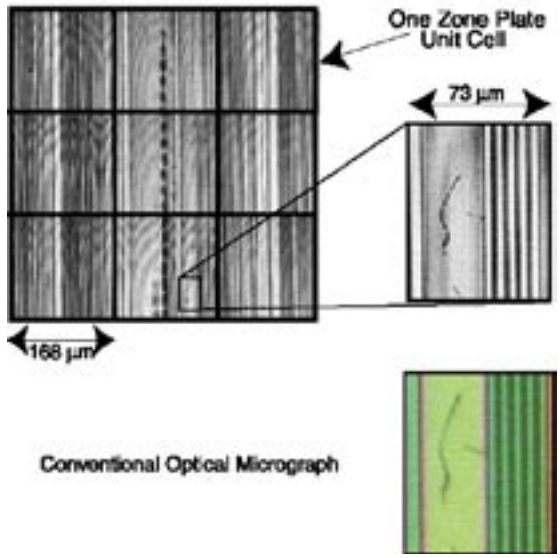

Fig. 23: Images obtained with ZPAM. Such images could be used for level-to-level lithographic alignment in ZPAL. TOP LEFT: Image of etched silicon sample. Rough patterns in center were present on the sample. Dark lines indicate zone-plate unit cells ~0.5 x 0.5 mm field-of-view, taken at ~620 nm resolution. TOP RIGHT: Close-up of ZPAM image of a scratch in the sample. BOTTOM RIGHT: Conventional optical micrograph of the same region for comparison.

Improved Mask Technology for X-Ray Lithography

Personnel

absorber patterns we electroplate gold onto the membrane, using a specially designed apparatus, after resist exposure and development. A Ti/Au plating base is deposited on the membrane prior to resist coating. To pattern periodic structures on the X-ray masks, we use Interferometric Lithography (IL),

and for patterns of arbitrary geometry we use e-beam lithography. A high-resolution Leo SEM and a Digital Instruments STM/AFM are used to inspect X-ray masks for defects. Radiation hardness for SiN_x membranes remains a problem at dose levels corresponding to production (i.e., millions of exposures). For research purposes, however, the material is entirely acceptable. Currently we are investigating the problem of X-ray mask distortion, which is a potential problem in X-ray lithography.

X-ray mask distortion is rooted in the flexibility of its membrane. The membrane responds to stress in the absorber patterns by flexing both in-plane and out-of plane. Distortion caused by this motion, especially in-plane, must be overcome if X-ray lithography is to meet the overlay requirements of future electronic and optical devices. Thus far, the X-ray lithography community has attacked this problem by trying to achieve very low-stress absorbers and, when necessary, compensating for absorber induced stress by modifying the pattern written by the electron beam. We are pursuing a new approach in which we first measure the membrane distortion and then correct it.

To measure distortion, we have developed a broadly applicable, nondestructive, global, membrane-distortion measurement technique called Holographic-Phase-Shifting Interferometry (HPSI). The HPSI system is based on the Interferometric Lithography (IL) system we use to generate large-area, highly-coherent gratings. Figure 24 is a schematic of the IL apparatus, configured as a HPSI system. The IL system splits a laser beam (λ=351nm) and forms two mutually coherent spherical waves, which interfere at the substrate at a half-angle θ. The standing wave created at the substrate surface

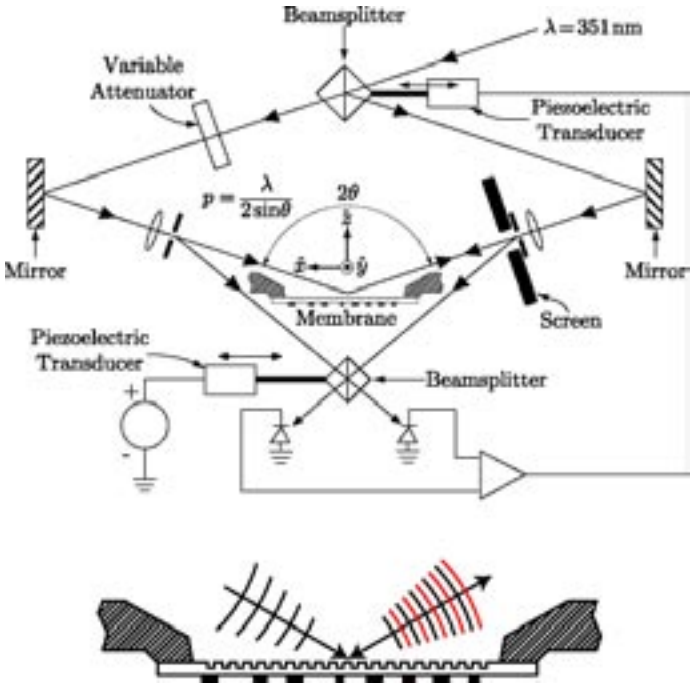

Fig. 24: A schematic of the Holographic Phase-Shifting Interferometer (HPSI) based on the interferometric lithography system that we use to generate highly-coherent gratings.

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is used to expose photoresist. After development, the grating is present on the substrate surface or can be etched into it. The IL system is used as a holographic interferometer by mounting the IL-generated grating on the substrate platform, and placing a fluorescent screen in front of one or both of the spatial filters, as depicted in Figure 24. A fringe pattern appears on the screen, which is due to the superposition of two wave fronts: one reflected from the substrate surface and the other back-diffracted from the grating. If the grating has suffered no distortion between exposure and reinsertion, the reflected and back-diffracted beams will be identical and no fringes will be observed on the screen. Any in-plane distortion of the grating will result in a fringe pattern. A CCD camera is used to capture the fringes. To increase the precision, a phase-shifting measurement is implemented, by changing the phase of one of the arms and acquiring several images, Fig. 25. In order to use this apparatus to measure the in-plane distortion, we etch shallow IL-generated gratings into the membrane.

We have developed an analytical technique that predicts both In-Plane Distortion (IPD) and Out-of-Plane

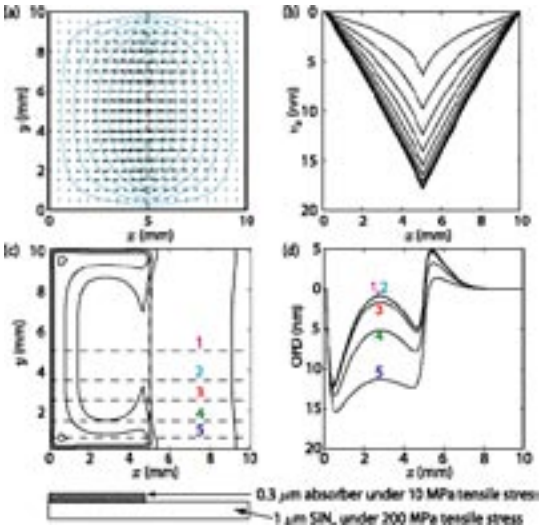

Fig. 26: Our calculational technique can solve both in-plane and out-of plane membrane distortions in 2-dimensions. For example, covering half-plane of a 10 mm square SiN_x membrane with an absorber results in both IPD and OPD displacements. (a) shows a 2-dimensional map of the IPD, which clearly indicates that a 1-D approximation would be inadequate. This is more clearly shown in (b), as the cross-sectional slices of the x component of the distortion along the x-axis vary as one moves closer to the boundary of the membrane. (c) and (d) show that the OPD also has a significant 2-D component.

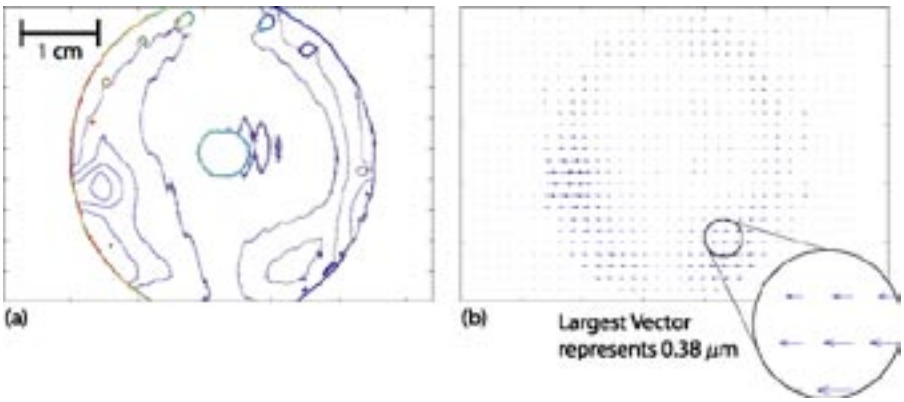

Fig. 25: The HPSI uses diffractive metrology to make a rapid, global measurement of the distortion of a membrane. (a) Contour plot of phase distortion (nonlinear component) obtained by the HPSI. Successive contours are separated by π/2 radians., (b) conversion of the phase map of (a) into a distortion map.

Continued

Continued

M. H. Lim, J. M. Daley, K.Murooka, S. Uchiyama, and M. Feldman (LSU)
(H. I. Smith)

Sponsorship

DARPA, Naval Air Systems Command, and Louisiana State University

At feature sizes of 100 nm and below the mask-to-substrate gap in X-ray lithography, *G*, must be less than ~10-μm. Thus, for nanolithography the mask membrane should be considerably flatter than 1-μm, preferably ~100-nm. Our mask technology is based on low-stress, Si-rich silicon nitride, SiN_x. This material is produced in a vertical LPCVD reactor. Membranes of SiN_x can be cleaned and processed in conventional ways. For Distortion (OPD) arising from arbitrary stress distributions in 2D. Moreover, we can also solve the inverse problem; *i.e.*, we can predict the stress distribution which, when applied to any existing distortion, eliminates it. The calculational techniques are based on the variational method. It is relatively straightforward to formulate the total energy due to membrane distortion, even for a very complicated stress distribution. We calculate the true distortion by minimizing the total membrane energy due to the placement of the stressed absorber; the total energy is straightforward to formulate for even complicated absorber distributions. Figure 27 shows the results of a calculation where half the SiN_x membrane is covered with an absorber under

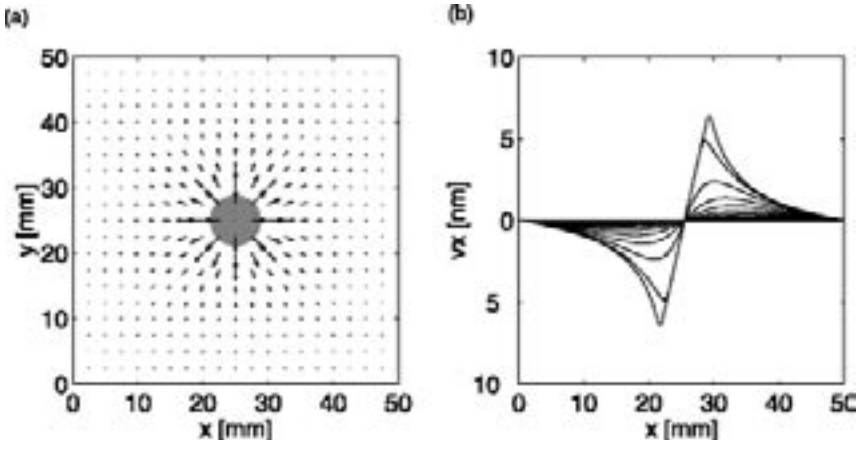

Fig 27: The calculated distortion of a 50 mm square SiN membrane, with a thickness of 1 μm, in the presence of a 7.5 mm spot with 1˚C rise in temperature. (a) The vector map showing the 2D distortion; (b) the cross-section of the x-component along the x-axis.

Continued

tensile stress.

A correcting stress distribution can be introduced by means of local heating. Figure 27 shows the analytical result of a 7.5 mm spot, with a 1˚C elevation in temperature, centered on a 50 mm square SiN_x membrane that is 1 μm thick. There is a peak displacement of 6.3 nm that occurs around the edges of the spot. This is equivalent to a circularly shaped absorber with 1.3 MPa of stress. The analysis indicates the time constant of the heating is less than one second. Moreover the calculational process also requires less than one second to complete.

Figure 28 shows a comparison of a self-consistent calculation of the distortion from a locally heated spot and the measured distortion.

We hope to build on this work by developing a system that can actively introduce a heat distribution into the X-ray mask in order to correct for membrane distortion in real-time. If successful, this should enable X-ray nanolithography to be used in applications such as integrated optics which demand the highest accuracy, precision and coherence in the placement of pattern elements.

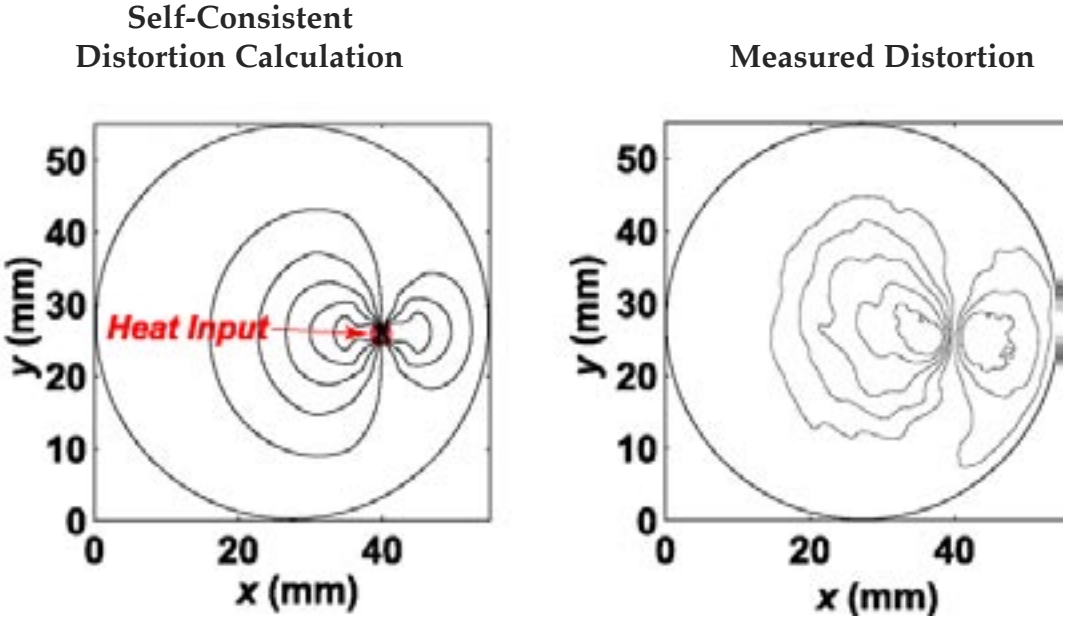

Fig. 28: A comparison of the calculated distortion and the measured distortion.

Interference Lithography

Personnel

J. M. Carter, M. Farhoud, R. C. Fleming, T. A. Savas, and M. Walsh
(M. L. Schattenburg H. I. Smith)

Sponsorship

AFOSR and U.S. ARO

Interference Lithography (IL) is the preferred method for fabricating periodic and quasi-periodic patterns that must be spatially coherent over large areas. For spatial periods down to 200 nm, an argon ion laser is used in a Mach-Zehnder configuration, with a fringe-locking feedback system, as illustrated in Figure 29. This scheme produces large area (10-cm-diameter) gratings with long-range spatial-phase coherence. Fringe locking ensures reproducibility of exposure.

In the past year, two additional tools were constructed that use the 325 nm line of a HeCd laser. One is a Lloyds-mirror interferometer designed for printing gratings or grids on substrates up to 10 cm in diameter, shown in Figure 30. The primary advantages of this system are its simplicity and the fact that the period of exposure can be varied from many microns down to ~170 nm without realignment of the optical path. Another system similar to the one shown in Figure 29 is being built with collimating lenses donated by Ultratech Corporation. This system will have the dual functions of interference lithography and Holographic Phase-Shifting Interferometry (HPSI). In the HPSI, the grating pattern formed by the interference of the two arms of the HPSI is superimposed over a pre-existing grating on the substrate. By analyzing the Moiré pattern formed between the two gratings, spatial phase distortions on the order of parts per million in the substrate grating can be accurately measured and mapped. In many applications, spatial-phase distortions even as small as ppm can be problematic. We are currently investigating innovative methods for reducing spatial-phase distortions in gratings printed using interference lithography.

The gratings and grids produced by interference lithography have found a wide range of applications. The Chandra X-ray astronomy satellite launched in August of 1999 included hundreds of matched, high-precision gratings. Other applications being pursued include: ultra-high-density magnetic information storage, alignment templates for organic crystals and co-polymers, atom-beam interferometry, and the use of interferometrically-produced grids as fiducials in spatial-phase-locked electron-beam lithography and in a new approach to metrology for the sub-100 nm domain.

For spatial periods of the order of 100 nm, a source wavelength below 200 nm must be used. Since such sources have limited temporal coherence, one is forced to employ an achromatic scheme, as shown in Figure 31. The source is an ArF laser (193 nm wavelength). A collimating lens, polarizer and scanning system are interposed between the source and the interferometer in order to achieve reasonable depth-of-focus and large exposure areas. Using this system, gratings and grids of 100 nm period (50 nm features and 50 nm spaces) are obtained in PMMA on top of an antireflection coating. Figure 32 shows a 100 nm-period grid etched into Si produced achromatic interferometric lithography and

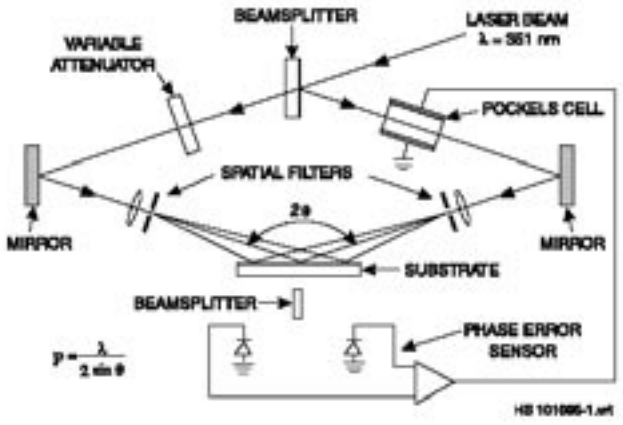

Fig. 29: Schematic of the MIT interferometric lithography system. The system occupies a 2x3m optical bench in a class 100 clean environment. The beamsplitter directs portions of the two interfering spherical beams to photodiodes. A feedback locking is achieved by differentially amplifying the photodiode signals and applying a correction to the Pockels cell which phase shifts one of the beams.

Continued

a sequence of etching steps. Grids of Si posts are being used to investigate photo-and electroluminescence which may result from charge-carrier quantum confinement.

A new generation of interference lithography tools is being developed, based on the achromatic principle in which gratings are used rather than mirrors to split and recombine beams. These new tools will produce gratings and grids of 50 nm period (25 nm lines and spaces), and will, of necessity, utilize wavelengths below 100 nm. One such achromatic interferometer will be installed on the 13 nm undulator line at the University of Wisconsin. Another will be set up here at MIT and utilize the 58 nm wavelength from a neon discharge.

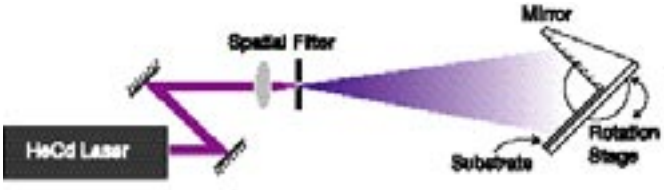

Fig. 30: Schematic of a Lloyds-mirror interferometer. The substrate and mirror are fixed at a 90˚ angle to one another, and centered in a single incident beam. The spatial-period of the exposed grating is varied by rotating the substrate/mirror assembly about its center point.

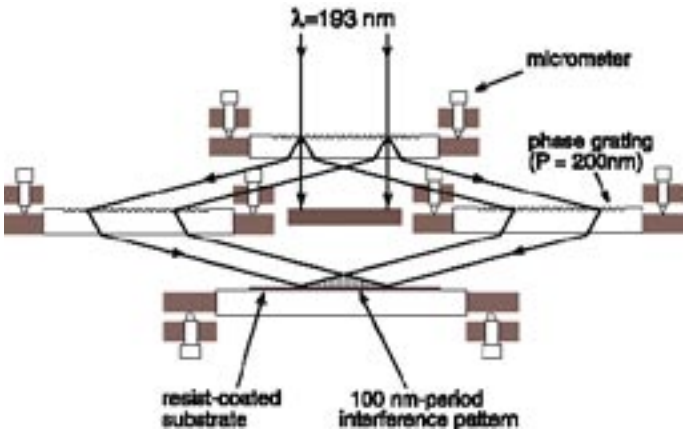

Fig. 31: Achromatic Interferometric Lithography (AIL) configuration employed to produce 100 nm-period gratings and grids.

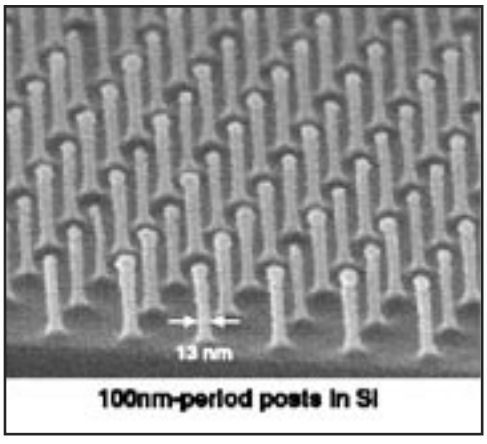

Fig. 32: Scanning electron micrograph of a 100 nm-period grid, exposed in PMMA on top of an antireflection coating, and transferred into Si by reactive ion etching.

Alternative Chemistries for Wafer Patterning

Personnel
S. Karecki, L. Pruette, and R. Chatterjee
(R. Reif)

Sponsorship
NSF/SRC Engineering Research Center (ERC) for Environmentally Benign Semiconductor Manufacturing
The goal of this project is to identify possible alternatives for perfluorocompound chemistries for wafer patterning of silicon dioxide and silicon nitride films that do not pose long term environmental problems. The etch viability of a variety of alternatives have been determined, and the most promising candidates from the etch viability study will be further tested to define an alternative wafer patterning process. The effluents are identified with Fourier Transform Infrared Spectroscopy (FTIR) and Quadrupole Mass Spectrometry (QMS) to assess their potential ESH impact. Beta testing of alternative processes are performed at the facilities of industrial collaborators.

Gases such as fully fluorinated alkanes - CF_4, C_2F_6, C_3F_8 - as well as inorganic compounds like NF_3 and SF_6, collectively termed as perfluorocompounds (PFCs), are used heavily by the semiconductor industry for the etching of dielectric films in wafer patterning applications. Their use and emission is problematic, however, from an environmental standpoint because of the global warming nature of these substances coupled with their long atmospheric lifetimes.

This report highlights recent work done in the development of etch processes with alternative chemistries, specifically NF_3/hydrocarbons and Unsaturated FluoroCarbons (UFCs). The experimental work has taken place on one of three commercially available etch reactors: a magnetically enhanced reactive ion etcher at MIT, an inductively-coupled, high density plasma etch tool at Motorola, or a dual frequency medium density

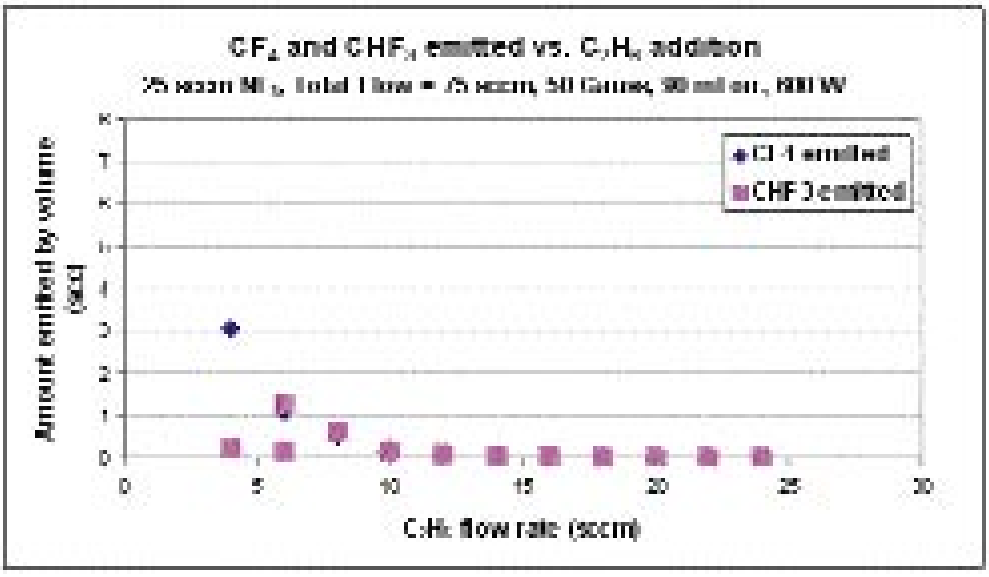

Fig. 33: PFC by-product formation as a function of ethane addition to NF_3 chemistry.

Continued

etch tool at Texas Instruments. Diagnostic tools include optical emission spectroscopy for plasma analysis and FTIR spectroscopy and QMS for effluent analysis.

Blanket oxide and photoresist etch rates along with global warming emissions have been measured and calculated for etch processes using NF_3/C_2H_2, NF_3/C_2H_4, and NF_3/C_2H_6. The C_2H_6 additive to the NF_3 etch gas demonstrated the highest ratio of blanket oxide etch rate to blanket photoresist etch rate (at 25 sccm NF_3, 16 sccm C_2H_6, 34 sccm Ar, 600 W, 50 Gauss, 90 mTorr) along with the lowest overall global warming emissions. The largest contributor to the total global warming emissions in each case was undestroyed NF_3, although the processes using C_2H_2 or C_2H_4 additives also showed evidence of CF_4 and CHF_3 formation at low additive flow rates. Even though the total global warming impact of the processes measured was not zero, it was significantly lower that the global warming impact of similar etch processes using PFC chemistries. Normalized for etch rate, a process using NF_3/C_2H_6 demonstrated a reduction in global warming emissions of over an order of magnitude when compared to a CF_4/CHF_3 process typically used on the tool. Figure 1 shows the amount of PFC by-products formed (by volume) as a function of C_2H_6 added to the process. Four hydrocarbon additive gases were tested with NF_3 in a medium density etch tool: propyne (CH_3-C≡C-H), allene (CH_2=C=CH_2), ethylene (CH_2=CH_2), and ethane (CH_3-CH_3). Process performance was assessed using cross-sectional Scanning Electron Microscopy (SEM), and specific criteria evaluated included etch rate, profile, Critical Dimension (CD) control, resist selectivity, and nitride selectivity. A process using c-C_4F_8 was used as a basis for comparison for the NF_3/hydrocarbon processes, particularly for the global warming emissions, since the process conditions represented typical ranges used with the c-C_4F_8 chemistry but were not necessarily optimized for the specific tool being used for this work. Global warming emissions, which were quantified using a Fourier Transform Infrared Spectrometer (FTIR) supplied by Air Liquide, were measured from a sampling port after the roughing pump on the tool at near atmospheric pressure in order to approximate emissions to the atmosphere as closely as possible.

Process results indicate that using NF_3 with a hydrocarbon additive chemistry with a nearly 1:1 ratio of carbon to hydrogen can offer a reasonably high etch rate with good profiles, CD control, and resist selectivity. However, there was no evidence of selectivity to silicon nitride, which is a critical requirement of most dielectric etch processes today. It is possible that nitride selectivity could be achieved with further changes to the process, but work in that area is beyond the scope of this

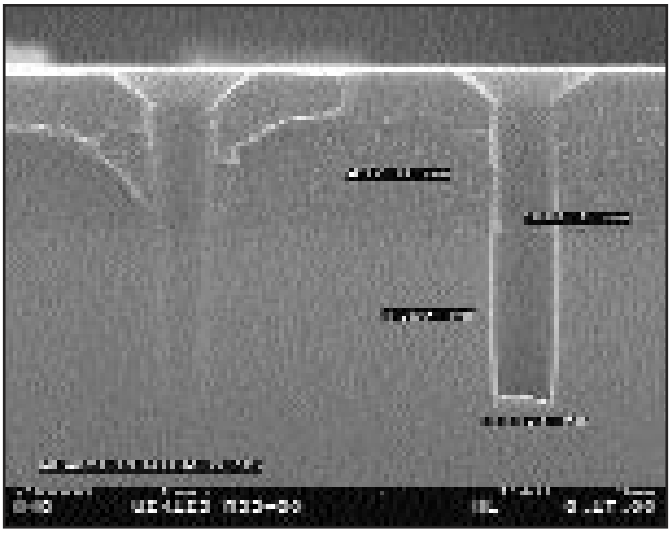

Fig. 34: Etch using hexafluoro-2-butyne: 1000 W bias power, 1680 W source power, 24 sccm etch gas flow, 75 sccm Ar flow, 6 mTorr pressure, 160 C roof temperature, 120 s etch time.

continued

report (and remains to be completed at the time of this writing). Process performance with the hydrocarbon additives with a higher amount of hydrogen relative to the carbon (ethylene and ethane) was not as promising, with lower etch rates and poor profiles, a result of the high rate of polymerization and fluorine abstraction associated with excess hydrogen in the system. Another family of alternative chemistries that has shown considerable promise in terms of process performance as well as emissions is the Unsaturated FluoroCarbons (UFCs). Previous work has shown that three isomers of C_4F_6, hexafluoro-2-butyne, hexafluoro-1,3-butadiene, and hexafluorocyclobutene, exhibit the most promise amongst the UFC chemistries. It was found that all three of the isomers of C_4F_6 were capable of etch performance comparable to a typical C_3F_8 process with a significant reduction in global warming emissions.

Figure 34 shows a profile of a via etched with hexafluoro-2-butyne. It is seen that there is very little resist erosion. In addition, a good etch rate of 5010 Å/min and no indication of etch stop are observed. The emissions for this process was 0.0539 kgCE which is a reduction of 82.9% relative to the typical C_3F_8 based process. A near complete destruction of the etch gas was observed with a destruction efficiency of 99.3%.

The quantity of each effluent emitted for this process

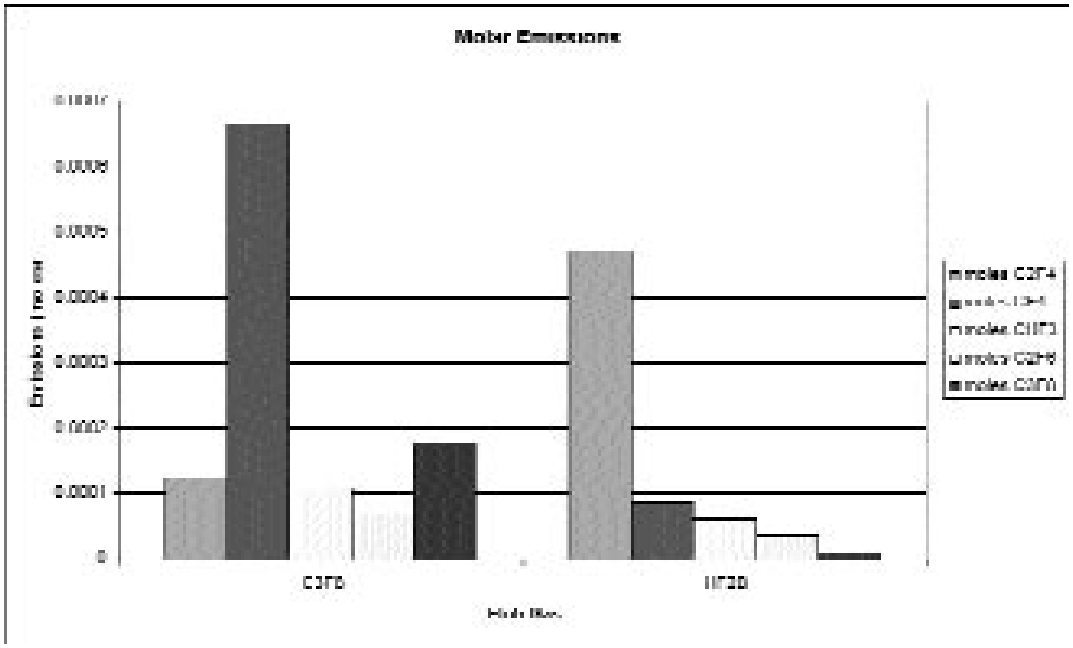

Fig. 35: Etch using hexafluoro-2-butyne: Quantity of each effluent released.

Continued

and for the typical C_3F_8 process is shown as Figure 35. It is seen that for the hexafluoro-2-butyne, much of the C is removed via the formation of C_2F_4. This was the same trend that was observed for the hexafluoro-1,3-butadiene. In comparison, the C_3F_8 based process did not emit as much C_2F_4, but removed the C via the formation of high-GWP byproducts, mainly CF_4. In addition, unlike the hexafluoro-2-butyne, there is not complete destruction of the etch gas. It is seen that the significant reduction in emissions for the C_4F_6 chemistries are due to two reasons. First, in the plasma, the C_4F_6 processes preferentially form C_2F_4 which has a low GWP rather than other high-GWP byproducts. Second, the etch gas for the three isomers are not high-GWP gases, therefore unreacted source gas is not of concern from a global warming standpoint. This is not the case for the C_3F_8, which is a high-GWP gas and exhibits incomplete destruction during the etching process.

The processes for all three isomers were very simple. The only gases that were flowed were the etch gas and the carrier gas, Ar. In previous work it was found that O_2 addition was necessary to suppress excessive polymerization. The processes shown in this work have been optimized to operate without the addition of O_2. This makes the process more robust as process control, especially for resist erosion, is very strongly dependent on the level of control of O_2 flow. Future work with these chemistries will involve examination of etch performance with low-k dielectrics, stop layer selectivity, and performance in medium density plasma systems.

Development of Fabrication Techniques for Building Integrated-Optical Grating-Based Filters

Project Staff

J. Todd Hastings, M. Jalal Khan, M. H. Lim, and T. E. Murphy
(H. Haus and H. I. Smith)

Sponsorship

AFOSR

Bragg gratings have widespread application in the rapidly growing field of optical telecommunications. A Bragg grating is formed by creating a periodic corrugation or refractive index modulation in an optical waveguide. Such a structure behaves as a wavelength-selective filter, reflecting a narrow band of wavelengths while transmitting all other wavelengths. Fiber Bragg gratings, in which a periodic index modulation is induced in the core of a photosensitive optical fiber, are now manufactured and used for a variety of applications, including dispersion compensation and wavelength add/drop filters. As optical networks spread deeper into the consumer market, it will become important to have low-cost, manufacturable Bragg grating devices that can be integrated on a chip with other electrical and optical components. The transition from fiber-optic devices to integrated-optical devices may be likened to the development of integrated circuits as a replacement for discrete components. This project seeks to develop the technology for building Bragg grating devices in planar optical waveguides.

Figure 36 illustrates the general structure of an integrated Bragg grating. Integrated Bragg gratings offer several advantages over fiber Bragg gratings. First, the integrated Bragg grating is formed by physically corrugating a waveguide, therefore it does not rely upon a photorefractive index change. This enables one to build Bragg gratings in materials that are not photorefractive (e.g. Si or InP), and allows stronger gratings to be constructed since the grating strength is not limited by the photorefractive effect. Second, integrated Bragg gratings can be made smaller, and packed closer together than fiber-optic devices. Third, the planar fabrication process gives better control over the device dimensions. For example, the beginning and end of the Bragg grating can be sharply delineated rather than continuously tapered. Abrupt phase shifts can be introduced at any point in a grating, and precise period control can be achieved. In essence, the integrated Bragg grating can be engineered on a tooth-by-tooth basis. Fourth, multiple levels of lithography can be combined, with precise nano-alignment between them, allowing the Bragg gratings to be integrated with couplers, splitters, and other electronic or photonic components. For this reason, relatively sophisticated optical filters can be constructed using integrated Bragg gratings.

Despite the flexibility afforded by Bragg gratings, their application in integrated-optical devices has been limited to relatively simple components, largely because the required fabrication techniques have not been adequately developed.

The fabrication of integrated Bragg gratings involves two lithography steps: one defines the relatively coarse

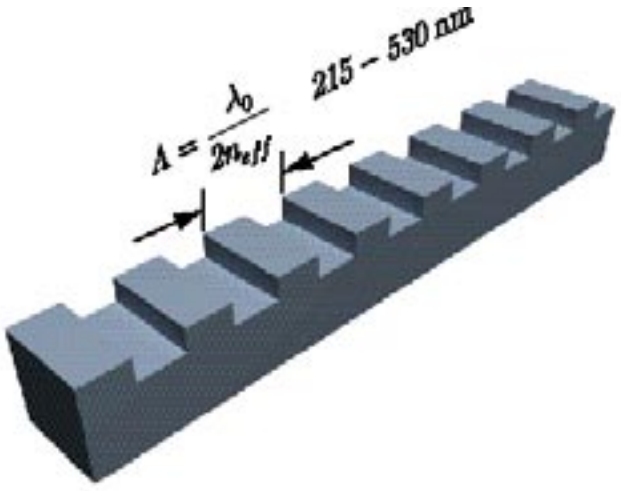

Fig. 36: Schematic of an integrated Bragg grating. A shallow corrugation is etched into the top surface of a waveguide. Depending on the index of refraction, the Bragg grating period should be between 215 nm and 540 nm.

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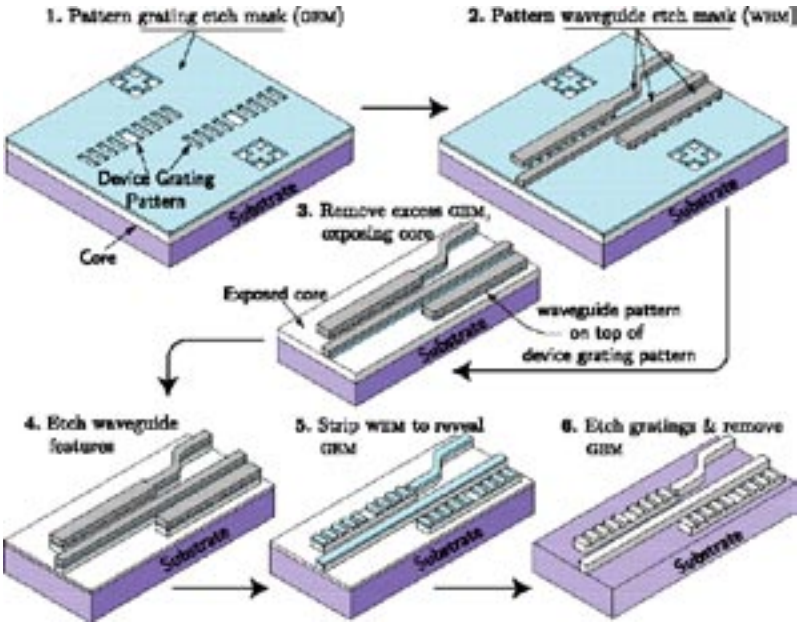

Fig. 37: Dual layer hardmask process used to pattern fine-period Bragg gratings atop relatively tall waveguide structures. The process is designed such that all lithography steps are performed over essentially planar topography.

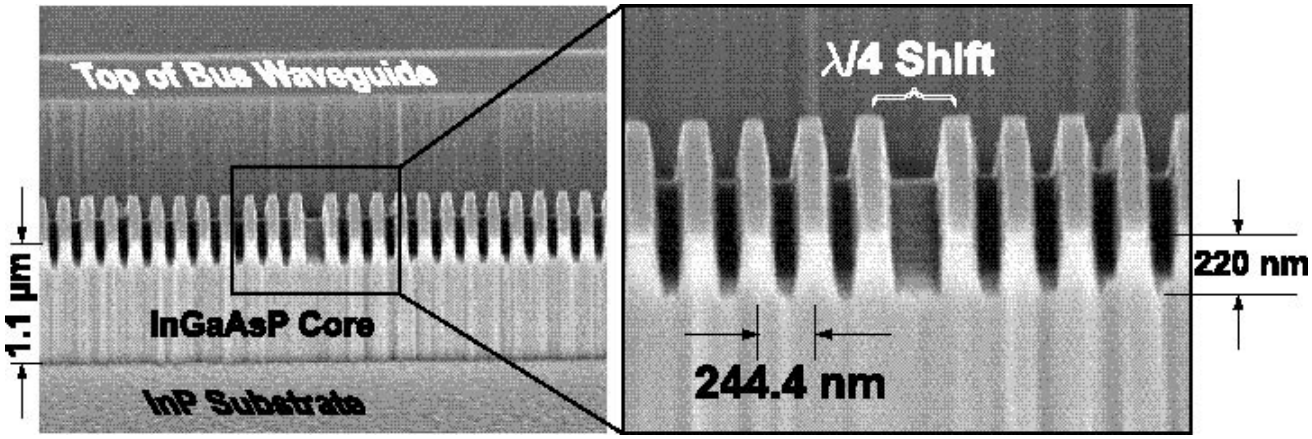

Fig. 38: Scanning electron micrograph depicting a quarter wave shifted 244.4-nm period Bragg grating etched into the top surface of an InGaAsP waveguide.

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waveguide features, and one that defines the fine-period grating features. While the waveguides can be patterned using conventional optical photolithography, high-resolution nanolithography must be used to print the Bragg gratings. Moreover, these two lithography levels must be precisely aligned relative to one another.

We use a combination of several different types of lithographies to generate the Bragg grating patterns for our devices. Interference lithography is the cornerstone of our Bragg grating work. In interference lithography, two coherent laser beams are crossed, generating a standing wave interference pattern. This standing wave pattern is used to expose photoresist, yielding a coherent deep-submicron-period grating, which serves as a fiducial reference for subsequent steps.

For devices that require long Bragg gratings with engineered phase shifts, we use a technique called Spatially-Phase-Locked E-beam Lithography (SPLEBL), which combines the long-range spatial coherence of interference lithography with the flexibility of e-beam lithography. Using an interferometrically-generated grating as a guide, we are able to write long grating patterns with our e-beam tool, avoiding the inter-field stitching errors which would otherwise spoil the device.

In order to allow precise alignment between the gratings and the waveguides, we have developed a technique of adding alignment marks to interferometrically-generated patterns. In this technique, we use our e-beam lithography system to place alignment marks on an interferometrically-generated pattern. Before writing the alignment marks, the e-beam system samples the existing grating in order to ensure that the marks are precisely aligned to the submicron gratings.
In most cases, the techniques mentioned above are not applied directly to a device, but instead to an X-ray mask. Once the mask is generated, with the appropriate gratings and alignment marks, the patterns can be

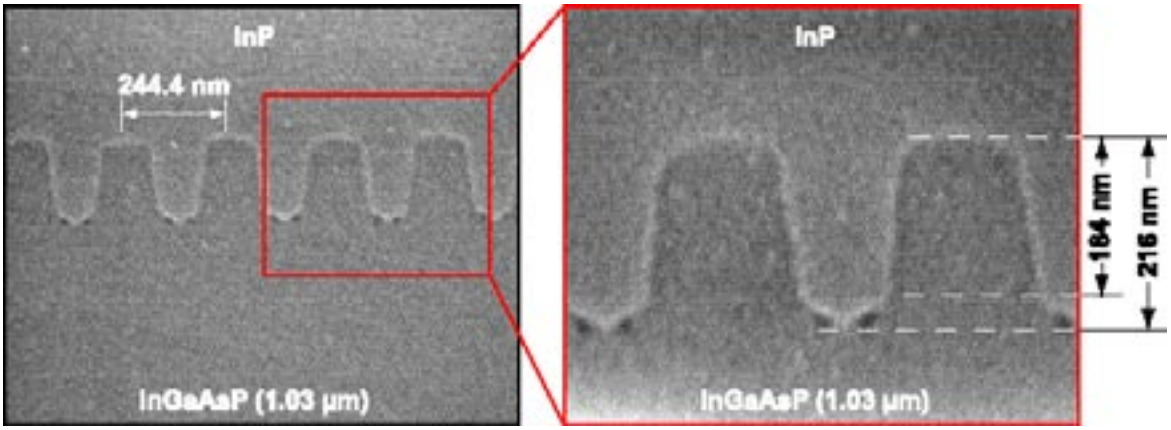

Fig. 39: Scanning electron showing the profile of the overgrown structure; the square tooth grating shows very little degradation. Chuck Joyner, of Lucent Technologies, performed the overgrowth.

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repeatedly transferred to optical substrates using X-ray lithography.

One of the critical challenges faced by integrated Bragg gratings is that they require submicron grating structures patterned over relatively tall optical waveguides. In order to address this topography problem, we have developed a novel dual-hardmask process, depicted in Figure 37. This allows both lithography steps to be performed over essentially planar surfaces. The process is quite general, in that it can be applied to almost any waveguide structure. For example, Figure 38 illustrates how we have used this approach to pattern a quarter-wave-shifted Bragg grating on top of a 1.1 micron-high InGaAsP waveguide. This micrograph illustrates the power and flexibility of our fabrication scheme: we can engineer complex submicron-period Bragg-grating structures with precisely positioned, abrupt phase shifts, placed atop relatively tall waveguide structures.

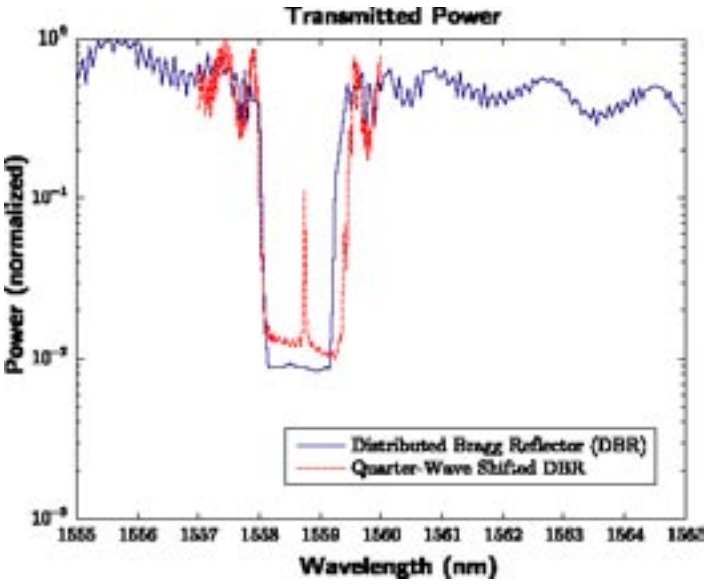

Fig. 40: Performance of the in-line filters shows that our fabrication sequence results in good devices.

Double-Sided Interconnect Technology for 3-D Integration

Personnel
I. Lauer
(D. Antoniadis)

Sponsorship
SRC

As scaling reduces the intrinsic delay associated with transistors in ULSI, interconnect delay becomes a bottleneck for increased system performance. Double-sided interconnect technology is being investigated as a means to increase interconnect performance. By "sandwiching" an SOI film between interconnect layers, routing can be potentially be improved, shortening line lengths. Additionally, the process used to fabricate double-sided interconnects can be extended to 3-D integration.

The focus of this research is to develop a process for fabricating double-sided interconnects. This approach entails fabricating NMOS devices on an SOI wafer and forming a layer of double-damascene tungsten interconnects. The SOI film is then transferred to a handle wafer by means of wafer-bonding and subsequent removal of the bulk of the SOI wafer. Additional interconnects are then fabricated on the exposed underside of the SOI film. Fabrication of a demonstration structure is currently underway.

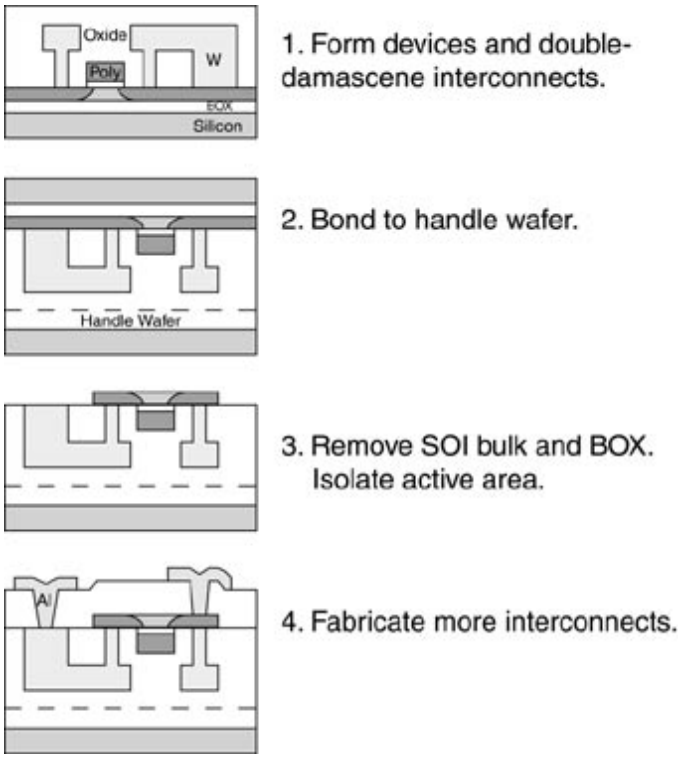

Fig. 41

Three-dimensional Integration of GaAs and Si Circuitry using Silicon-on-Gallium Arsenide Techniques

Personnel

E. Barkley and C. G. Fonstad, Jr., in collaboration with Mr. A. Loomis of MIT Lincoln Laboratory

Sponsorship

DARPA

Recently we proposed the development of a technology for 3-dimensional heterogeneous integration of silicon CMOS VLSI (memory and signal processing electronics) with III-V HEMT and HBT MMICs using aligned low-temperature oxide wafer bonding, with the purpose of dramatically increasing the capabilities, complexity, and performance of microwave integrated circuits, and we are currently pursuing this goal in a one-student effort.

The aspects of modern electronic systems that are hardest to integrate on GaAs and InP are large amounts of memory and highly complex signal processing circuitry. By integrating silicon CMOS VLSI directly with III-V MMICs, we immediately add high density memory and complex signal processing circuitry to the MMIC toolbox, highly leveraging the billions of dollars spent on developing modern silicon technology, and leapfrogging completely the costly and formidable (perhaps impossible) problem of fabricating comparable circuitry in GaAs and InP. The proposed technology represents a paradigm-shifting enhancement in MMIC complexity and performance. The CMOS circuitry can be used, for example, to store coordinate data, adjust phase delays and steer beams, tune and/or change carrier frequencies, modify code patterns and keys, monitor signal quality and make critical adjustments to optimize performance, do complex signal conditioning, and much more, in the underlying MMIC. The only limitations to the potential of these Intelligent MMICs should be the imaginations of application engineers.

The present concept builds on the low temperature oxide Silicon-on-Gallium arsenide (SonG) bonding process we developed for optoelectronic integration. The proposal is to bond fully processed silicon and III-V wafers using low-temperature oxide bonding techniques, to remove the substrate of the silicon wafers, and to then interconnect the three-dimensionally stacked CMOS and microwave circuitry to complete the integration process. The silicon circuitry will be strained, but no more than in Silicon-On-Sapphire (SOS) integrated circuits.

Because of the thermal expansion coefficient mismatch between Si and GaAs and the presence of metalization on the processed IC wafers, the 3-D integration process must incorporate low temperature bonding techniques. We have explored two low temperature bonding methods, one of which involves the conventional use of clean, planar, hydrophilic surfaces at the bonding interface, and a second method which uses Spin On Glass (SOG) as a bonding agent. In both techniques a Low Temperature Oxide (LTO) is first applied to the SIMOX wafer. This LTO is then Chemo-Mechanical Polished (CMP) to obtain a planar surface, free of the topographical remnants of the underlying metal layers.

Using the conventional bonding process the bonding surface of both the GaAs and SIMOX wafer are made hydrophilic with an RCA clean. The wafers are then bonded under pressure using the Electronic Visions Wafer Aligner/Bonder. The quality of the resulting bond relies heavily on the surface roughness of the two wafers. Initial weak bonds using this method have prompted the use of Atomic Force Microscopy (AFM) to quantitatively evaluate the wafer surface roughness, and we are currently using the AFM results to determine an approximate maximum allowable rms surface roughness specification that must be met by the CMP process to obtain a strong hydrophilic bond.

In parallel with the conventional hydrophilic bonding method, we are experimenting with using SOG as a bonding agent. SOG is typically used as a part of the Inter-metal-Layer Dielectric (ILD) stack in conjunction with conformal CVD oxides because of its gap filling abilities. It is spun on as a relatively low viscous liquid but after a sequence of increasing hot plate treatments followed by a cure at 400 C, it pyrolizes to form an inorganic glass with SiO_2-like characteristics. We

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have successfully bonded Si wafers using SOG. After spinning SOG onto both wafers, each wafer separately undergoes the hot plate treatments. The two wafers are then brought into contact and the bonded pair is cured at 400 C. The wafers are contacted before the final cure because at this point the SOG is plastic-like and exhibits good sticking and gap filling characteristics. The razor blade strength test showed that the bond was very strong, and after separation it was apparent that in most locations the SOG had cracked and did not delaminate from either of the bonding surfaces. Perhaps more importantly, the bond was also very strong before the cure meaning that the wafer pair could withstand a backside thinning of the SIMOX wafer in the case of a SIMOX to GaAs wafer bond. The higher temperature cure could then be carried out after the thinning step. The drawback to this technique is the formation of gas pockets in the SOG. We believe that this is a result of outgassing from the SOG during the cure step, and we are experimenting wicycles to minimize the post-bond outgassing during the cure step.

Fabrication and Characterization of Er2O3 Thin Films

Personnel

K.M. Chen, M. Lipson, X. Duan, and M. Aidan
(L.C. Kimerling)

Sponsorship

MARCO Focused Research Center on Interconnect
(SRC/DARPA)

Erbium oxide (Er2O3) is a promising luminescent material for microphotonic devices because the Er3+ f-shell transition is at l=1.54 mm and is temperature independent. Moreover, the concentration of Er3+ ions in the oxide is greater by several orders of magnitude over Er-doped systems, thereby enabling access to higher luminescence intensities and light amplification. We have fabricated Er2O3 thin films via UHV reactive magnetron sputtering of Er metal in an Ar/O2 mixture at room temperature.

The as-deposited film is amorphous and does not show PhotoLuminescence (PL) because the required ligand field for the Er atoms is absent. An anneal in O2 is done to crystallize the film, thereby optically activating the Er atoms to yield sharpline PL at 4K. Interestingly, in addition to annealing, we have found that Er2O3 films which have been deposited and annealed on a film of SiO2 possess strong PL compared to films deposited directly onto Si; this result has implications on the Er-O-Si phase diagram. In this work, we investigate the relationship between the oxide microstructure and its optical properties. We examine the effect of sputter plasma power and gas pressure, subsequent anneal time/temperature and ambient, and underlying film. Finally, we integrate our understanding of Er2O3 film growth to demonstrate a microphotonic device using this material.

Diffusion and Activation of N-type Dopants in Silicon Germanium Alloys

Personnel
S. Eguchi
(J. L. Hoyt)

Sponsorship
Hitachi Ltd., DARPA, and collaboration with IBM

We are studying diffusion and electronic properties of n-type dopants in Silicon Germanium (SiGe), to enable the fabrication of a wide range of devices. The *npn* SiGe-base Heterojunction Bipolar Transistor (HBT) has been successfully commercialized world-wide as an RF device with high speed and low power density. In this device, the use of a p-type SiGe base has stimulated studies of the diffusion of boron in SiGe alloys, with no information about n-type dopant behavior. With the recent success of the strained Si MOSFET, new markets are expected to be developed based upon strained Si/relaxed SiGe CMOS circuits. An understanding of n-type dopant diffusion in SiGe, specifically the formation of the source/drain regions in the NMOS and the n-body region in the PMOS, is essential for the success of this technology. In addition, n-type SiGe fabrication technology is expected to be important for the development of other devices such as thermoelectric generators, novel MOSFET structures that utilize SiGe source/drain contacts, and the *pnp* HBT.

As a first step, we compare the diffusivity of ion implanted Arsenic (As) and Phosphorus (P) in SiGe and Si. The relaxed SiGe epitaxial wafers are provided by Chris Leitz (E. A. Fitzgerald, Materials Science and Engineering). The SiGe samples have a 2 micron-thick graded-SiGe layer, and a 20% Ge, 2 micron-thick top layer, doped with boron to 10^{17} cm^{-3}. The Phosphorus-doped samples were implanted at 30 KeV, 8 x 10^{14} cm^{-2}, and the Arsenic implants were 30 KeV, 4 x 10^{14} cm^{-2}. After implantation, a 50 nm-thick low temperature oxide cap layer was deposited on the wafers. The samples were then furnace annealed at 1000C for 30 minutes in an Ar ambient. The oxide layers were stripped and samples were analyzed by Secondary Ion Mass Spectrometry (SIMS) at Charles Evans and Associates. The SIMS data was compared with SURPREM4 simulations. For comparison, Si control pieces were processed and analyzed at the same time as the SiGe samples. The diffusivity of n-type dopants is observed to be enhanced in SiGe compared to Si, in contrast to the diffusion of B, which is known to be retarded in SiGe relative to B diffusion in Si. Figure 42 compares the Phosphorus data for Si and SiGe, along with the SUPREM simulations. The expression for the concentration-dependent diffusivity of P in Si must be multiplied by a factor of roughly two, in order to match the P in SiGe profile. The junction depth in the SiGe sample is about 0.7 micron. Figure 43 shows the results for Arsenic under similar conditions. The effective arsenic diffusivity enhancement factor is roughly 7 for diffusion in SiGe compared to diffusion in Si. The

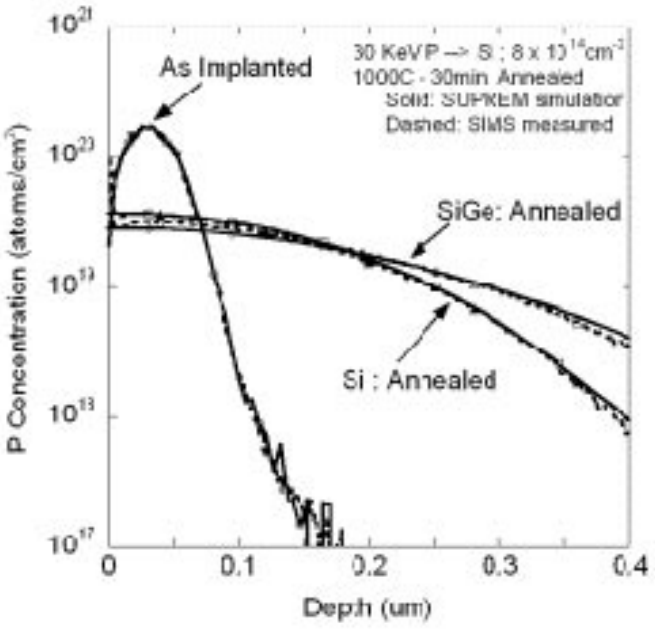

Fig. 42: Diffusion profiles for ion implanted P in Si and SiGe after 1000C, 30 min. furnace annealing.

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junction depth is roughly 0.35 microns for the As-doped sample. Our results indicate that As is a better choice than P for the formation of shallow n-type source/drain regions in SiGe. The next step will focus on the details of As diffusion and electrical activation.

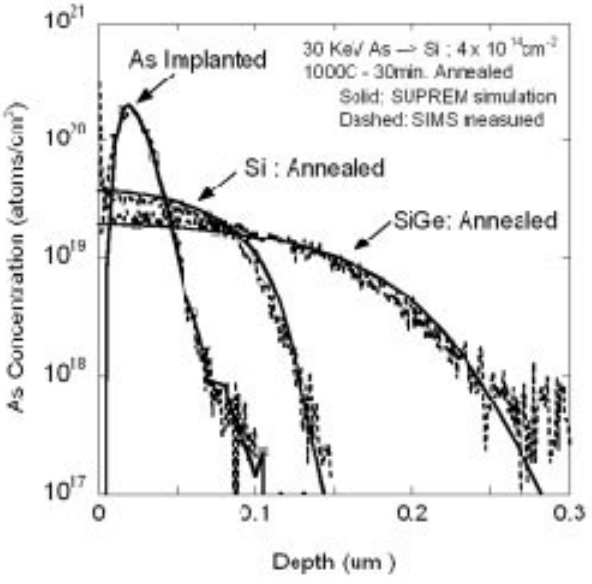

Fig. 43: Measured and simulated diffusion profiles for As in Si and SiGe after 1000C, 30 min. furnace annealing.

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Magnetically-Assisted Self Assembly - a New Heterogeneous Integration Technique

Personnel

J. Perkins, J. Rumpler, and K. Maezawa
(C. G. Fonstad, Jr., in collaboration of M. Zahn, EECS, and C. Ross, DMSE)

Sponsorship

Vitesse Professorship

We have recently proposed a radically new approach to the heterogeneous integration of compound semiconductor devices such as laser diodes with silicon integrated circuits, and have begun an experimental program to develop this technique. Our new approach, called Magnetically-Assisted Statistical Assembly (MASA), uses statistical self-assembly to locate compound semiconductor device heterostructures in shallow recesses patterned into the surface of an integrated circuit wafer, and short-range magnetic attractive forces to keep them there. When all of the recesses on the wafer are filled with heterostructures, the wafer is processed further to transform the heterostructures into devices monolithically integrated with the underlying circuitry. The process is summarized in Figure 44.

During statistical assembly, the surface of a wafer prepared with recesses will be flooded with several orders of magnitude more nanopills than are needed to fill its recesses. The large number of pills will mean that there are many pills in the vicinity of each of the recesses, and with the symmetric nature of the pills will result in a high probability that a pill in the vicinity of a recess will fall into it. The strong short-range magnetic attractive force which will come into play when a pill settles into a recess will keep the pill from being removed from the recess by gravity or by another nanopill or by the fluid used to flood the surface with nanopills. The process can be favorably compared to carrier trapping by deep levels in semiconductors, and the probability that a given recess is filled will be one. Once the nanopills are assembled on the circuit wafer they will be fixed in position using a polymer which will also fill in any voids on the surface surrounding the pills and planarize the surface. Processing of the heterostructures to convert them into devices and integrate them with the underlying electronics then proceeds using standard monolithic photolithographic processes.

The MASA process is an attempt to combine the best features of our Epitaxy-On-Electronics (EoE) and Aligned Pillar Bonding (APB) integration techniques, with the ability to monolithically integrate any semiconductor device on any substrate (including full 12" silicon wafers and electro-optic waveguide substrates). In MASA the device heterostructures are located in recesses in the wafer surface as in EoE and APB, and the final device patterning, processing, and integration is done after assembly at the wafer level and in a batch mode. At the same time, the device heterostructures can be grown on their optimum substrate under optimal conditions, as in APB, but the epitaxial material is much more efficiently used than in APB because the pillars are etched in a close-packed array. Finally, the relative sizes of the device and IC wafer are unimportant in MASA, unlike EoE and APB which are limited by the lack of large GaAs or InP wafers (currently 6" and 4", respectively).

With the help of Profs Zahn and Ross (MIT), we have conducted an analysis of the magnetic retention concept, and we find that a 0.5 μm thick layer of Co-Pt alloy patterned into stripes 2 μm wide and magnetized normal to the substrate surface will exert sufficient attractive force on nanopills coated with a 0.2 μm film of Ni to hold them in a well very strongly, and the attractive force is very short range, as we want. It will be negligible if the separation between the pill and the bottom of the well exceeds 2 μm, but it increases rapidly at smaller separations and far exceeds the force of gravity, for example, when the separation is under 1 μm.

We will begin an experimental study of the MASA technique in 2001 and have already obtained mask sets for test arrays of recesses and nanopills to begin a study

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of the geometric dependence of this process. The mask for the recesses has 12 arrays of recesses with different combinations of recess diameter (55, 65, and 75 μm) and spacing (125 and 250 μm) and covering two different areas (0.5 and 1.0 cm square). These 12 sections are arranged such that they all can be patterned on one 4-inch wafer. The pill mask has 1.5 cm square arrays of pills in three different diameters (40, 45, and 50 μm). Each array contains 22,500 pills.

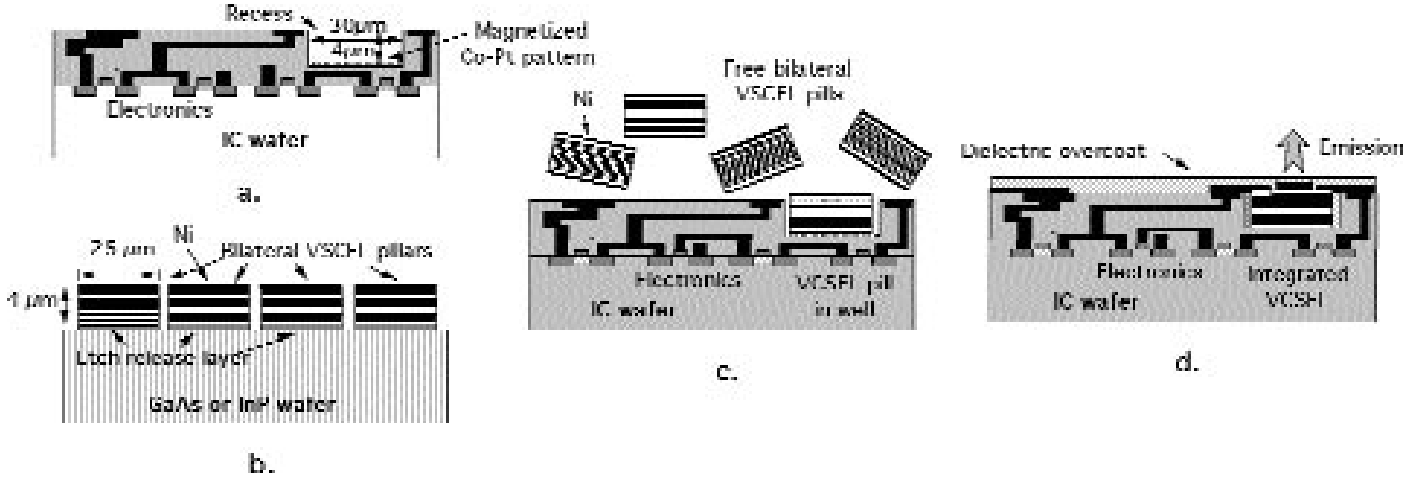

Fig. 44: The MASA process: (a) the processed IC wafer with the recesses prepared, and (b) the p-side down VCSEL wafer with pillars etched in a close-packed array; (c) statistical assembly of the freed nanopills in the recesses on the IC wafer; and (d) after completing device processing and integration.

Selective Self-Organization of Colloidal Particles

Personnel
K.M. Chen, X.P. Jiang, and P.T. Hammond
(L.C. Kimerling)

Sponsorship
ONR

Submicron sized colloidal particles have been selectively self-organized into patterned arrangements on a substrate using a novel technique. At the substrate, a polyelectrolyte multilayer film has been deposited onto a chemically patterned surface; subsequently, the polyelectrolyte surface is immersed in an aqueous colloidal suspension of bare SiO_2 microspheres or functionalized polystyrene latex particles. The colloids self-organize at the surface, driven by the spatially-varied electrostatic and secondary interactions between the colloid and the substrate. The polyelectrolyte platform provides a strong bond to the colloids, imparting mechanical robustness which enables post-processing of the patterned assemblies. The polyelectrolyte also resents the feasibility of introducing functionality into the underlying layers. We have demonstrated control over the density and selectivity of particle adsorption. Three mechanisms have been used to control adsorption:

(i) pH of the colloid suspension, which determines the ionization of the uppermost surface of the polyelectrolyte multilayer;

(ii) ionic strength of the suspension, which determines the extent of charge screening about the colloid and polyelectrolyte; and

(iii) concentration of added surfactant, which causes charge screening and introduces hydrophobic interactions between the surfactant and polyelectrolyte.

Using a patterned polyelectrolyte, we have demonstrated self-assembly of single-particle chains of polystyrene latex spheres. We are investigating an energy model for the sequential adsorption process.

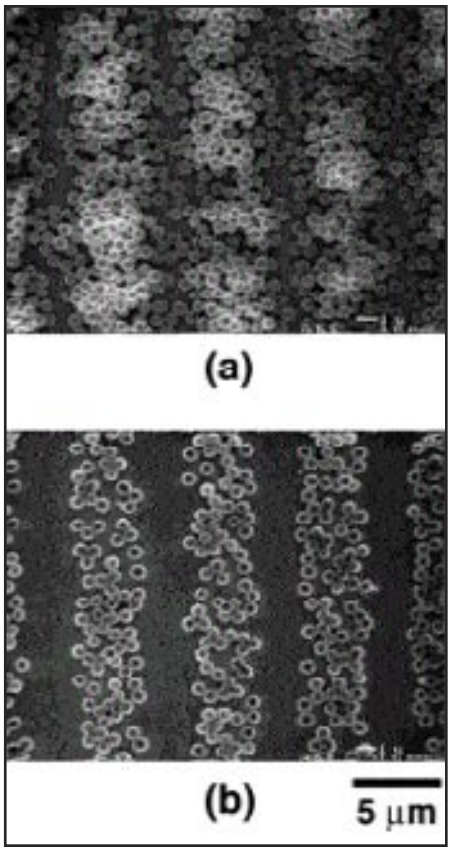

Fig. 45: SEM micrographs of SiO_2 microspheres bound by electrostatic attraction onto an underlying patterned polyelectrolyte at (a) pH = 6.8 and (b) pH = 8.1.

Silicon Field Emitters with Integrated Focusing Electrode (IFE-FEA's)

Personnel

L. Dvorson
(A. I. Akinwande)

Sponsorship

DARPA, NIH, and Creativ MicroTech

The goal of this project is to integrate a focusing electrode into the standard field emitter triode. The additional electrode, positioned above the gate, will be used to collimate the field emission beam; thus, it will help overcome the tradeoff of resolution versus brightness, luminous efficiency and display lifetime that limits the performance of today's field emission displays. We have already fabricated an IFE-FEA using the Spindt cone process; however, those devices suffered from tip-to-tip non-uniformity and dielectric breakdown in the gate to focus insulating layer. Based on prior work on silicon field emitters carried out in our group, we expect silicon IFE-FEA's to achieve considerably higher tip-to-tip uniformity and operational stability in the focusing mode.

To fabricate silicon IFE-FEA, we have designed a novel 3-mask CMOS-compatible, CMP-based process that begins with formation of a high aspect ratio silicon pillar with a pointed end (i.e. a silicon "pencil"). Ingenious use of CMP then permits us to reduce gate radius to 0.25 mm while keeping gate-to-cathode insulation at 1.5 mm. As of now, this is the last major stage of the process that we have completed. We are currently working on opening the gate aperture - perhaps the most difficult part of the process - using either CMP or dry etch. After this step, the same CMP technique would allow us to similarly reduce the focusing aperture. Once the focusing aperture is opened, either by CMP or by dry etch, patterning the gate and focus contacts completes the process. The masks that we laid out incorporate field emitter arrays of several different sizes and shapes, which will permit a more comprehensive electrical characterization of the completed devices.

To carry out precise optical characterization of the focusing performance of IFE-FEA's, we are assembling a system of high-sensitivity camera, an image-grabber video card and image processing software.
On the device modeling front, we have significantly expanded our Bowling Pin Model for conical field emitters. We were able to derive expressions for gate-to-cathode capacitance, closed form IV equation for a field emitter, and a governing relation for the optimal operating voltages on the gate and focus electrodes. We expect the latter relation, which was confirmed by computational studies carried out by another student, to be particularly useful in determining the best operating point for the IFE-FEA.

Silicon Field Emitter Array Fabrication and Characterization

Personnel

M. Ding
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Sponsorship

DARPA

Field emission phenomena are being explored in various devices such as Field Emission Displays (FEDs), sensors, microwave amplifiers and switches. High quality Field Emitter Arrays (FEAs) are critical for all these applications. A field emitter is made up of a micron-sized cone located within a gate aperture. An applied gate voltage establishes potential difference between the cone tip and the gate, resulting in high electric field at the cone tip. Electrons then tunnel into the vacuum through the barrier at the tip and then are accelerated to the anode by a high anode.

Low turn-on voltage, high transconductance and high current density characterize the performance of FEAs. Low operating voltage is directly related to power dissipation, an essential concern in displays for portable information appliances. Furthermore, low voltage operation would allow single wafer integration of FEAs with standard CMOS devices. High current density and high transconductance are directly related to the high frequency performance of the device. These performance goals can be simultaneously achieved by increasing the transmission of electrons through the surface barrier. Reducing the barrier height (lower work function) and/or reducing the barrier width (high electric field at tip through high field factor) attain this goal. In our work we focus on reducing the barrier width by reducing the tip radius.

Last year we reported a doped-poly-silicon gate Si Field Emitter Arrays (FEAs) fabricated with Chemical Mechanical Polishing (CMP) that had extremely low turn-on voltage and negligible gate current. The devices are fabricated on 4-inch (100) n-type silicon substrates with dopant concentration of about 10^{16} cm^{-3}. The devices turned on at about 25-30V without field forming and conditioning. Some devices are observed to turn on at 20V. It was the lowest turn-on voltages for 1-μm gate aperture devices. We also observed the negligible gate leakage currents that are 3-4 orders of magnitude smaller than emitter current. We attributed the low turn-on voltage to the extremely small radius of curvature of the Si tips, achieved through low temperature oxidation sharpening. We attributed the low gate leakage current to two factors: (i) the symmetric and self-aligned nature of the CMP-FEA and (ii) the high quality of the gate dielectric which consists of a thin thermal oxide at the SiO_2/Si interface and a thicker densified LPCVD oxide. Furthermore the devices showed excellent uniformity for different sized arrays, which were crucial for device reliability and mass production. The current-voltage characteristics agree with Fowler-Nodheim field emission theory very well in the transmission-controlled region. Beyond the transmission-controlled region we observed current saturation due to the insufficient electron supply limited by the low dopant concentration and small cross-section of the electron supply channel near the tip apex region.

Presently we are fabricating several batches of wafers with different doping concentration to study further and relationship between the current saturation and the wafer doping. The fabrication is near its final steps. The fabrication of very high aspect ratio field emitters for the purpose of field ionization arrays is also underway. Also we are the set-up of the Scanning Maxwell Stress Microscope system to image simultaneously the topology and the surface potential of the wafer surface and emitters.

Field Emission from Thin Films

Personnel

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Sponsorship

IBM Fellowship, AFOSR, and NSF

Field Emission Displays (FED) are an important flat panel display technology. FEDs have several advantages over competing technologies (especially liquid crystal displays) in brightness, temperature range, and a need for external components such as a backlight. Cost and durability issues, however, have limited the success of FEDs in the marketplace. Our project seeks to address the cost problem by creating an emissive backplane using a thin film of carbon nanotubes or a conjugated polymer. This approach provides two benefits. First, it eliminates the sensitive and difficult micromachining typically performed to create emissive backplanes. Second, all of the processing steps occur at temperatures below 90° C, so a wider variety of substrates than traditionally employed in displays may be used. This includes organic and flexible materials.

The performance will be measured by using patterned substrates coated with candidate materials. We will examine the emission characteristics in vacuum both on a macroscopic level and at localized sites using a scanning tunneling microscope.

For the nanotube side of the project, the goal is to characterize their field emission properties. The mechanisms for field emission are being studied to develop possible models for the nanotube emission process. I-V curves studying the Fowler-Nordheim behavior of nanotubes in particular will be valuable for this goal. An AFM will also be used to examine and manipulate the tubes, and a four point probing of individual nanotubes will be attempted.

In thin organic films, emission of this type has already been observed in regioregular polythiophene derivatives. The first effort is to duplicate those results. Other conjugated candidate materials will also be screened. A second focus of the project is to identify the mechanism through which this emission occurs. Work at other universities has identified morphological changes in the polymer film which are believed to be the source of electrons. This remains unconfirmed, however, until STM measurements of the emissivity can be made on a microscopic level. An understanding of the mechanism for emission from the organic film can ultimately lead to the development of superior emitting structures.

Work thus far has focused on obtaining the materials, chemicals, and equipment necessary for testing candidate materials, particularly suspended nanotube preparations and polythiophene derivatives which will be examined first. A significant effort has also been made to design and fabricate test substrates with features which allow the determination of intrinsic properties (such as the emissivity per surface area and surface conductivity of the material). Both of these efforts are almost complete, and testing is expected to begin in February of 2000.

Care has been taken to insure that significant flexibility remains in the testing process. The substrates can be made with a variety of metals to test workfunction dependence on the emission, and almost any deposition process may be used to coat the substrates with either nanotubes or organic materials (including Langmuir-Blodgett and vacuum evaporation). This leaves the project open to new material and substrate approaches which is essential for testing novel candidates.

Opposite Page:

Thermal pad imaging in CMP. An Agema 550 infra-red camera is focused upon the polishing pad behind the trailing edge of the carrier. Temperature measurements at the indicated discrete pad positions in the image provide spatial information regarding polish uniformity and endpoint.
Courtesy: D. White (D. Boning).
Research sponsored by NSF/SRC ERC for Environmentally Benign Semiconductor Manufacturing