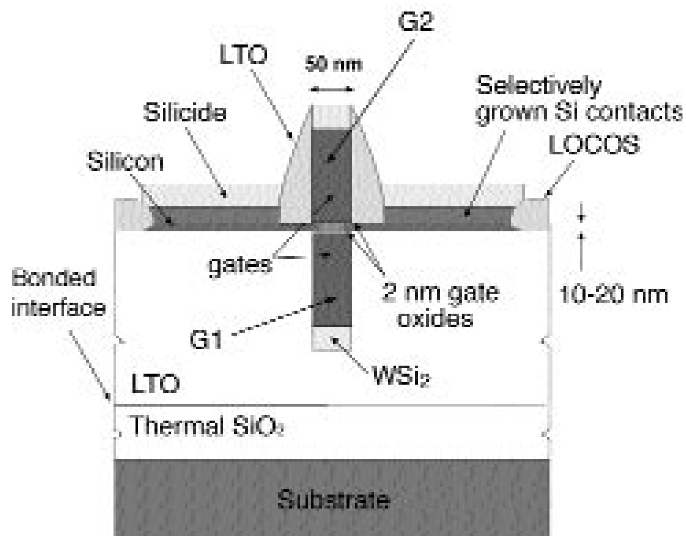
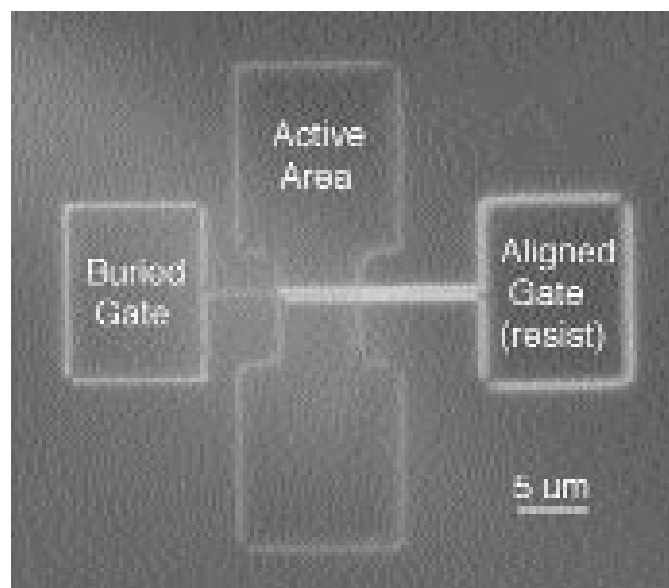
Electronic Devices





Electronic Devices

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Double-Gate MOS Transistor with Self-Registration

Personnel

D. Song (D. A. Antoniadis)

Sponsorship

DARPA

The double-gate MOSFET is considered the most promising candidate to circumvent the scaling limits of bulk CMOS devices. In order for the double-gate MOSFET to exhibit its inherently ideal features such as approximately twice current per unit width, enhanced transconductance, ideal subthreshold swing, and short-channel effect immunity, it should satisfy several criteria, namely : 1) perfect top-to-bottom gate alignment, 2) very thin uniform undoped Si channel, 3) source/drain extension structure to enable high doping, as well as thick source/drain structure to reduce the series resistances, 4) control of spacer length to reduce gate to source/drain overlap capacitance while maintaining proper current drive, 5) suitable process integration for a higher dimensional IC implementation. Such a device structure has not been yet developed. In this work, we propose a double-gate MOS transistor with self-registration (DGSR). The key features of DGSR are i) a top-to-bottom gate self-registration device structure , where the spacers in the top-to-bottom are self-aligned, and the alignment accuracy of the top-to-bottom gate is determined by the difference in spacer thickness ; ii) a thick source/drain structure using a reverse active patterning ; iii) an easy doping control of source/drain extension regions by ion implantation onto those regions just after gate formation as well as an easy control of spacer length. Also the device fabrication process has been designed to avoid novel processing techniques so that it can be ready to be integrated into a standard CMOS process, and it has also been designed to be suitable for a higher dimensional IC integration.

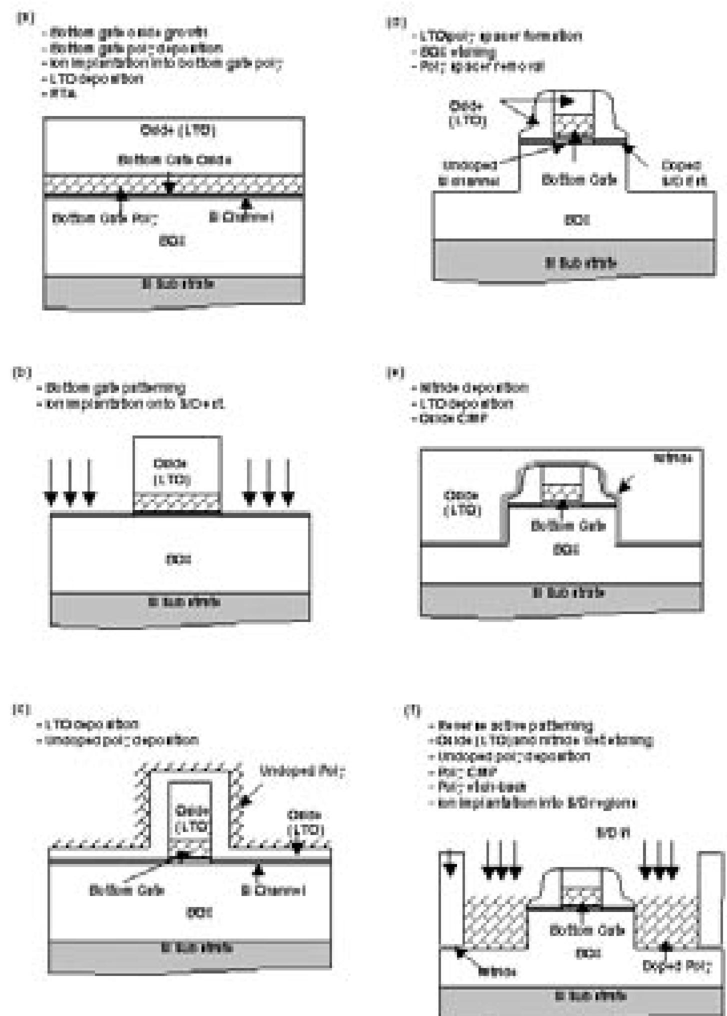

Fig.1

Shown below in Figure 1 is a schematic of key process steps used to realize the DGSR MOSFET. Fabrication starts with formation of the bottom-gate stack on an SOI wafer. Then the source/drain regions are ion implanted. After LTO/poly spacer formation, the buried oxide is etched to make a top-to-bottom gate self-

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as a hard etch-mask. To realize a thick source/drain structure, a reverse active patterning technique is used followed by removal of the residual poly spacer, thin nitride deposition, and LTO deposition and oxide CMP for planarization. Poly deposition, poly CMP, poly etch-back, and ion implantation into source/drain regions followed by wet etching of the oxide and nitride complete the thick source/drain structure. It is interesting to mention that at this process step, the formation of interconnection levels to either a higher dimensional integration or a single gate MOSFET for the characterization of process quality as well as electrical device characteristic can be made. The SOI wafer with polished LTO is bonded to a handle wafer with thermal oxide, and the SOI substrate and buried oxide are removed. Thin sacrificial oxide growth is followed by nitride spacer formation, and the thin oxide is removed. By top gate oxide growth, top gate poly deposition, top gate poly CMP and etch-back, and ion implantation for top gate as well as source/drain regions, the device structure of the DGSR MOSFET is completed with the subsequent formation of interconnection levels.

Optimal MOSFET Design for Low Temperature Operation

Personnel

K. M. Jackson(R. Dennard – IBM, D. A. Antoniadis, H. Smith)

Sponsorship

IBM, Intel (Intel Fellowship)

Low temperature operation of MOSFETs improves their performance by increasing the mobility and by allowing lower threshold voltages. The goals of this project are to understand how to achieve an optimal device design at low temperature and how much performance gain occurs at low temperature. A set of devices from IBM which have two different threshold voltage designs (a "low-V_{th}" design and a "high-V_{th}" design) were used to examine two design options. Since a device's switching speed depends on both current and capacitance, the two designs were compared at the same channel length (approximately the same gate capacitance) allowing the on-current of the devices to give a direct measure of device switching speed. Also, in order to make a fair comparison, a forward substrate bias was used to adjust the off-current of all devices to the same value (10^{-9} A/μm). A large forward bias can be used, with no impact on the off-current, because the source and drain p-n junction current is significantly reduced at low temperature.

Plotting each device's on-current versus channel length (L_{eff}) clearly shows that the low-V_{th} design consistently yields a higher on-current for a given L_{eff} (Figure 2) and same off-current (Figure 2).

Examining device characteristics (again, at the substrate bias needed to set the off-current), the low-Vth devices have a steeper subthreshold slope than the high-Vth devices (Figure 3 middle) which, given the fixed off-current, results in a lower V_{th} (Figure 3 top) and thus a higher on-current. The low-V_{th} designs also have less short channel effects as evidenced by their lower drain induced barrier lowering (DIBL) at a given Leff (Figure 3 bottom).

The differences in subthreshold slope and short channel effects are directly related to the maximum depletion depth in the channel ($x_{d,max}$). For instance, a small $x_{d,max}$ gives a larger (shallower) subthreshold slope, but better short channel effects. In this

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case, although the two device designs (at a given L_{eff}) have the same off-current, the high-Vth design has a smaller $x_{d,max}$ than the low-V_{th} design. This results in the worse subthreshold slope which gives a higher V_{th} and thus a lower on-current. What this suggests is that designing for a low threshold voltage requires both reaching the maximum off-current allowed, as well as minimizing the subthreshold slope by having as large a $x_{d,max}$ as allowed by short channel effects limits.

In summary, the optimal design of a MOSFET at low temperatures requires the use of a low threshold voltage. A low V_{th} with the proper $x_{d,max}$ (balancing the subthreshold slope and short channel effects) is best achieved by using a lower channel doping, than a room temperature device, coupled with a forward substrate bias. The experimental results above for 80 nm N-MOSFETs at 200 K show the low-V_{th} design achieving a 5% higher on-current (for the same off-current) than the high-V_{th} design. Continuing work is focusing on quantifying the origins of the performance gains across designs and versus temperature.

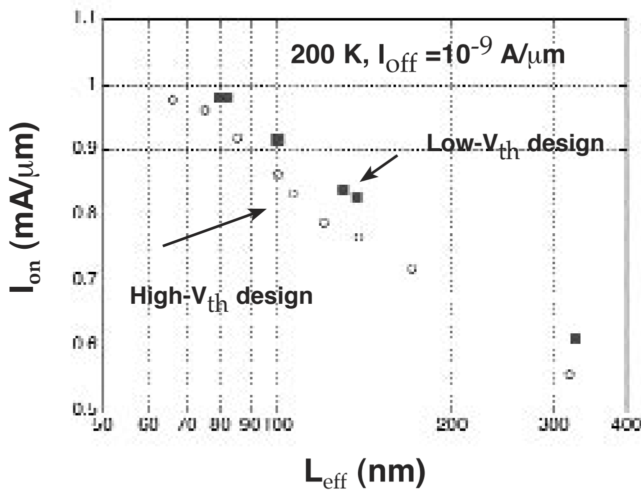

Fig. 2: On-current vs. L_{eff} at I_{off}=10-9 A/mm

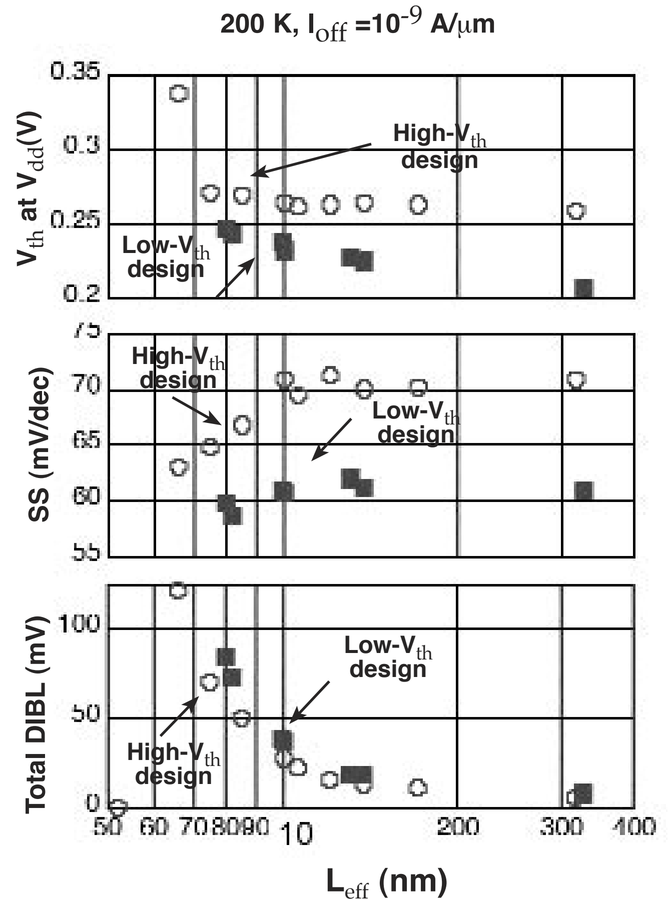

Fig. 3: Device parameters at the substrate bias that gives an I_{off}=10^{-9} A/μm.

Experimental Investigation of Carrier Velocity and Mobility in Deeply Scaled NMOS

Personnel

A. Lochtefeld (D. A. Antoniadis)

Sponsorship

DARPA

Continued success in scaling bulk MOSFETs has brought increasing focus on fundamental performance limits. Drain current is limited by carrier velocity (v_{eff}); the theoretical limit to carrier velocity is the rate at which carriers can be thermally injected from the source into the channel. This "thermal limit" is equivalent to fully ballistic transport. In this work we investigate the physical meaning of different MOSFET carrier velocity extraction methods, in order to measure appropriately how close to the thermal limit a modern MOSFET operates. Applying our findings to two advanced industry NMOS technologies, we experimentally set an upper bound on the thermal or ballistic efficiency . Figure 4 summarizes these results: we find that a deeply-scaled (L_{eff} < 50 nm) 1V NMOS technology operates, at most, at 40% of the limiting thermal velocity. In addition, we see no indication that bulk NMOS scaling will bring us closer to this limit.

	T_{ox}^{inv} (nm)	Nom. V_{th} (V)	Min. Useful L_{eff} (nm)	V_{eff} (cm/s)
Tech. A	2.4	0.3	40	6.6×10^6
Tech. B	4.3	0.35	65	7.7×10^6
25 nm MC	1.8	0.27	25	$6.7\text{-}7.6\times10^6$

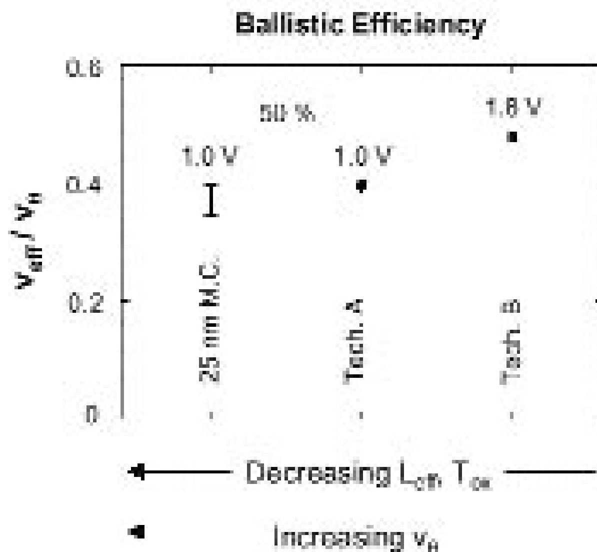

Fig. 4: Ballistic efficiency (v_{eff} / v_q, where v_q is the thermal velocity of carriers in the source accumulation layer) for industry bulk NMOS technologies A and B, as well as for Monte-Carlo results for 25 nm L_{eff} NMOS. Derived from measured effective velocities, plus estimates for v_{inj}. The decrease in v_{eff} from "B" to "A" may be mainly due to a decrease in mobility; this may be due to heavier channel doping necessary to suppress short-channel effects, as well as to increased scattering associated with ultra-thin oxides.

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Improving the ballistic efficiency of deeply-scaled MOSFETs may require strategies for enhancing carrier mobility, such as strained-Si channels, or undoped thin-film SOI (Silicon-on-Insulator). However, the relationship between low-field effective mobility (μ_{eff}) and high-field carrier velocity is not well understood for deep-sub-100 nm MOSFETs, where the lateral electric field is far in excess of Esat (which corresponds to velocity saturation in isotropic field regions). We have investigated this experimentally by mechanically inducing uniaxial strain, via a four-point bending apparatus, on the above-mentioned 1V NMOS technology. As Figure 5 shows, shifting μ_{eff} in a long-channel device by 13% corresponds to a velocity shift in a short-channel device of 4%. However, uniaxial strain appears to effect short devices (which have higher average channel doping, due to non-uniform lateral doping profiles associated with halos) differently then long devices. Preliminary results suggests that shifting μ_{eff} in a short-channel device ($L_{eff} < 50$ nm) by just 5% corresponds to a velocity shift (in the same device) of 3%.

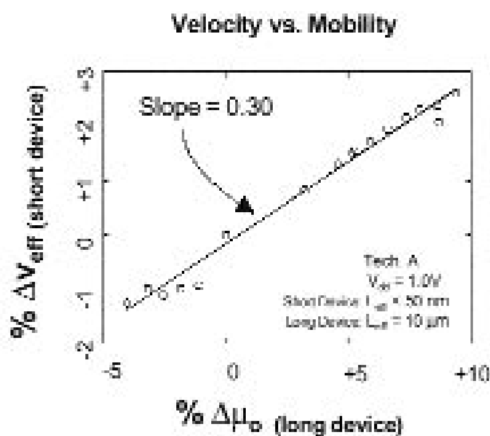

Fig. 5: Shift in long-channel mobility vs. shift in short-channel velocity, induced via uniaxial strain applied to technology A (see table, Figure 4).

SiGe CMOS Design

Personnel

H. Nayfeh (D. A. Antoniadis, J. L. Hoyt)

Sponsorship

SRC, DARPA

This study investigates possible substrate options that can be used for SiGe CMOS design. CMOS devices fabricated on SiGe substrates offer a practical means of extending the scaling of Si devices since it is silicon process compatible and allows for strained layers resulting in enhancement of electron and hole transport. One possible substrate shown in Figure 6 has been studied by Rim et. al at IEDM 1998.

Transport in this structure occurs in the strained silicon layer at the top. The layer is under biaxial tensile strain since the lattice constant of germanium is larger than silicon. It was demonstrated that NMOS devices built on this substrate exhibit enhanced electron mobility for a wide range of vertical fields but that PMOS devices suffered a degradation of enhancement for vertical electric field greater than 1.15 MV/cm resulting in further imbalance of PMOS and NMOS devices warranting a study of alternative substrates. Possible substrates where analyzed by performing electrostatic simulations using MEDICI.

One possible substrate shown in Figure 7 below combines a biaxial compressive layer giving enhanced hole mobility with a biaxial tensile strained layer for enhanced electron mobility.

The hole concentration can be made to be confined to the hole layer for a proper bias voltage due to the valence band discontinuity between $Si_{0.2}Ge_{0.8}$ and the strained-silicon. The electron population is concentrated in the strained-silicon layer due to the proximity to the surface and the conduction band discontinuity of strained-silicon and $Si_{0.2}Ge_{0.8}$. The substrate has promising potential for improving electron and hole transport, but the electrostatic integrity is poor as shown below in Figures 8 and 9 that show higher subthreshold slopes, SS.
The SS increases due to a large hole concentration in the buried compressive layer that results in a weaken-

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ing of the top-gate control of the electron charge. A larger Ge concentration is also simulated so as to increase the hole charge. The result is that the SS is larger demonstrating the effect of the hole well. Figure 10 below shows the band structure and charge concentration at subthreshold for the NMOS device.

The PMOS SS is degraded from 73 mV/dec to 100mV/dec. To understand this, the formula for the subthreshold slope is n*60mV/dec where n is an ideality factor that is 1+Cs/Cgc, where Cs is the semiconductor capacitance at subthreshold and Cgc is the gate to channel capacitance in inversion. The ratio of Cs to Cgc is larger for the buried hole well structure than the surface channel device due to hole charge modulation in the well reducing the Cgc capacitance and as a result increasing the ideality factor.
It is apparent that to improve the NMOS subthreshold characteristics the hole well below the electron well needs to be removed. A substrate that removes the hole well is shown below in Figure 9. The NMOS device area is achieved by selectively etching the top layers so that the buried hole is removed resulting in devices with the same electrostatics as the bulk-Si counterpart.

However, the PMOS to no surprise has a degraded SS for a Ge fraction of 60% in the buried layer. The PMOS electrostatics will improve by reducing the hole population in the hole well by reducing the Ge concentration since the valence band discontinuity is reduced. This indicates that a compromise between electrostatics and current drive improvement is needed since mobility enhancement increases with strain. Analysis is currently underway to determine the optimum layer structure.

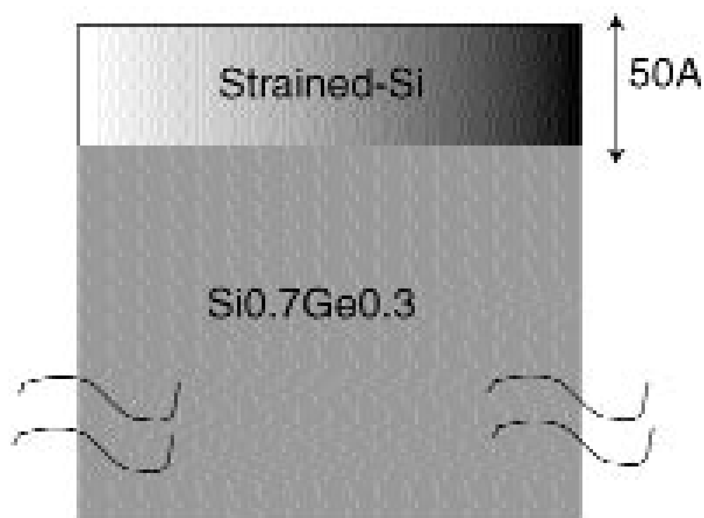

Fig. 6: Strained -Silicon CMOS substrate.

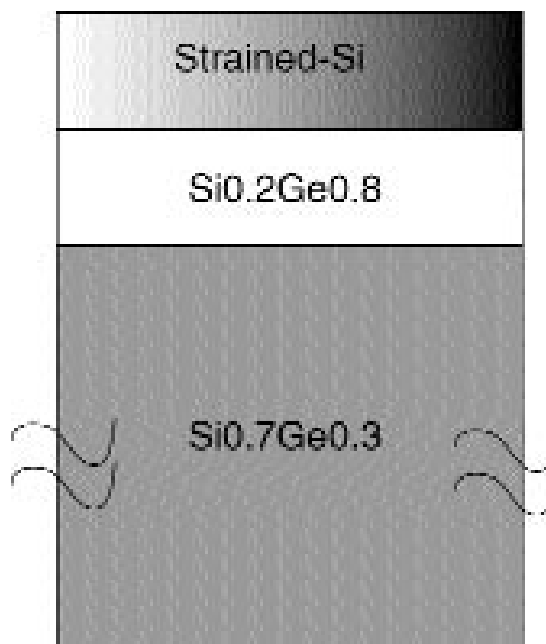

Fig. 7: Compressive and tensile strained layer subtrate.

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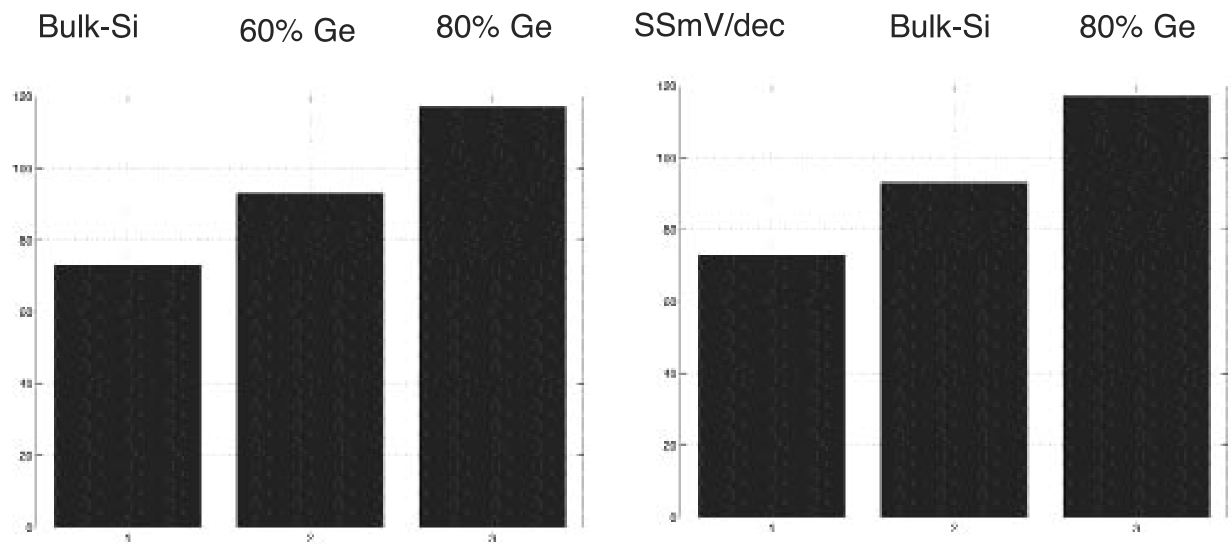

Fig. 8: (Left) Degraded NMOS SS. (Right) Degraded PMOS SS

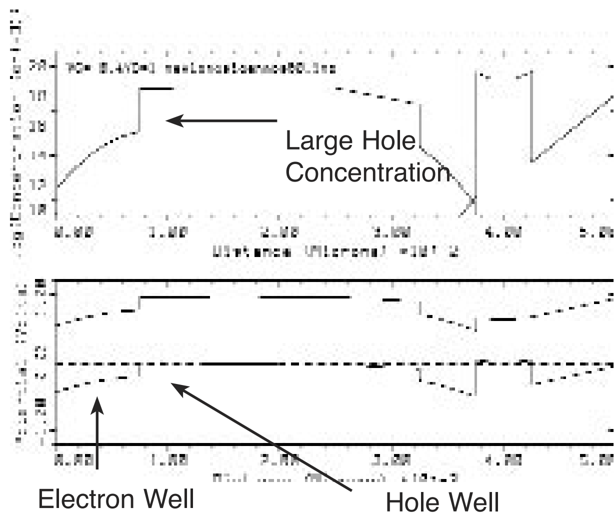

Fig. 9: Band structure and charge concentation at subthreshold for the NMOS device.

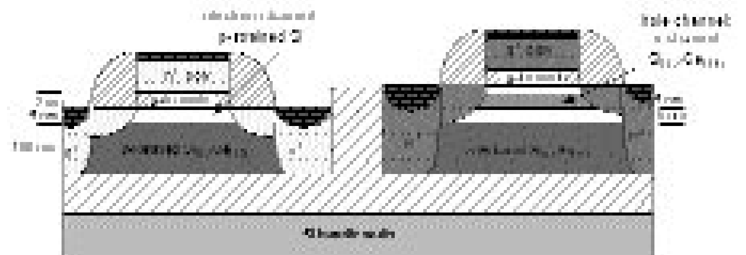

Fig. 10: Substrate with hole well removed.

SiGe Heterostructure Field Effect Transistors

Personnel

M.T. Currie, C.W. Leitz, Z. Cheng, M.L. Lee (E.A. Fitzgerald and D.A. Antoniadis)

Sponsorship

DARPA, Singapore-MIT Alliance, NSF/MRSEC

We are exploring mobility enhancements in heterostructure MOSFETs grown on relaxed SiGe virtual substrates. Such devices offer significant performance improvement over bulk Si devices and can be integrated into conventional Si MOSFET processing schemes. We have fabricated heterostructure MOSFETs via a novel short-flow process with a deposited gate oxide and a single photolithography step. The effects of strain and channel thickness on device mobilities have been investigated. In agreement with theoretical predictions, different mobility enhancement saturation behaviors are observed for strained Si n- and p-MOSFETs fabricated on relaxed SiGe virtual substrates. By performing an intermediate CMP step on the relaxed SiGe layers, strained Si devices were fabricated on virtual substrates of negligible surface roughness for the first time. The mobility enhancements of these devices are virtually identical to those of devices on unplanarized SiGe substrates. The process stability of strained Si devices has also been studied. The effects of Ge interdiffusion explain the mobility degradation of strained Si MOSFETs annealed at temperatures over 1000ºC. We are currently investigating MOSFETs fabricated on SiGe-on-insulator substrates, strained Ge p-MOSFETs, and optimized heterostructures for SiGe-based CMOS.

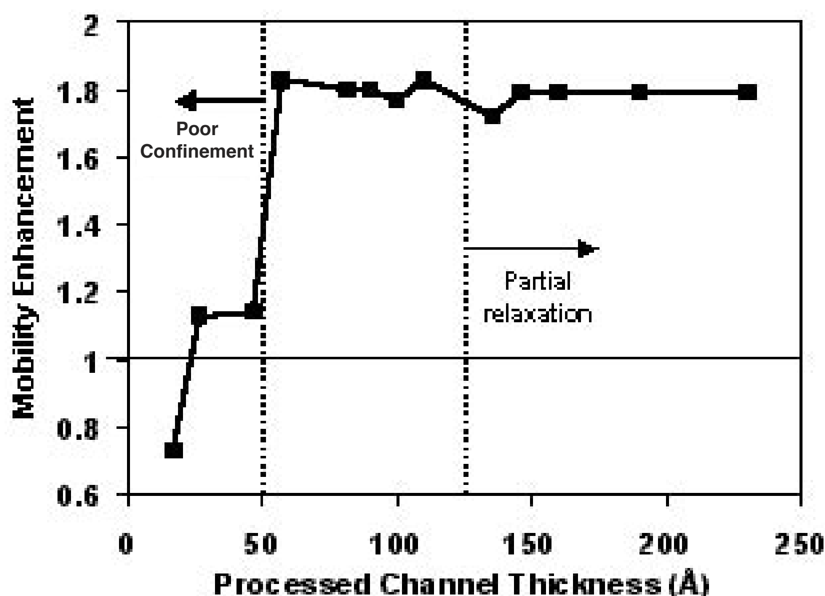

Fig. 11: Electron mobility enhancement of strained Si n-MOSFETs as a function of channel thickness. Poor confinement degrades the mobility of the thinnest channels. The slightly relaxed thickest channels exhibit no mobility degradation

CMOS Technology for 25 nm Channel Length

Personnel

A. Lochtefeld, M. Meinhold, D. A. Antoniadis and H. I. Smith

Sponsorship

DARPA and ONR

The double-gate (DG) MOSFET (Figure 12) is considered a promising device for CMOS scaling to deep sub-100 nm gate lengths. However, realization of the ideal DG-MOS structure involves significant technological challenges: formation and alignment of gates above and below a thin single-crystalline silicon layer, and achieving low source/drain resistance for this thin layer. We are addressing these issues though integration of three primary technologies: wafer bonding with pre-patterned features, interferometric alignment, and selective epitaxy.

Monte-Carlo modeling predicts that double-gated devices that are scaled to L_{eff} = 25 nm will have transconductances Gm in excess of 2000 mS/µm, while maintaining almost perfect sub-threshold slope. However, models also predict that the tolerance in aligning front and back gates has to be within Lg/4 in order to avoid performance deterioration due to overlap capacitance. The Lg/4 requirement translates into 6 nm alignment tolerance for a 25 nm channel. In order to meet this alignment challenge we will use the IBBI (Interferometric Broad-Band Imaging) alignment technique which achieves sub-nanometer misalignment detectivity. The planar double-gate devices will be fabricated starting with a SIMOX wafer. First the gate stack for the back-gate will be deposited and patterned by x-ray lithography. The structure will then be covered by a layer of CVD oxide, planarized, and bonded to a "handle wafer". The bulk of the SIMOX wafer will then be chemically etched using the back-oxide of the SIMOX wafer as the etch-stop. The fabrication will then follow a conventional SOI (Silicon on Insulator) process, with front gate precisely aligned to back-gate layer using the IBBI alignment scheme. The final structure is depicted in Figure 12.

We employ a direct alignment approach to form top-gates with correct relative placement to the bottom-gates. We have demonstrated the functionality of this alignment system. Figure 13 shows a DG-MOS device after top-gate x-ray lithography, with buried n^+ poly gate visible beneath a 25 nm silicon layer. Although we have attained alignment detectivity of the order of several nanometers, final alignment results are equally a function of precise pattern placement between the upper-and lower-gate x-ray masks. We have been developing a process to obtain this precision through close proximity x-ray mask replication. In this scheme, gate patterns from the upper-gate mask are transferred to the lower-gate mask using x-ray lithography. This is done while the alignment marks of the two masks are aligned. Lithography of this sort is challenging primarily for two reasons: 1) the pattern on the replicated mask must be of the same polarity as that on the source mask, 2) it is necessary to maintain sub-100 nm resolution. Maintaining pattern polarity is a subtle yet crucial aspect of this process. Recently we have succeeded in developing a mask replication process compatible with these constraints. The process that takes place on the duplicate mask involves the following four steps : X-ray patterning positive resist, liftoff (yielding a pattern reversal), etch down (forming trenches) and finally, Au electroplating within those trenches. Once these steps are accomplished, mother and daughter masks have precisely matching patterns when the two masks are compared face-to-face. This is a key result for this project.

We are also investigating performance of deeply scaled DG vs. bulk MOS. It has been projected that with aggressive channel dopant profile engineering, bulk may scale down to ~25 nm L_{eff} which may be near the practical DG-MOS limit. However, to achieve this the bulk MOSFET must have very heavy (~$1x10^{19}$ cm^{-3}) peak body doping to suppress punch-through, which results in a very high transverse electric field (E_{eff}) at the inversion layer. According to the well-verified universal mobility relationship, this can be expected to result in severely degraded mobility in bulk MOSFETs. In SOI devices with undoped channels, short channel

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effects are suppressed by limiting silicon and oxide film thicknesses. Body charge can be essentially zero, resulting in low Eeff and correspondingly superior mobility. Using 2D numerical simulations (Avant! MediciTM) we have determined the doping required for electrostatically sound bulk uniform-doped n-MOSFETs (at the L_{eff} = 50 and 25 nm generations), as well as the resulting E_{eff} seen by electrons in the inversion layer. In Figure 14 we show the corresponding range of mobility expected, based on the universal dependence of mobility on E_{eff}. Also shown are results for one additional bulk, and three SOI, MOSFET architectures. Our results suggest that single-gate SOI is an attractive alternative down to 50 nm L_{eff}. For deeper scaling, double-gate SOI should have a 3-4X mobility advantage over aggressively designed bulk NMOS.

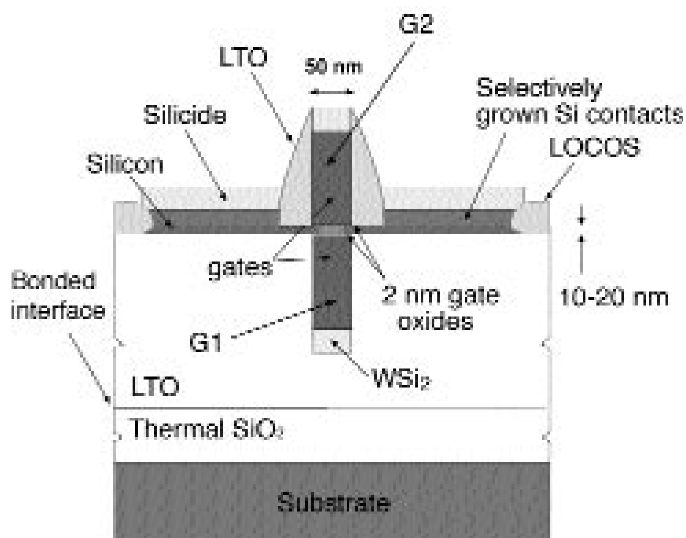

Fig. 12: Double-gate (DG) NMOS transistor with 25 nm effective channel length. Gate-to-gate alignment is via IBBI.

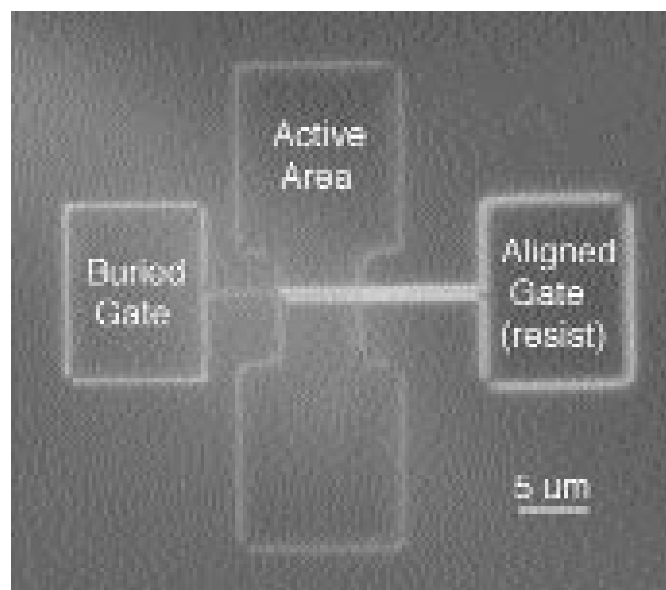

Fig. 13: DG-NMOS device after top-gate x-ray lithography. Alignment of gates is via IBBI.

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Understanding Mobility Behavior in Strained Si MOSFETs

Personnel

G. Xia (J. L. Hoyt)

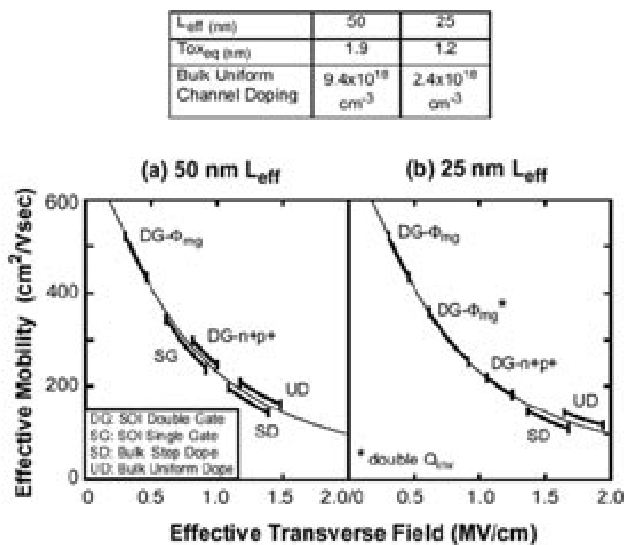
Sponsorship

SRC and IBM Corp.

An attractive method to enhance MOSFET performance is to alter the bandstructure of silicon to improve the carrier transport properties. This can be achieved by inducing biaxial tensile strain in the silicon channel. For example, epitaxial growth of 10 nm-thick layers of silicon on relaxed SiGe (20% Ge) will provide sufficient strain in the silicon. Recent results on the application of these concepts to silicon MOSFETs indicate significant strain-induced performance enhancements at a given channel length, in the deep sub-micron regime. Understanding the mobility enhancement mechanism is important for determining the ultimate performance limits of these devices.

In this project, we begin by studying issues related to the electron mobility in strained Si MOSFETs. One method of understanding the mechanism of mobility enhancement is to study the vertical effective field dependence of the mobility as a function of temperature. For high vertical fields (>1 MV/cm), it is anticipated that surface roughness scattering will dominate transport. The impact of strain on surface roughness scattering is not understood at this time. Lowering the measurement temperature reduces the phonon component of scattering, and thus enables us to observe the remaining mobility terms, which include Coulomb and surface roughness scattering, in strained and unstrained Si devices.

Strained Si n-MOSFETs (20% Ge) and unstrained Si control wafers with similar doping profiles were fabricated by K. Rim (Ph.D. thesis, Stanford). Our preliminary measurements at room temperature are illustrated in Figures 15 and 16. Figure 15 shows split-CV data which is used to obtain the inversion charge, Qi, which is required for the extraction of the effective mobility ueff = (L/W)gD/Qi. The lines in Fig.16 illustrate the mobility we have measured for strained Si n-MOSFETs, and unstrained Si controls, at room temperature.



L_{eff} (nm)	50	25
Tox_{eq} (nm)	1.9	1.2
Bulk Uniform Channel Doping	$9.4x10^{18}$ cm^{-3}	$2.4x10^{18}$ cm^{-3}

Fig. 14: Universal effective MOSFET mobility curves from [2], with regions of operation delineated for five different bulk and SOI device architectures. Figure 14a corresponds to the 50 nm L_{eff} generation, and Figure 14b to the 25 nm generation. "DG-Fmg" refers to double-gate SOI with midgap gate workfunctions. "DG-n^+p^+" refers to double-gate SOI with asymmetrical n^+/p^+ poly gates. For each device architecture the range of E_{eff} is determined from 2D simulation, and corresponds to a range of inversion layer densities (Qinv) from $0.8x10^{13}$ to $1.2x10^{13}$ cm^{-3}.

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The dashed line is the room temperature universal NMOS mobility (S. Takagi, et al., IEEE Trans. Electron Devices,Vol. 41 p. 2357, 1994). The symbols show the 77K NMOS mobility for the strained Si devices, illustrating a significant enhancement compared to the universal MOS mobility at that temperature.

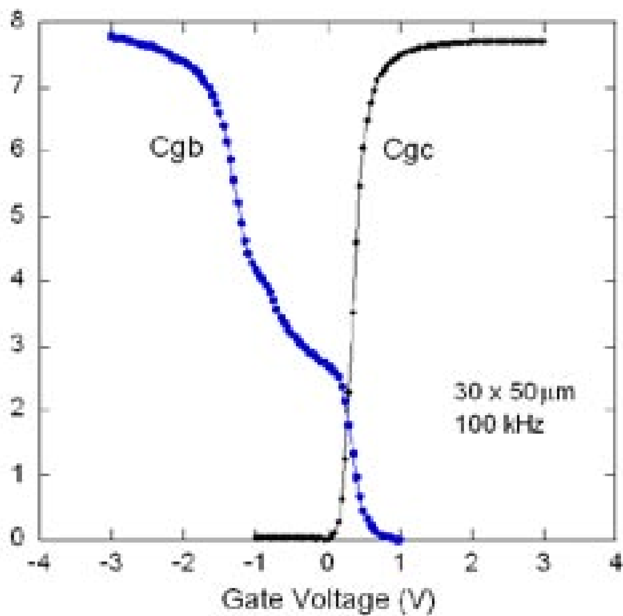

Fig. 15: Split-CV measurements of a strained Si n-MOSFET at room temperature.

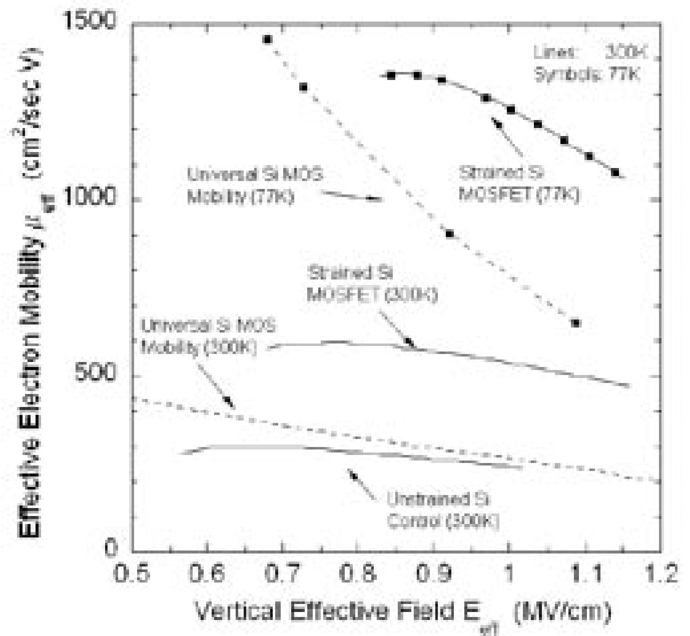

Fig. 16: Measured effective mobility versus vertical effective field for strained Si and unstrained Si control n-MOSFETs, at room temperature (lines). Symbols show the 77K data for strained Si and the universal MOS mobility curve.

Strained Si/SiGe-on-Insulator (SGOI) RF Power MOSFETs

Personnel

N. Waldron (J. del Alamo)

Sponsorship

DARPA

The rapid growth in wireless communication products in recent years has driven the development of RF technology. The implementation of the power amplifier function of these systems in the intermediate frequency range of 5-20 GHz has predominately been fulfilled by GaAs technology. Advancements in SiGe HBT may allow performance of up to 10 GHz depending on the power level of the application, but as of yet there is no current prospect for Si-based technology to operate in the >10 GHz range. This project pursues emerging strained Si/SiGe MOSFET technology to develop high performance RF power devices that can operate in the 10-20 GHz range at power levels of 100s of mWs. Such a device will rival the performance of GaAs technology but at a lower cost and with the potential for system-on-chip integration.

The basis for the superior performance of strained Si/SiGe MOSFET technology is that it exhibits an enhancement in the fundamental transport properties of Si resulting in improved device speed and power dissipation. The stress induced by the lattice mismatch between a thin layer of epitaxially grown Si on a relaxed SiGe buffer layer induces a strain that results in improved carrier transport through the thin Si film for both holes and electrons. Recent experimental work has shown increases of up to 80% in the low field mobility of n-MOSFETs. The incorporation of an insulator layer underneath the stack (as in SOI) offers the further benefits of lower capacitance and power dissipation.

A cross section of the proposed initial device structure is shown in Figure 17. An LDMOSFET design is used. The main features of the device are the lightly doped drain which enables a high breakdown voltage

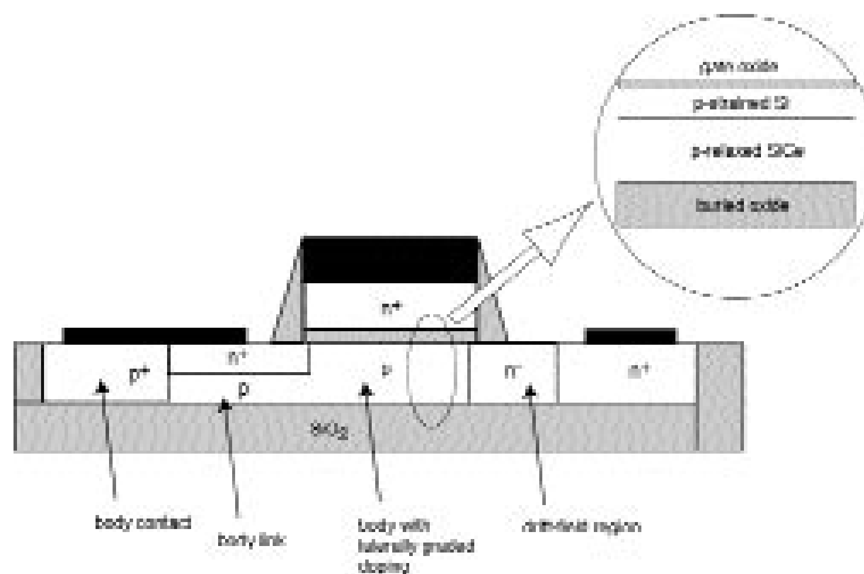

Fig 17: Schematic cross section of proposed strained-Si RF-power LDMOSFET. Inset shows the epitaxial layer structure

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and the graded body doping profile which results in a high transconductance. These two key features impact the trade off between the cut-off frequency fT and breakdown voltage of the device. A P^+ body contact is included to counteract floating body effects. The constituent layers of the epitaxial stack are also shown. The epitaxial structure consists of a SiGe relaxed buffer layer on top of which the thin strained-Si layer is deposited. This thin Si layer forms the active region of the device where the channel inversion layer is created. The gate oxide is grown on the strained-Si layer and the entire stack sits on a buried oxide forming what is termed an SGOI (Strained Si/Ge on Insulator) structure. The SGOI substrate is prepared by means of a Smart Cut process developed at MIT.

A simulation platform which will allow for design optimization is currently being developed using the MEDICI device design CAD tool. This modeling environment will be used to gain an understanding of the performance benefits/tradeoffs of various epitaxial layer structures. While strained Si/SiGe processing is entirely compatible with traditional CMOS fabrication techniques, it does present some potential technological challenges particularly for RF power applications. Therefore identification and evaluation of the key critical processing steps such as isolation, gate oxide formation and body doping drive in is presently ongoing.

Hydrogen Degradation of GaAs and InP High Electron Mobility Transistors

Personnel

S.D. Mertens (J.A. del Alamo)

Sponsorship

NTT, HRL

GaAs and InP High Electron Mobility Transistors (HEMTs) hold promise for ultra-high-speed photonics and millimeter wave power-applications. A major reliability concern in some of these devices is the shift of the threshold voltage that is observed when the devices are exposed to hydrogen. This can result into circuit malfunction. The goal of this project is to understand this reliability problem and find device level solutions to mitigate it.

Recent research at MIT has shown that H exposure results in the formation of TiHx in Ti/Pt/Au gates. This produces compressive stress in the gate, which generates a tensile stress in the heterostructure underneath. The resulting piezoelectric polarization charge in the semiconductor causes a threshold voltage shift. The reported experimental values of these shifts in InP HEMTs and GaAs PHEMTs seem contradictory. For GaAs PHEMTs, DVT is always positive and increases as the gate length, L_g, is reduced. In contrast, for long gate length InP HEMTs, DVT is negative and increasing in magnitude with decreasing L_g. At a certain L_g, however, there is a sign turn around and H-induced DVT becomes positive.

In this project, we are developing a model for H-induced piezoelectric effect in InP and GaAs HEMTs that explains this peculiar behavior of DVT and provides design guidelines for minimizing H sensitivity. Our modeling approach involves: i) performing two-dimensional mechanical stress simulations in typical heterostructures, ii) computing the resulting piezoelectric charge, and iii) estimating its effect on V_T. The figure shows the piezo-electric charge distribution that is induced in an InP HEMT by an expansion of its 1 mm gate. This calculation framework provides results that are consistent with the experimental measurements and illuminate the key dependencies of DVT on heterostructure design. They also explain the fundamental difference between GaAs and InP HEMTs.

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This work will allow us to better understand the impact of layer structure and gate design on the H-induced V_T shift in GaAs and InP HEMTs. Our ultimate goal is device design guidelines that minimize the H sensitivity of these devices.

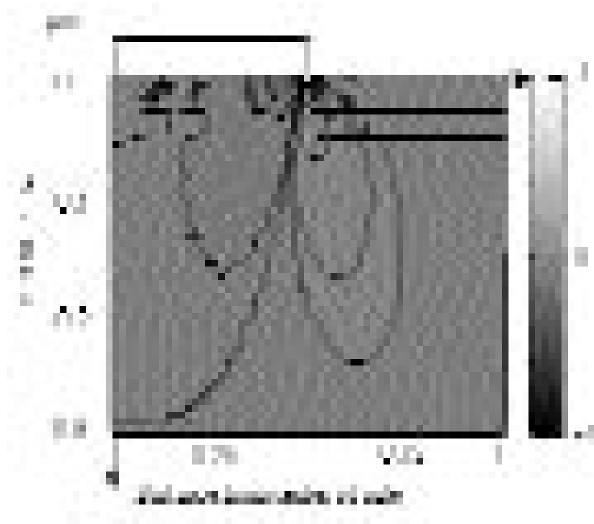

Fig. 18: Relative 2D piezoelectric charge distribution in a 1 mm InP HEMT stressed by an expanding gate. Only half of the device is simulated, as the other half shows a symmetric charge distribution.

Automatic Small-Signal Model Extraction for RF-LDMOSFETs on SOI

Personnel

J. Scholvin, J.G. Fiorenza (J.A. del Alamo)

Sponsorship

SRC

RF-power LDMOSFETs on SOI have great potential for system-on-chip integration. The use of SOI also results in lower parasitics and improved power efficiency.

For a device designer, it is important to understand how each element of a device influences its performance. For RF power MOSFETs, for example, the gate resistance is a very important parasitic and needs to be minimized. We have set up an infrastructure to automatically extract a small-signal equivalent-circuit model of RF-power LDMOSFETs. This has allowed us to isolate the influence of each model element and to evaluate the impact of changes in device design on performance.

To build a small-signal equivalent-circuit model that matches measured S-parameter data, it would be a poor strategy to fix the equivalent-circuit topology and then simply to try to optimize all parameter values. This is because of the large number of variables involved. Also, conventional equivalent-circuit model topologies optimized for bulk devices might not be suitable for SOI. Instead, our approach is to start with the most intrinsic model of a MOSFET, which captures the core device behavior, and then, once optimized, add new elements one by one with a strict sense of priority. It is very important, however, that every element that is added is physically meaningful.

For our SOI LDMOSFETs, we started with the very basic intrinsic model, indicated in Figure 19. The value of all elements of this model was derived from experimental Y-parameters. After this, the program tried all possible element additions and choose the one that gave the best improvement in the data fit. Several of these cycles of adding one element and optimizing followed, until the degree of improvement fell below a threshold at which the program stops. Figure 20 shows the result. As one can see, not only does the model match the experimental Y-parameter data very well,

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but the selected elements also capture all the important parasitics associated with the substrate and gate.
The approach demonstrated in this work will be instrumental in developing accurate device models and in understanding the connections between device design and device operation.

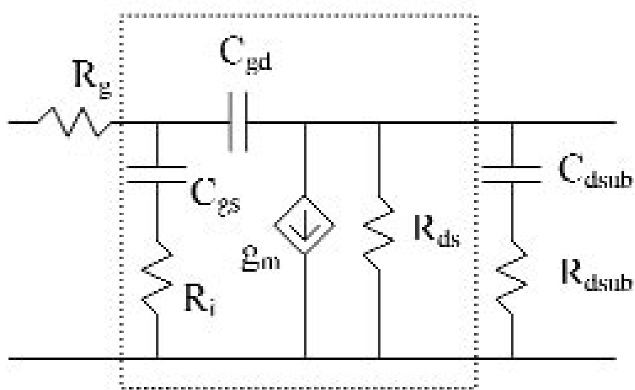

Fig. 19: Automatically derived small-signal equivalent circuit model for RF-power SOI-LDMOSFET. R_g captures the gate resistance and the C_{dsub}-R_{dsub} network represents substrate parasitics. The intrinsic model is marked by the box.

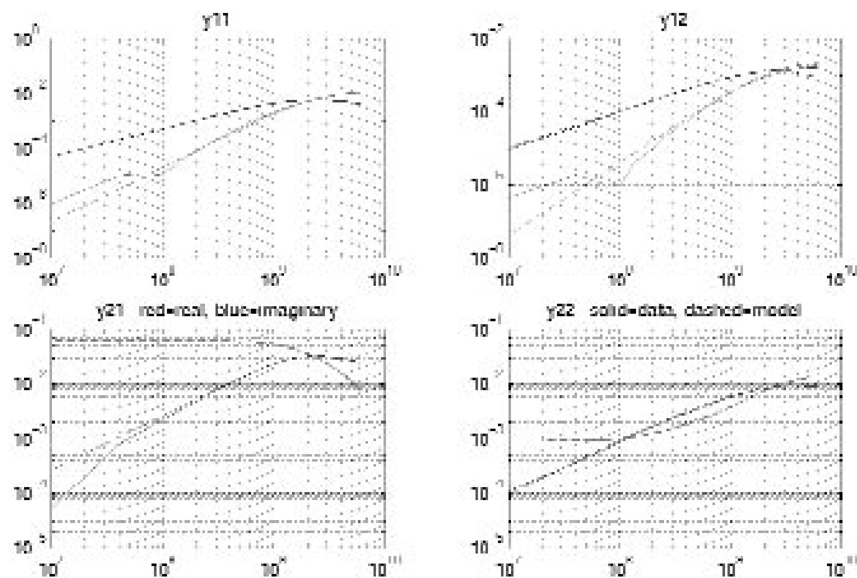

Fig. 20: Measured (solid) and simulated (dashed) Y-parameters of a 1 mm wide RF-power SOI LDMOSFET.

RF Power SOI LDMOSFETs for System-On-Chip Applications

Personnel

J. G. Fiorenza (J. A. del Alamo)

Sponsorship

SRC

Our research focuses on the development of a transistor technology for the RF power amplifiers of future generations of highly integrated wireless communication systems. We have developed an SOI (Silicon-on-Insulator) LDMOSFET (Laterally Diffused MOSFET) which is optimized for RF power amplifier applications and which is fabricated with a technology that permits its integration with CMOS into a single-chip wireless system.

A cross-section of the RF SOI LDMOS device that we have fabricated is shown in Figure 21. The device is a MOSFET that features several enhancements to give it superior RF power performance. To enhance its gain the body doping of the device is laterally graded. The lightly doped n-type drift region, combined with a body contact under the source, increases the device's breakdown voltage and its power handling capability. The insulating buried oxide layer reduces the parasitic drain capacitance and improves its high frequency power gain as well as the isolation between different devices on the same substrate. The device fabrication process has been designed to avoid exotic processing techniques so that it will ultimately be possible to integrate the power device process into a standard digital SOI CMOS process.

We have demonstrated that the performance of SOI LDMOSFETs can meet or exceed the performance of bulk silicon LDMOSFETs, which are widely used today in PA applications. Figure 22 shows the gain and efficiency of the devices as a function of the input power. Included in the figure are both SOI LDMOSFETs and bulk silicon LDMOSFETs that were fabricated in parallel using an identical process. The power efficiency of the SOI device exceeds the performance of the bulk device. Our research has shown that the origin of this is reduced interconnect and contact pad loss on the SOI substrate.

In summary, the RF SOI LDMOSFET is a promising

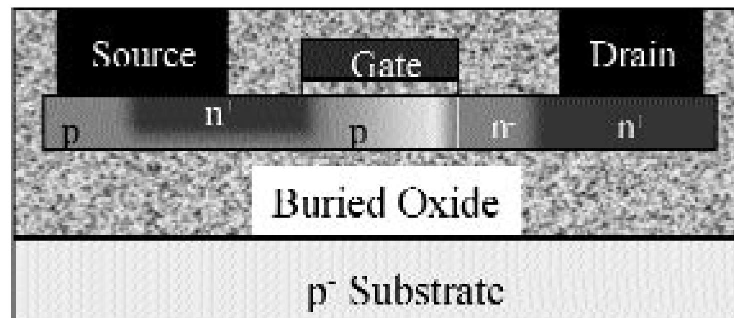

Fig. 21: An RF Power LDMOSFET on SOI

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technology for RF power amplifiers in future generations of highly integrated wireless systems.

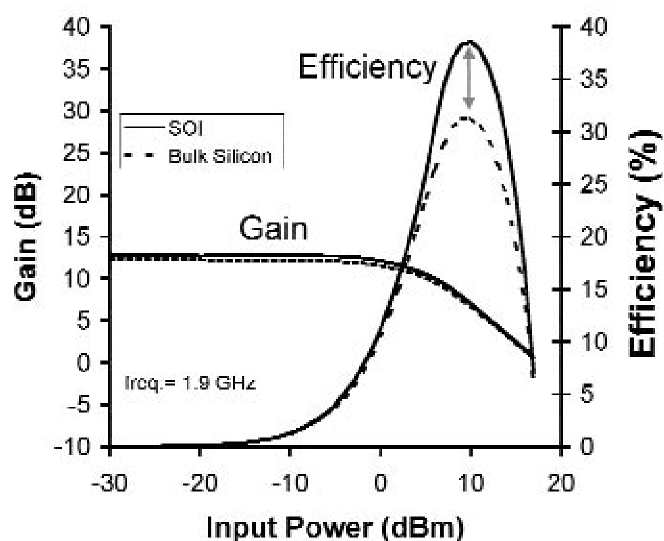

Fig. 22: RF Power Performance comparison between SOI and bulk-silicon LDMOSFETs fabricated at MTL.

Magnetic Random Access Memories (MRAMs)

Personnel

C.A. Ross, H.I. Smith, B. Vogeli, F. Castano, M. Walsh, Y. Hao, S. Haratani, in collaboration with J.Q. Wang

Sponsorship

TDK Corp., DARPA through U. of New Orleans

MRAMs are solid-state non-volatile magnetic storage devices in which each bit of data is stored an a small, elongated magnetoresistive sandwich element. A typical magnetoresistive (MR) sandwich consists of two magnetic layers of different coercivity, one hard and one soft.

The direction of magnetization of the hard layer is used to represent the data bit. To write data, a magnetic field is applied by passing a current through a conductor line (word line) adjacent to the element, such that the field is large enough to change the magnetization of the hard layer. To read, a smaller current is passed, which can change the magnetization of the soft layer only. The resistance of the element depends on whether the hard and soft layers are magnetized parallel or antiparallel, hence changes in the resistance resulting from the reversal of the soft layer can be used to probe the magnetic state of the hard layer. Elements are arranged in a rectangular array and connected with conductor lines, allowing individual elements to be selected.

We have used interference lithography combined with reactive ion etching and ion-milling to produce arrays of Co/Cu/NiFe spin-valve elements and prototype MRAM structures. The aim of this research is to investigate the behavior of sub-100 nm elements, much smaller than those used in present-day MRAM devices.

To tailor the properties of the pseudo spin valve (PSV) elements for MRAM devices, we analyzed the hysteretic behavior of large-area arrays of rectangular and elliptical PSV dots. Rectangular dots of sub-100nm width with aspect ratios ranging from 1:1 to 1:10 were fabricated by exposing and etching a first grating into an SiO_2-layer, and then spin-coating the sample with new resist and exposing a second grating of different period perpendicular to the first one. The hysteresis obtained from an array of 80x140nm PSV dots exhibits two distinct steps, as shown in the Figure 23, corresponding to the separate

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switching of the Co and NiFe layers. The switching of the two magnetic layers and their antiparallel alignment at remanence leads to the conclusion that the layered PSV-structure is preserved through the pattern transfer process. Upon increasing the aspect ratio of the PSV-dots, the magnetic field at which the soft layer switches to antiparallel alignment decreases and eventually the two magnetic layers align parallel at remanence, as required for MRAM devices.

In Fig. 24, an MRAM structure is shown. The PSV elements are located where the horizontal word lines and the nearly vertical sense lines intersect, sandwiched between the sense lines and a 30nm SiO2-insulation layer. The buried PSV elements form a large-area array of 80x180nm PSV dots, as indicated by magnetic measurements. Their magnetic behavior is similar to that of large-area PSV-dot arrays of the same dimensions. Both word and sense lines were found to be conductive.

Block copolymers consist of polymer chains made from

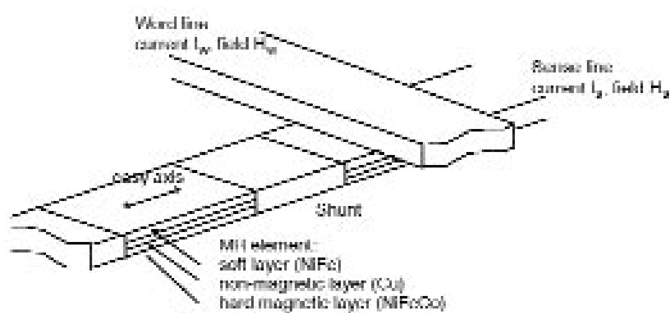


Fig. 23: Schematic of MRAM structure, which consists of an array of parallel sense lines and parallel word lines. The MR elements are connected in series. Magnetic fields generated by currents passed simultaneously through a sense line and a word line write the element at the intersection of the two lines. To read, resistance changes in the sense line caused by a smaller wordline current are measured.

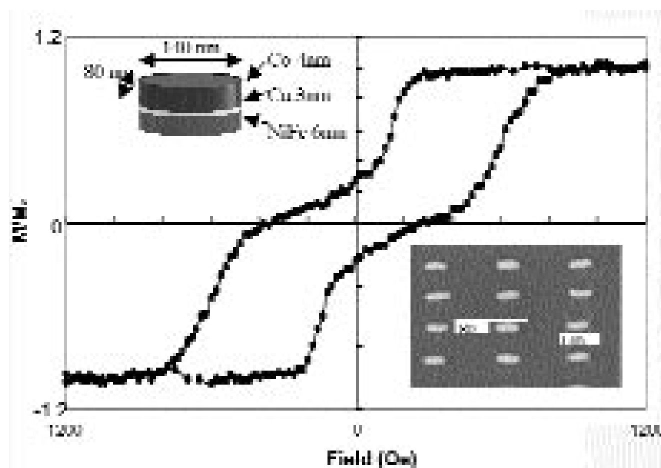


Fig. 24: Hysteresis loop of an array of 80 nm x 140 nm elliptical particles made of a Co/Cu/NiFe film. The steps in the loop correspond to the separate switching of the NiFe and Co layers, which are coupled antiparallel at remanence.

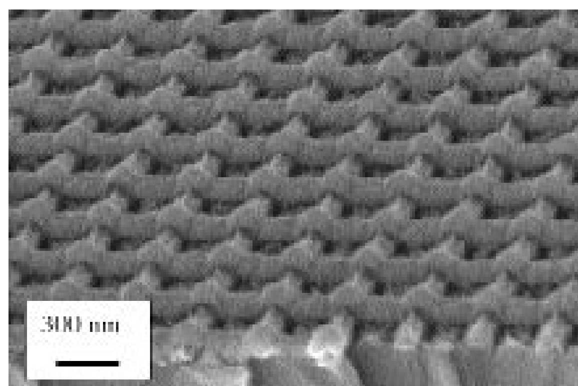


Fig. 25: Scanning electron micrograph of an array of PSV elements located at the intersection of the horizontal word lines and vertical sense lines.

Magnetic Nanostructures made by Block Copolymer Lithography

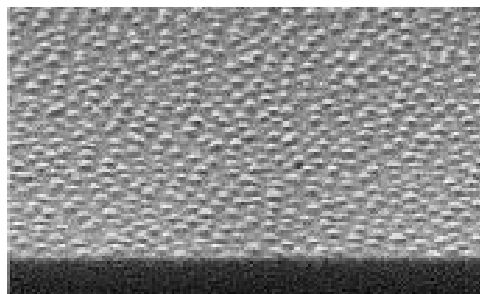
Personnel

C.A. Ross, J. Cheng, H. I. Smith, collaboration with E.L. Thomas

Sponsorship

National Science Foundation through a Seed Grant from the MIT Center for Materials Science and Engineering

two chemically distinct polymer materials. These can separate to form small scale domains whose size and geometry depend on the molecular weight of the two types of polymer and their concentration. The domains have a very uniform distribution of sizes and shapes. We have been using block copolymers as templates for the formation of magnetic particles, by selectively removing one type of domain and using the resulting template to form a nanostructured magnetic film. This can lead to hexagonally close packed arrays of magnetic dots or columns with diameters on the order of 20 nm and periodicities of order 50 nm. As an example, a block-copolymer has been used as a lithography template to ion-mill a thin magnetic film into a close-packed array of magnetic dots. Such materials are useful for studying the thermal stability, switching behavior, and interactions between magnetic particles that are smaller than can be obtained using conventional lithography techniques. They may also be useful in future generations of storage materials such as flexible media.



200 nm

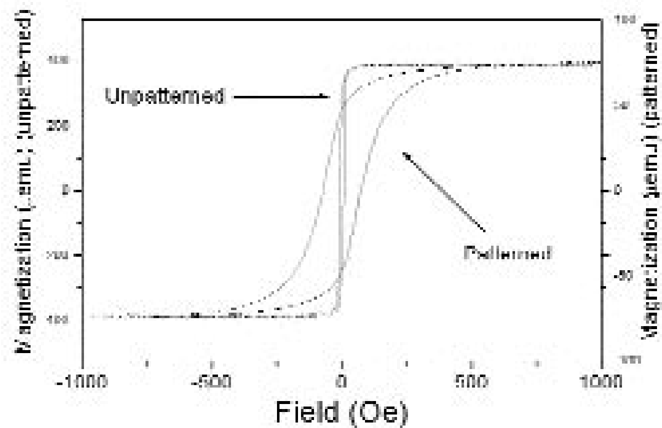


Fig. 25a: An array of Co dots, 8 nm thick and 20 nm in diameter, made by block-copolymer lithography. The array has a coercivity of about 100 Oe at room temperature.

Vertical MOSFET for Field Emission Applications

Personnel

P. R. Herz (A. I. Akinwande)

Sponsorship

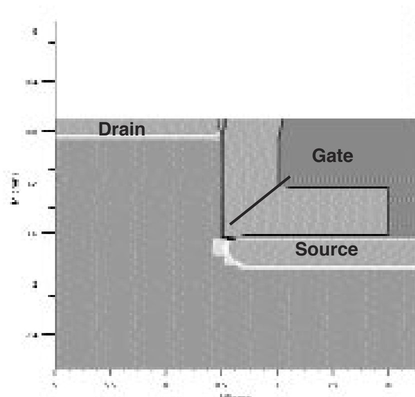
DARPA

As the pixel density of high-resolution electronic display increases, there is a corresponding increase in the I/O data transfer rate necessary to address the display. This ultimately reduces the row access time on the display for a fixed scanning refresh rate. To alleviate this problem, active matrix addressing is used in current display technologies. However, the I/O data transfer rate is still very high and leads to large power dissipation in the addressing circuits and system drivers.

A proposed solution to this issue is the use of intelligent pixel arrays whereby an actively addressed pixel retains on/off information within the pixel between frame scans. This reduces the necessary refresh rate if the actively on or off pixel state does not need to be modified on the subsequent picture frame. We are proposing to construct a field emitter array with an integrated transistor structure to form the basis of a pixel latch sub-system. Using an additional transistor to isolate the pixel latch element from the display row and column address lines, random addressing of each pixel latch element is possible. An additional benefit of an integrated transistor structure is stabilization of field emission current from the emitter arrays (FEA).

Using an integrated transistor structure, it is possible to modulate the field emission current density by adjusting the vertical MOSFET (VMOS) gate voltage. Because the VMOS is connected in series with the field emitter array the gate voltage of the FEA is divided between the drain to source voltage, VDS, and the gate to emitter voltage, VGE, of the FEA. This can be modeled as a voltage controlled current source with a floating drain voltage for the VMOS device. The floating drain voltage is then controlled such that the desired level of emission current is produced.

Other approaches that have been proposed for MOSFET/FEA structures have used lateral MOSFET designs integrated with field emitter arrays. While this is a very good device structure, higher packing density and thereby greater display resolution can be achieved with a vertically integrated MOSFET/FEA device. The device can be constructed such that the same voltage controls the VMOS channel and field emitter gate. Initial investigations into VMOS simulation and fab-



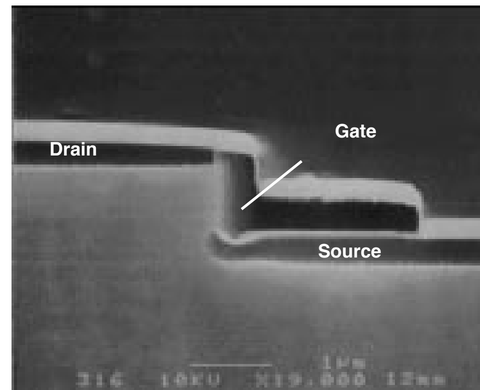


Fig. 26: VMOS doping profiles.

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rication has been completed. The process design has used vertically etched silicon pillars to create the VMOS structure for testing and analysis. Figure 26 shows VMOS source and drain doping profiles, indicating good agreement of simulation and experimental results. Top view SEM of the completed VMOS structure are shown in Figure 27. There was some concern regarding feature topology and gate oxide integrity however device testing yielded encouraging results. VMOS current-voltage characteristics were tested experimentally and are shown in Figure 28, indicating clear transistor behavior with a 2V threshold voltage and drive currents of 5-10mA for a given VMOS array (100 transistors per array).

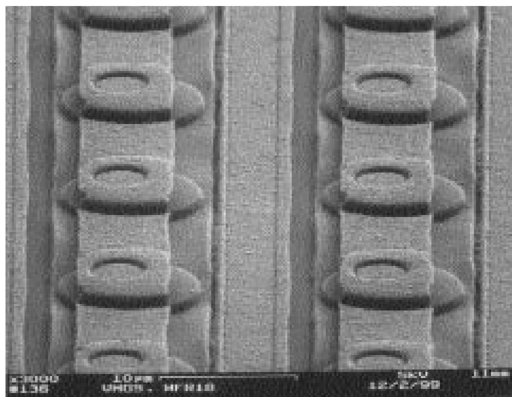

Fig. 27: VMOS array. Fabricated device (top view).

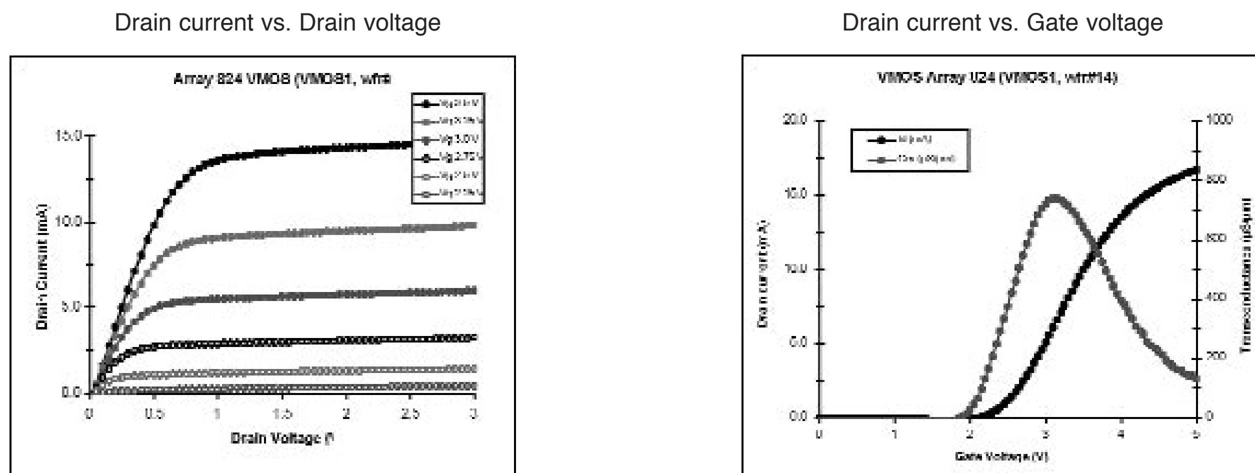

Fig. 28:VMOS experimental I-V characteristics.

Field Emitter Array Flat Panel Displays for Head-Mounted Applications

Personnel

D. Pflug (M. Schattenburg, A. I. Akinwande,H. I. Smith and C. Bozler)

Sponsorship

MIT Lincoln Laboratory

Advances in nanostructure technology have made feasible small, high-resolution, high-brightness and high-luminous-efficiency field-emitter-array sources for Head-Mounted Displays (HMDs). HMDs are expected to have a variety of applications in military, medical, commercial and entertainment fields. The technology most commonly used in deployed HMD systems is the CRT which is bulky, because of the use of a single electron gun to generate images on a cathodoluminescent screen, but has the most desirable attributes of high luminous efficiency, high brightness and easy image rendition. However, the relay optics required for see-through HMDs become complicated because of the bulky nature of the CRT. For other applications, such as entertainment virtual reality, the most commonly used image source is the backlit Active-Matrix-Liquid-Crystal Display (AMLCD), which is thin and has high resolution. Furthermore, the addressing electronics are integrated on the same substrate as the image source. However, the backlit AMLCD image source does not have sufficient brightness nor luminous efficiency to make it suitable for application to see-through HMDs.

Our approach to demonstrating a small, high-resolution, high-luminous-efficiency and high-brightness display is the field-emitter-array Flat-Panel Display (FED) which incorporates a high-density, high-performance array of low-voltage field emitters. CMOS-controlled electron emission from the tips impinges on a cathodoluminescent screen. It is thus possible to integrate the addressing and signal conditioning electronics on the same substrate as the Field Emitter Arrays (FEAs). The main advantage of this approach is the reduction of the number of wires and bond pads from about 2,000 to about 50. For example, it will be difficult to attach > 2,000 wires to bond pads in an area of 1.5" x 1.5" and obtain ultra-high vacuum in the display envelope. High resolution (>1000 dpi) FEDs are only possible if the addressing/driver and other signal conditioning electronics are integrated on the same substrate as the field emitter arrays.

Our initial objective is to demonstrate the integration of Si CMOS technology with low-voltage field-emitter arrays fabricated using interferometric lithography. This project requires the fabrication of Si CMOS wafers with one or two levels of metal interconnect, followed by surface planarization using CMP technology. Interferometric lithography is then used to define Mo-cone field emitter arrays that are spaced 200 nm tip-to-tip and have <50 nm gate-to-emitter separation. Fabricated cone-field-emitter arrays with a 320 nm period have demonstrated emission currents of 1 mA at a gate voltage of 20V from 900 cones in a 10 mm x 10 mm area. This current is more than adequate for a brightness of 1000 fL at a screen voltage of 500V.

Our initial efforts focused on modeling the scaling behavior of FEA devices. Numerical simulation and computer models to predict FEA performance have been developed and continue to be refined. These models allow us to obtain a correlation between different device geometries (cone tip radius or curvature, gate aperture, etc.) and the emitter's output characteristics. The results of this study have directed our fabrication efforts toward devices whose performance will not only be better, but more dependent on geometries that can be well controlled in the manufacturing process. Simulation results indicate that we will be able to increase the current density and reduce the operating voltage, by decreasing the tip-to-tip separation to 200 nm.

FEAs of 200 nm period have been fabricated by using interferometric lithography and standard processing techniques. Additional metallization layers and conventional lithography were used to create discrete Molybdenum Spindt arrays for electrical characterization. Standard CMOS processing techniques have been also been combined with the interferometric lithography to form 200 nm-period arrays of Si etched cones.

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A semi-automated Ultra High Vacuum (UHV) probe chamber has been developed for the electrical characterization of FEAs. This test bed allows the performance of the arrays to be evaluated without the lengthy overhead of vacuum packaging devices. Device performance has been shown to be not only dependent on the device physical structure, but also on surface contamination that may have resulted during fabrication and MEMS processing. The UHV probe chamber has the capability to do device conditioning including ECR plasma cleans and wafer bake-out. The system is designed to allow the future expansion to include surface analysis chambers including a Kelvin Probe, Scanning Maxwell Microscope and Auger.

Electrical characterization of the 100 nm-aperture Molybdenum arrays (200 nm tip-to-tip spacing) has shown that arrays can operate at voltages as low as 16 volts and provide adequate current to support flat panel display applications. We have demonstrated initial testing of low-gate-voltage FEAs with discrete solid state devices. We replace the resistor that previous approaches have used to limit and control emission current with a MOSFET. Current control is critical to the uniformity of brightness across the display because Fowler-Nordheim emission depends exponentially on the ratio of the gate voltage to the tip radius-of-curvature (Vg/r). It is therefore very sensitive to small changes in the radius-of-curvature. It was possible to control the emitted current density using the gate voltage of the transistor load. This may enable analog voltage gray scale or temporal gray scale.

The above demonstration has gone a long way to show the feasibility of high brightness, high-resolution FEA image sources for head-mounted displays.

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Opposite Page:

Example of a ratchet potential. The particle sitting on the well requires less force to move through the first peak to the right than to move to the left. Therefore, there is a preferred direction of motion.
Courtesy: K. Segall, E. Trías, J. J. Mazo (T.P. Orlando).
Research sponsored by NSF.