
*Opposite Page:
Process Engineer at wafer cleaning station (TRL).*

Microsystems Technology Laboratories



MIT Microsystems Technology Laboratories (MTL)

Organization and Administration

Background

MIT's Microsystems Technology Laboratories (MTL) was founded in the early 1980s to provide a complex of modern microelectronics fabrication laboratories, ultraclean rooms, and materials processing facilities. At the present time, MTL is as an Interdepartmental Laboratory of the Institute reporting to the Dean of the School of Engineering.

Mission Statement

MTL's primary mission is to enable research through the support of an intellectual and physical environment that makes possible education through teaching and research in areas that require or that may benefit from microelectronic/microfabrication technology. The microfabrication, test, and computational facilities of the MTL are open to the entire MIT community and researchers from other university or government laboratories.

The facilities of the MTL consist primarily of clean-room microfabrication laboratories plus associated design, simulation, testing, and characterization equipment and expertise, as well as an extensive computer network.

Over the period of its existence, the MTL has committed significant resources to the maintenance and acquisition of capital equipment. These capital improvements, upgrades, and purchases allow us to serve an increasing user base, to decrease experiment turn-around (cycle) time resulting from lowered equipment "down-time". At the present time the MTL is embarking on a major capital program (~\$10.8M) that will upgrade our process facilities from 100-mm to 150-mm substrates. This plan is supported through industrial funding and equipment donations, institutional funding, and the MTL reserve fund.

Administrative Structure

MTL is administered through the Office of the Director, Professor Martin A. Schmidt, who has overall responsibility for the operations of the MTL. Reporting to Professor Schmidt is Mr. Samuel Crooks, MTL Assistant Director for Administration and Administrative Officer. Reporting to Mr. Crooks are a Fiscal Officer, Contract Administrator, Liaison Coordinator, Executive Assistant, Fiscal Assistant, and Account Assistant. Mr. Crooks and his staff maintain responsibility for the non-technical operations of the MTL. Also reporting to Professor Schmidt is Ms. Anne Wasserman, who provides direct administrative support as Assistant to the Director.

Fabrication Facilities

MTL technical resources are managed by a professional technical staff. MTL facilities are open to all MIT faculty and students as well as users from other academic institutions and government agencies. Directly reporting to Professor Schmidt, is Dr. Vicky Diadiuk, MTL Assistant Director, who manages the day-to-day technical operations of the MTL. Dr. Diadiuk has a staff of seven research engineers and seven research technicians.

Researchers planning to utilize the process facilities of the MTL submit an application to Dr. Diadiuk describing their process. The Process Technology Committee (PTC), made up of faculty, students, and technical staff, reviews the process to ensure that it does not compromise or contaminate any of the tools. The PTC may recommend alternative process steps or disallow certain uses of materials, etc. Once the process application has been approved, users may begin utilizing the labs. First time MTL users are required to successfully complete a safety and orientation course prior to their use of MTL facilities and must receive training from a research specialist for each piece of laboratory equipment they plan to operate.

MTL also maintains a comprehensive Computation Infrastructure, providing a broad array of services to the community. Professor Duane Boning (Electrical Engineering), MTL Associate Director has responsibility for this activity. Users of MTL's fabrication facilities interface with the MTL's Computer Aided Fabrication Envi-

continued

ronment (CAFE) to perform their processes (e.g., reserve machines). The user log is coupled to a sophisticated charging algorithm which calculates a user fees on a monthly basis.

Policy recommendations within the MTL are developed by a working group made up of Professor Martin Schmidt, Professor Duane Boning, Dr. Vicky Diadiuk and Mr. Samuel Crooks and with significant input from the faculty who make up the MTL. Recommendations from this working group may be presented to faculty during a weekly luncheon (Microlunch), or may be brought to the MTL Faculty Policy Board. Twice annually policy issues and decisions are reviewed with the MTL Microsystems Industrial Group Advisory Board, whose members represent MTL's sponsor companies, and who provide advice and counsel on issues concerning the operations and research directions of the MTL.

Personnel involved in ongoing research activities at the MTL include over 60 faculty, 18 senior research staff, 300 graduate students, 150 undergraduate students, 20 postdoctoral associates, 15 visiting scientists, 60 research affiliates, 28 technical support staff, and 23 administrative and support staff. During the 1998-1999 academic year, 30 Ph.D. and 30 S.M. and M. Eng. degrees were awarded in conjunction with research activities whose primary area of focus was microelectronics and which were strongly coupled to the facilities of the MTL.

For information regarding MTL's technical operations and capabilities, contact Dr. Vicky Diadiuk, MTL Assistant Director, Operations, telephone (617)253-0731, e-mail diadiuk@mtl.mit.edu. For information regarding MTL programs and other general information, please contact Mr. Samuel Crooks, Assistant Director, Administration, telephone (617)253-3978, e-mail crooks@mtl.mit.edu. You may also wish to visit our Web Site at: <http://www-mtl.mit.edu/mtlhome/>

The following page provides and organizational chart for those personnel (other than faculty) whose appointment is administered through the Microsystems Technology Laboratories.

Personnel

continued

Microsystems Technology Laboratories (MTL) - Administrative Service

The Microsystems Technology Laboratories (MTL), which include the Integrated Circuits Laboratory (ICL) and Technology Research Laboratory (TRL), are managed by the MTL Director, Professor Martin Schmidt, Electrical Engineering and Computer Science.

Administrative Staff and Personnel

S. Crooks, Assistant Director, Administration, and Administrative Officer

D. Goodwin, Fiscal Officer and Grant and Contract Manager

P. Burkhart, Billing Manager

C. Gordy, Liaison Coordinator

A. Wasserman, Assistant to the Director

D. Hodges-Pabon, Executive Assistant and MTL VLSI Seminar and Memo Series Coordinator

C. Mokalled, Account Representative

K. Nici, Account Representative

Fabrication Facilities Staff and Personnel

Dr. V. Diadiuk, Assistant Director, Operations, Principal Research Engineer

M. Karapetian, Clerical Assistant

Fabrication

P. Tierney, Research Specialist, Operations Supervisor

D. Adams, Project Technician

J. Bishop, Senior Technician

J. DiMaria, Project Technician

W. Price, Technician A

R. Stoute, Technician A

J. Mathias, Technician B

Diffusion, Device Characterization and Process Control

B. Alamariu, Research Engineer

Vacuum Etching

J. Walsh, Research Engineer

Vacuum Deposition

P. Zamora, Research Specialist

TRL Processes

K. Broderick, Research Specialist

Facilities

P. McGrath, Research Specialist

Equipment Maintenance

D. Sullivan, Research Specialist

continued

Personnel

continued

Computational Facilities Staff and Personnel

D. Boning, Associate Professor,
Electrical Engineering and Computer Science,
Associate Director,
Computation and Information Systems

D. E. Troxel, Professor,
Electrical Engineering and Computer Science,
Technical Advisor,
Computation and Information Systems

T. Lohman, Research Specialist,
System/CIM Manager

T. Wingard, Research Specialist,
System/CAD Manager

M. Hobbs, Research Specialist,
System Manager

Operating Committees

Process Technology Committee (PTC)

A. Akinwande, Associate Professor, EECS
J. del Alamo, Professor, EECS
V. Diadiuk, MTL Assistant Director,
Operations (Chair)
J. Lang, Professor, EECS
J. Hoyt, Associate Professor, EECS
D. Chen, Ph.D. Candidate, EECS
M. Currie, Ph.D. Candidate, Mat. Sci.
A. Luan, Ph.D. Candidate, Mat. Sci.
A. Ritenour, Ph.D. Candidate, EECS

Computer Systems Committee

D. Boning, Associate Professor, EECS (Chair)
A. Chandrakasan, Associate Professor, EECS
L. Frechette, Ph.D. Candidate, EECS
V. Gutnik, Ph.D. Candidate, EECS
T. Lohman, System/CIM Manager
A. Ritenour, Ph.D. Candidate, EECS
C. G. Sodini, Professor, EECS
D. E. Troxel, Professor, EECS
M. Varghese, Ph.D. Candidate, EECS
T. Wingard, System/CAD Manager

MTL Faculty Policy Board

D. Antoniadis, Professor, EECS
D. Boning, MTL Associate Director and,
Associate Professor, EECS
A. Epstein, Professor, Aero/Astro
K. Gleason, Professor, ChemE
L. Kolodziejski, Professor, EECS
M. Schmidt, MTL Director, and
Professor, EECS (Chair)
C. G. Sodini, Professor, EECS
S. Crooks, Assistant Director (ex-officio)
V. Diadiuk, Assistant Director (ex-officio)

continued

Research Laboratories and Facilities

The Microsystems Technology Laboratories (MTL)

MTL is located in the Gordon Stanley Brown Building (Building 39). Administratively, the MTL is an Interdepartmental Laboratory of the Institute reporting to the Dean of the School of Engineering. In accordance with the multidisciplinary nature of microsystems technology, the faculty, staff, and students using MTL are affiliated with the many schools, departments, and centers of MIT.

The following is a brief description of the MTL research facilities:

The Integrated Circuits Laboratory (ICL)

7,910 sq-ft integrated circuit fabrication facility comprised of:

- 2,800 sq.-ft Class 10 clean space
- 4,000 sq.-ft support space
- 460 sq.-ft characterization space
- 650 sq.-ft electrical testing and parametric characterization (ICs and devices)

The Technology Research Laboratory (TRL)

3,600 sq-ft of laboratory space comprised of:

- 2,200 sq.-ft class 100 clean space
- 1,400 sq.-ft support space

The Exploratory Materials Laboratory

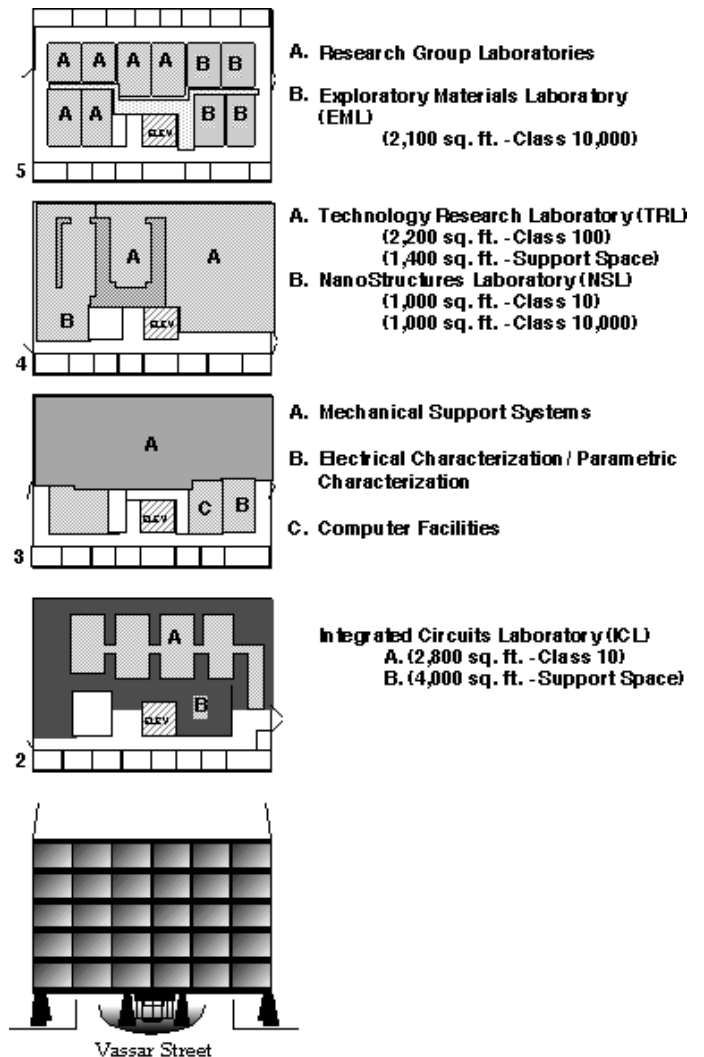
- 2,100 sq.-ft class 10000 clean space

The Research Group Laboratories (RGL)

3,000 sq-ft of laboratory space divided into six laboratory rooms assigned to individual research groups who are the principal users of ICL, TRL, EML, and the NanoStructures Laboratory (NSL).

An additional 4,000 sq-ft of MTL office and laboratory space are located adjacent to Building 39 in Building 38.

Gordon Stanley Brown Building (Building 39) Microsystems Technology Laboratories



continued

Research Laboratories and Facilities

continued

MTL Fabrication Laboratories

Process research and device fabrication at MTL are primarily conducted in two laboratories, the Integrated Circuits Laboratory (ICL) and the Technology Research Laboratory (TRL). The ICL is designed, equipped and staffed to serve as a highly advanced silicon integrated circuit, device, structures, and process research facility. The laboratory houses a complete four inch silicon IC fabrication line. Cassette-to-cassette transfer techniques are employed extensively, and VLSI discipline is maintained throughout the facility.

The TRL has two primary functions:

- To support the development of novel process technologies
- To provide facilities for the fabrication of novel circuits and microstructures

The TRL and ICL are complementary laboratories. Since the ICL is designed to permit fabrication of complex integrated circuits and devices, by necessity it must be operated under the strict discipline that is required for state-of-the-art silicon device and circuit research. The TRL is designed to make up for any loss of flexibility that this discipline imposes. Similarly, fabrication of devices in the ICL can readily take advantage of new technologies that have been developed in the TRL. Examples of such technologies include a titanium silicide process and low temperature Si/Ge epitaxial growth. The Class 100 clean room environment and clean room procedures employed in the TRL assure that wafers can move between the ICL and TRL without compromising either the wafers or the facilities.

Over the period of the past twelve months we have committed significant resources to the maintenance and acquisition of capital equipment. These capital improvements, upgrades, and purchases allow us to serve an increasing user base, to decrease experiment turnaround (or cycle) time resulting from lowered equipment

“down-time”, and to integrate new or improved process technologies or capabilities into the facility. During the past year several major tools were added to the facilities, and are now on-line and in full use.

We are continuing with our plan to convert the labs from 4" to 6" wafer diameter. This conversion will allow us to improve our process capabilities and will return us to compatibility with nearby fabs at Lincoln Lab and Analog Devices. To this end, we received two major equipment donations whose installation in ICL was completed in 1999: an Applied Materials Endura Metal Deposition cluster tool and Centura high-density plasma oxide etch system; both are capable of processing 6" wafers. The Endura will satisfy our post-conversion metal deposition needs. The Centura, donated jointly by Motorola and Applied Materials, complements our present etch capabilities. Several research groups have expressed interest in using these machines, and are doing collaborative work with the donors. The installation in ICL of the LAM Rainbow metal etcher donated by Advanced Microdevices (AMD) is scheduled to be completed as we achieve the full 6" conversion. In late 1999, we received a substantial donation from Intel that included 6"-capable Thermco furnace banks and a Nikon i-line stepper, whose installation in ICL is in progress. We also replaced an aging Karl-Suss mask aligner with an EV650, infrared-equipped mask aligner, and added a second STS deep trench silicon etcher; both of these tools contributed significantly to increased through-put in TRL.

MTL has continued to serve the microfabrication needs of the MIT community, working on projects from an ever-larger variety of academic departments (e.g., Biology, Chemical Engineering, Mechanical Engineering, Physics). As a result, lab activity continued to increase, as evidenced by both the number of students using the labs, and the amount of processing carried out. Once

continued

Computation and Communications

more, the Process Technology Committee served MTL well in carefully scrutinizing the increasing variety of new processes submitted, to ensure the integrity of all processes.

As indicated on the building schematic on the previous page, the building also houses the critical support facilities required to maintain the clean room conditions stated and provide for leading-edge process-related research. These include an air handling and conditioning system capable of maintaining the class 10 or 100 conditions at a temperature of $70 \pm 1^\circ\text{F}$. Liquid gas sources (nitrogen, oxygen, and argon) are used to supply ultrapure gases to the laboratories; ultrapure hydrogen gas is also supplied from a central source. The building also houses a sophisticated Deionized (DI) water system and a modern waste water treatment plant. The DI water system capacity was increased in 1997 from 20 to 100 gpm of 17 M-ohm water and the total organic compounds reduced by an order of magnitude to 2ppb. The waste water treatment plant is monitored for full compliance with state and Federal environmental rules. The MIT administration provided support for these upgrades as well as funding for the cleanroom expansion necessary to accommodate the tools donated towards the 6"-conversion.

Data communication is essential to any modern laboratory. An extensive data communications network is installed in the Gordon Stanley Brown Building. The entire building is also served by a high-speed ethernet connected to the MIT computer network, and consists of a fiber optic backbone for the major subnet with multiple dedicated 10 Mb/second ethernets for each floor and major computer server. Terminals and workstations connected by way of these facilities can access the central computers in the building and, through a series of networks, computers all over the MIT campus as well as in universities, government, and industry throughout the United States and abroad.

MTL Baseline Process

An "enhancement-compatible" 1.5 μm twin well CMOS process is run continuously in the ICL. This baseline process serves three functions: First, it provides a full process monitoring function for the Integrated Circuits Laboratory. Second, it is the starting point for more complex processes such as BiCMOS, or CCD/CMOS to fabricate circuits and systems with technology innovation. And third, the unit processes may be used to synthesize new process flows from simple devices, such as NMOS and PMOS capacitors and transistors, to novel micro-mechanical structures. A complete description of the baseline process ("Twin Well CMOS Process"), including process flow, process simulation results, layout rules, typical electrical parameters, etc. is available to all MTL users.

In order to understand the engineering trade-offs made in the design of the baseline CMOS process, a brief description of the philosophy which governed our decisions is necessary. The baseline process must serve as a good overall facility monitor, must be enhancement compatible, and be optimized for analog circuit and system design. Conservative design rules and device design were employed to ensure a high probability of successful runs in a reasonable turnaround time. The conservative nature of the process design is necessary for it to serve as a useful facility monitor.

It is important that the baseline CMOS process be enhancement compatible so that new technology innovations can be tested in a real integrated circuit process. In order to accomplish this task, the process was designed modularly such that coupling between unit process steps was minimized. This dictated the choice of a Twin Well CMOS Process which allows the possibility of choosing either p- or n-type starting material, since the epitaxial layer in which the devices are fabricated is extremely lightly doped. N- and p-wells are implanted into the lightly doped epitaxial silicon to form the regions where n- and p-channel devices are individually optimized. Another

key to enhancement compatibility is to use separate masked implants for field regions, channel regions, and source- drain regions of the n- and p-channel devices. This allows for future additional optimization of the n- and p-channel devices individually.

Along with serving as a process monitor and being enhancement compatible, the baseline process was optimized for analog circuits and systems. Optimizing for analog applications led to somewhat different oxide thickness, junction depths, and well depths, than a conventional 1.5 μm CMOS process optimized for digital applications. Lightly doped wells are important to reduce the body effect of n- and p-channel transistors which makes the use of deep wells and thick lightly doped epitaxial silicon necessary. The gate dielectric thickness was chosen to be thinner than a conventionally designed 1.5 μm CMOS process, since thin gate dielectrics increase the transconductance and the output impedance, while reducing the flicker noise and thermal noise of the devices. Finally, the threshold voltages of both the n- and p- channel devices were designed to be greater than 0.7 volts such that dynamic charge storage necessary for MOS analog circuit design can take place.

The baseline process is run by the staff on a regular basis. A special structure, the "Defect Array", is used to track and evaluate the defect density in the baseline process as part of our defect monitoring program. The structure employs a foundation based on a content addressable memory cell. It consists of a 16K, an 8K, and two 4K memories (similar to a random addressable memory) per die; the cell size is 25 x 46 μm . The structure has been modified to permit measurement of metal - metal shorts, metal - substrate shorts, metal - polysilicon shorts, polysilicon - polysilicon shorts and polysilicon - substrate shorts. In addition, a standard MTL "drop-in" pattern is included on each die which contains standard parametric test structures to evaluate critical device and process parameters, such as gate and

continued

field threshold voltages (n- and p-channel devices), polysilicon and diffusion sheet resistance, various contact resistances, transconductance, etc. The “drop-in” pattern is described in the “Twin Well CMOS Process” document in more detail. The results of these measurements, as well as other in-process measurements used to characterize and monitor the process, are available to all users.

Process Development/Consultation

The MTL staff is available to assist users in developing new processes or process steps. This assistance ranges from casual consulting on a process problem, to joint user/staff development activities, to a staff-performed effort guided by the user. In addition, the staff frequently will develop new processes or unit steps which are deemed to be useful to the majority of the user community. Recent examples include the development of a nitrous oxide-based thin gate oxide process, CMP planarization, and several reactive ion etch/plasma etch processes both in Si and compound semiconductors.

In addition to these services, the staff is available to assist in a processing sequence defined by the user. This assistance ranges from performing a particular unit step or series of steps, all the way to processing an entire lot to completion. This can be done with the user’s involvement and direction, or completely independently, in which case the completed lot is delivered to the user for evaluation.

A library of standard process recipes is maintained and checked routinely. These recipes include those used in the baseline process, and many more in the diffusion, oxidation, etch, photolithography and metallization areas. These documented steps greatly simplify and shorten the process development cycle, since frequently a new process can be “developed” by combining a series of these unit steps. Often, however, it becomes necessary to develop a new step or series of steps, or to employ materials, procedures or techniques not previously used in MTL. If a user encounters this situation, the proposed process must be submitted to the Process Technology Committee (PTC, composed of three faculty members, three to five student or postdoctoral users, and the Assistant Director of Operations) for review and approval prior to proceeding. This procedure has been adopted to insure that a.) no materials are inadvertently introduced into the facility which would compromise the research of other users, and b.) to guard against the

Training

possibility of machine use in a parameter range which might prove harmful to the equipment or the user. The PTC meets weekly to ensure rapid response to requests for new process activities.

The MTL staff provides training to all new users of the facility to ensure safe and competent operation of MTL equipment. This training begins with a half day orientation session, in which the user is introduced to MTL facilities, policies and procedures. Safety is stressed at this session, which includes proper procedures and techniques for handling the various acids, solvents, and gases employed in the facility, as well as a description of the alarms and various other systems that enable MTL to operate safely. Proper clean room procedures and techniques are also covered, as is a demonstration of CAFE, the computer system used to operate and monitor MTL facilities.

Following the orientation session, individual training and instruction is given on each piece of equipment required by the user in his/her research project. The training consists of a series of "hands-on" sessions and continues until the user is comfortable with the equipment and the staff member is convinced that the user can safely and effectively operate the piece of equipment in question. Standard Operating Procedures are available for each piece of equipment, so users can refer to them conveniently.

MTL Services

continued

Mask Making Service

MTL discontinued its mask-making service in 1998. In its place, users are referred to commercial providers with whom MTL staff has worked out convenient file transfer procedures. This change has been well-received by users since costs are similar and turn-around time is often shorter. The equipment in the mask room has been decommissioned or transferred to other areas of the labs.

Semiconductor Information Services

The Microsystems Technology Laboratories provides electronic information resources to the semiconductor research community by way of the World Wide Web. These services include extensive information about the people, facilities, and research of MTL. In addition, MTL makes available and coordinates access to information of value to the larger semiconductor community.

MTL-specific information is available at www-mtl.mit.edu. Through this page, one can

- Learn about the students, staff, and faculty associated with MTL
- Scan the facilities and equipment in MTL
- Find a detailed list of equipment and the cost of using it
- Read standard operating procedures for most machines
- See updates to the MTL VLSI Seminar Series schedule
- Keyword search through on-line versions of the MTL Annual Report
- Learn more about MTL research programs
- Link to additional research organizations at MIT

The "University Microfabrication Laboratory Network" (or Labnetwork) page is an informal focal point for discussion on topics of mutual interest to research and teaching microfabrication facilities. Records of past meetings and an archive of the labnetwork@mtl.mit.edu mailing list can be found at www-mtl.mit.edu/labnetwork/labnetwork.html.

Finally, the "Semiconductor Subway" provides links to semiconductor and microsystems-related information, including: fabrication facilities, technology, computer-aided design, manufacturing, microelectro-mechanical systems, professional societies and other organizations and a spectrum of other information. This page is highly popular, and has been averaging nearly 2,000 accesses per week. It can be accessed at www-mtl.mit.edu/semisubway.html.

Equipment

Integrated Circuits Laboratory (ICL)

Lithography

- Wafer Stepper
GCA Corporation Model 6300 DSW
- Photoresist Coater Developer
SVG 8860
- Bake Oven/Vapor Prime
Yield Engineering Systems, Inc., Model 3/10
- Photoresist Stripper
Matrix 106 Plasma Asher
- Inspection Microscope
Nikon OPTIPHOT 88
- Polyimide Coater
MTI Flexi Fab
- Wet Chemical Process Station (2)
Semifab Inc., Model WPS-400
- Wet Chemical Process Station
Semifab Inc., Model WPS-800

Diffusion, Oxidation, and Chemical Vapor Deposition

- Furnaces
BTI Engineering Corp./Bruce Systems
Bruce BDF-4 Furnace Systems
(4 atmospheric tubes, 4 LPCVD)
Bruce Series 7800 Gas Control Systems
Bruce Model 7351C DDC Microcontroller
APEX Data System

Thermco 10K 4 Furnace Systems
(4 atmospheric tubes, LPCVD)
installation in progress
- Vertical Thermal Reactor
SVG/Thermco 7000 Series
- Suspended Loading System
Heraeus-Amersil, Inc. SLS-125 Diffusion
- Gas Cabinets
Veriflow Corp. Toxic Gas Delivery Systems
- Wet Chemical Process Station
Semifab Inc. Model WPS-400
- Tube Cleaner
Reynolds Tech
6" Horizontal Quartz Cleaning System
- Toxic Gas Monitor
MDA Scientific, Inc. PSM-8e & 16 Multipoint
Monitoring Systems
- Rapid Thermal Annealer
AG Associates Heatpulse 410
- Surface Charge Analyzer
Semi Test SCA

continued

Equipment

continued

Integrated Circuits Laboratory (ICL)

Metal and Dielectric Deposition

- Electron-Beam Evaporator
Temescal Semiconductor
Model VES 2550 Products
- Sputtering System
Applied Materials Endura
- Dielectric PECVD System
Novellus Concept 1
- Leak Detector
Veeco Instruments Inc. Model MS-20 &
Model MS-170
- Wet Chemical Process Station
Semifab Inc., Model WPS 400
- Gas Cabinets
Veriflow Corp. Toxic Gas Delivery Systems
- Toxic Gas Monitor
MDA Scientific, Inc., Model 7100

Etching

- Polysilicon/Oxide Dry Etch
AME Model P5000
- Polysilicon/Nitride Dry Etch
Lam Research Model 480
- Metal Dry Etch
Lam Research Model 680
- Wet Chemical Process Stations
Semifab Inc., Model WPS-400

Metrology

- Spectroscopic Ellipsometer
KLA-Tencor-Prometrix UV-1280
- Surface Profilometer
KLA-Tencor-Prometrix P10
- CV Plotter
Materials Development Corporation
Model CSM-16 Advanced Semiconductor
- Ellipsometer
Gaertner Scientific Corporation
Model L116BLC-26A
- Automatic Wafer Inspection System
Aeronca Electronics Inc. WIS 150
- Automatic Four-point Probe
Prometrix Corporation Omnimap 111B
Resistivity Mapping System
- Inspection Microscope
E. Leitz Inc. Ergolux Microscope/
Camera System
- Low Voltage Scanning Electron Microscope
Hitachi Model S-806
- Critical Dimension Scanning Electron Microscope
Hitachi Model S-6000

continued

Equipment

continued

Integrated Circuits Laboratory (ICL)

Polishing/Etching

- Chemo-mechanical Polishing
Strasbaugh GEC
- Wafer Cleaner
SSEC Evergreen
- KOH Wet Etch Station
- Cu-plating Wet Station
- Film-thickness measurement system
KLA-Tencor-Prometrix SM-300

Inspection and Test

- Non-Contact Surface Profiler
WYKO Corporation, TOPO - 2D, TOPO - 3D
- Spreading Resistance Probe
Solid State Measurements, Inc.
Model ASR-100C/2
- Scanning Electron Microscope
Hitachi Model S-800
- Electrical Measurements
Hewlett-Packard Model HP 4062B
Keithley Model 450 S
- Probers
Electroglas Model 2001X
Rucker/Kolls Model 1032

Technology Research Laboratory (TRL)

Lithography

- Mask Aligner
Karl Suss Model MA4
- Mask Aligner
Electronic Visions EV620
- Manual Photoresist Coater
Solitec Inc. Model 5110
- Bake Ovens
Blue M Model DDC-146C
- Wet Processing Station
Semifab Inc. Model WPS 800
- Inspection Microscope
Nikon Nomarski Microscope
- Surface Profilometer
Sloan Technology Corporation Dektak II
- Plasma Resist Stripper
Branson IPC
- Wafer Aligner/Bonder
Electronic Visions
- Photomask Contact Printer
Oriel Corporation Model 850202
- Measuring Microscope
Nikon Model MM-1

continued

Equipment

continued

Technology Research Laboratory (TRL)

Diffusion and Oxidation

- Furnaces
MRL Industries Model 718 System
(7 atmospheric tubes, 1 LPCVD tube)
- Wet Chemical Process Station
Semifab Inc. Model WPS-400
- Rapid Thermal Annealer
AG Associates Heatpulse 210T-02

Chemical Vapor Deposition/Etching

- PECVD/RIE
Plasma Technology Plasmalab mP
- PECVD/RIE
PlasmaQuest

Etching

- ICP Deep Trench Etching System
STS - 6"
- ICP Deep Trench Etching System
STS - 4"
- Wet Chemical Process Station
Laminaire Corp.
- Wet Chemical Process Station
- Toxic Gas Monitor
MDA Scientific, Inc., PSM-8e
Multipoint Monitoring System
- Gas Cabinets
Scientific Gas Products

Metal Deposition

- Electron-Beam Evaporator
Temescal Semiconductor Products
- Sputtering System
Perkin Elmer Model 4450

Metrology

- Non-contact profiler WYKO Corp., RST
- Wafer curvature measurement system
KLA-Tencor FLX 2320
- Film thickness Measurement System
Nanometrics, Inc. Nanospec, AFT
Model L116BLC-26A
- Surface Profiler
Sloan Technology Corp. Dektak IIA
- IV Characterization
2-point probe station
Tektronix 486 curve tracer

Experimental Apparatus

- Reactor for Low Pressure Epitaxial Growth of Erbium Doped Silicon and Silicon Germanium Alloys (L. C. Kimerling)

continued

Equipment

continued

Technology Research Laboratory (TRL) Computation and Communications

Assembly

- Saw
 - Disco Abrasive System Model DAD-2H/6T
 - Die Bonder
 - Kulicke and Soffa Industries Inc., Model 648
 - Gold Ball Wire Bonder
 - Kulicke and Soffa Industries Inc., Model 4124
 - Wedge Bonder
 - Kulicke and Soffa Industries Inc., Model 4123
 - Junction Sectioner
 - Philtec Instrument Co. Model 2015D
- Applications servers - Sun Ultra10 (2)
 - Network mail server - Sun Ultra10
 - CAD server - Sun Ultra2
 - Simulation server - DEC Alpha
 - Laboratory information servers - Sparc 20 (3)
 - Laboratory information PCs - 23
 - Intel 400 MHz Pentium-III
 - Research group workstations (60)
 - Research group personal computers (40)
 - X terminals (20)
 - Network color laser, black and white printers
 - Database servers(oracle) - Sun Ultra 10 (2)
 - WWW Server - Sun Ultra 10
 - Cad Server - Sun Ultra 2
 - Application/backup Cad Server - Sun Ultra 2
 - Application/Home Directory Server - Sun Ultra 2
 - MTL Mail/NIS Server - Sparc 5
 - Simulation Server - Dec Alpha 3000
 - Laboratory Information Servers - Sparc 20 (2)
 - Network Backup/Print Servers - Sparc 20 (3)
 - Laboratory and Staff Desktop PCs -
 - Intel 300MHz Pentium II (21)
 - NT Network Servers - Intel/Dual Processor Pentium II (2)
 - Network Switches - SuperStackII Switch 3300 (21)
 - Cisco 2500 Router (ten dial-in lines)
 - Peripheral Storage -
 - total +207Gigabytes StorEdge Multipaks (6)
 - Research Group Personal Computers (70)
 - Research Group Workstations
 - (Sun, HP, Alphas, IBM - 60)
 - X-terminals NCD (20)
 - Equipment Controller PCs (2)
 - Laboratory Access PCs (2)
 - Network Printers
 - Apple Color, HP Laserwriters (9)
-

Related Research Facilities

The NanoStructures Laboratory (NSL)

4,5000 sq-ft of laboratory clean space comprised of:

- 1,000 sq-ft class 10 clean space
- 1,000 sq-ft class 10,000 space
- 2,500 sq-ft of ordinary lab space

The Nanostructures Laboratory (NSL) at MIT develops techniques for fabricating surface structures with feature sizes in the range from nanometers to micrometers, and uses these structures in a variety of research projects. The NSL is closely coupled to the Space Microstructures Laboratory (SML) with which it shares facilities and a variety of joint programs. The NSL and SML include facilities for lithography (photo, interferometric, electron-beam, and x-ray), etching (chemical, plasma and reactive-ion), liftoff, electroplating, sputter deposition, and e-beam evaporation. Much of the equipment, and nearly all of the methods, utilized in the NSL/SML are developed in house. Generally, commercial processing equipment, designed for the semiconductor industry, cannot achieve the resolution needed for nanofabrication, is inordinately expensive, and lacks the required flexibility for our research. The research projects within the NSL/SML fall into three major categories: (1) development of nanostructure fabrication technology; (2) short-channel semiconductor devices, nanomagnetism and microphotonics; (3) periodic structures for x-ray optics, spectroscopy, atomic interferometry and nanometer metrology.

NSL Research Staff and Personnel

H. I. Smith, Keithley Professor of Electrical Engineering, Director
J. M. Carter, Research Specialist,
Research Lab of Electronics,
D. J. D. Carter, Research Scientist,
Research Lab of Electronics,
J. M. Daley, Senior Technician,
Research Laboratory of Electronics,
J. G. Goodberlet, Research Scientist,
Research Laboratory of Electronics,
C. A. Lewis, Administrative Assistant,
Research Laboratory of Electronics,
M. K. Mondol, Research Specialist,
Research Laboratory of Electronics,
E. Murphy, Research Technician,
Research Laboratory of Electronics
Dr. Mark L. Schattenburg, Principle Research Scientist,
Center for Space Research

continued

Related Research Facilities

continued

NanoStructures Laboratory (NSL) (Equipment)

- Electron-beam Lithography
IBM Vector Scan VS-2A, 50 KV
- Electron-beam Lithography
(Raith turnkey system)
- Achromatic Lithography System
(Custom System)
- Interference lithography system
(Custom system)
- Holographic-phase-shifting interferometer
(custom system)
- X-ray Lithography Systems
(4 Custom Systems)
- IBBI X-ray mask aligner
(Custom System)
- UV Lithography
Tamarack ELHG 200-350
- Deep UV Aligner
OAI 400
- Zone-plate-array lithography
(custom system)
- Reactive Ion Etchers
Perkin Elmer Model 3140
Plasma Therm Model 790
- Plasma Etcher
Technics Plasma Etch II
- Surface Profiler
Tencor Alpha Step 200
- Optical Microscopes (3)
Leitz, Orthoplan, Metalloplan
- Electron Microscope
Zeiss (LEO) 982 Gemini
- Ellipsometer
Gaertner L116B
- Substrate Cleaning Station
Interlab
- Evaporators
Ebeam: Airco Temescal BJD 1800
Thermal: Cooke MV VII CFR
- Gold Electroplating Systems
(2 Custom Systems)
- Ion Miller
Ion Tech
- RF Sputter System
MRC 8620
- Linnik Interferometer
Leitz
- Imaging Interferometer
Wyko Model 400
- Optical Spectrometer
EG&G/PARC Model 1235
- Atomic Force - Scanning Tunneling Microscope
Digital Instruments Nanoscope
- UV Ozone Cleaner
Jelight Model 42
- Workstation Computers - various types (14)

continued

Related Research Facilities

continued

The Space Nanotechnology Laboratory (SNL)

1700 sq-ft of laboratory space comprised of:

- 1230 sq-ft Class 100 space
- 450 sq-ft support space

The Space Nanotechnology Laboratory (SNL) is housed in the Center for Space Research (CSR). Its mission is to develop and apply advanced lithographic and nanofabrication technology to the fabrication of high performance space instrumentation, primarily for x-ray astronomy. These applications include nanometer-period transmission gratings for high-resolution x-ray spectroscopy, fabrication and assembly of super-smooth foil-optic x-ray mirrors and reflection gratings, and UV/atom beam filtering and diffraction. The SNL has fabricated a large quantity of 200-400 nm-period gratings for the NASA *Chandra* x-ray telescope now in orbit. The SNL has also fabricated gratings for eight other flight missions, including the NASA Solar and Heliospheric Observatory (SOHO), the NASA Imager for Magnetopause-to-Aurora Global Exploration (IMAGE), the NOAA Geostationary Operational Environmental Satellites (GOES), and the NASA Two Wide-Angle Imaging Neutral-Atom Spectrometers (TWINS). The SNL is also participating in several pre-mission technology development efforts.

The SNL is tightly integrated with research in the NanoStructures Laboratory (NSL). With support from NASA, DARPA, NSF, and other sponsors, the SNL/NSL collaboration has sustained a leadership position in several areas of advanced lithography research over the last two decades, including electron beam, and x-ray, and interference lithographies. In particular, the SNL houses the research interference lithography facility that was originally developed in the NSL. Nanometer-period gratings and grids patterned with this system support research at MIT in quantum-effect electronics, integrated opto-electronics, field-emitter flat panel displays, high-density magnetic storage, and nanometer metrology.

SNL Research Staff and Personnel

M. L. Schattenburg, Principal Research Scientist, CSR, Laboratory Director
C. R. Canizares, Professor of Physics and CSR Director, Faculty Advisor
J. M. Carter, Research Specialist, RLE
R. C. Fleming, Semiconductor Process Engineer, CSR, Laboratory Manager
R. Heilmann, Postdoctoral Associate, CSR
E. Murphy, Senior Technician, CSR
H. I. Smith, Professor, EECS, CSR, Laboratory Associate Director

Support Staff

D. Breslau, Project Technician Mechanical, CSR
S. Donovan, Senior Secretary, CSR

continued

Related Research Facilities

continued

The Space Nanotechnology Laboratory (SNL) (Equipment)

- Interference Lithography System
(experimental system)
- Interference Lithography System, Scanning Beam
(experimental system)
- UV Lithography
OAI Model 30
- Wafer Developer
SVG Wafertrack Model 8132
- Spin Coater/Dryer
Specialty Coating Systems Model P6204-A
- Bake Oven
VWR Model 1601
- UV Ozone Cleaner
Jelight Model 42
- Reactive Ion Etcher
Plasma Therm Model 770
- Full Wafer Imaging Interferometer (RIE Endpoint)
LES Model 1000-IS
- Gold Fountain-Bath Pulse-Plating System
Marks and Associates (custom system)
- Gold/Nickel Fountain-Bath Pulse-Plating System
(custom system)
- Acid Spin-Etch System
Materials and Technologies RotoEtch II
- Three-Axis Adhesive Dispensing System
CAMELOT Model 1414
- Bonding Aligner
(custom system)
- Optical Emission Spectrometer
EG&G Model 1420
- Optical Microscopes (2)
Leitz Ergolux, Wild M3Z
- Surface Profilometer
Dektak III
- Thin Film Analyzer (X-ray Fluorescence)
Fisons Instruments/ Kevex Omicron
- Thin Film Stress Monitor
Ionic Systems Model 3000
- Analytical Microbalance
Denver Instruments Model A-200DS
- Workstation Computers (15 of various types)
- Leak Checker, Helium
Balzers Model HLT 150
- Residual Gas Analyzer (3)
Leybold Transpector C100F
- Furnace
NEY Vulcan 3-550
- Signal Analyzer
HP 35670A
- Optical Surface Analyzer, Shack-Hartman
(custom system)

Related Research Facilities

continued

Facility for Growth and Processing of Compound Semiconductors Professor Leslie A. Kolodziejski

In the compound semiconductor epitaxy facility, the growth of III-V materials is accomplished using gas source molecular beam epitaxy techniques. The modular epitaxy system consists of six chambers which are all interconnected and maintained at ultrahigh vacuum pressures ($\sim 10^{-10}$ Torr). Three main chambers are located around the periphery of the central transfer chamber: a III-V-dedicated reactor, a second growth reactor and an analytical chamber. In addition to the aforementioned main chambers, an introduction chamber is connected to the transfer chamber and serves as the interface between the laboratory and the ultrahigh vacuum environment. The III-V gas source molecular beam epitaxy (GSMBE) reactor is equipped with (1) solid elemental sources of Ga, In, Al, Si and Be, (2) gaseous hydride sources of arsenic and phosphorus, (3) an atomic hydrogen source and (4) an *in-situ* spectroscopic ellipsometer. The atomic hydrogen source is invaluable for experiments involving regrowth as native oxides are removed at low temperatures. Low temperature processing of oxide-contami-

nated surfaces is particularly important for regrowth onto patterned surfaces or onto fully metalized electronic circuitry for integration of optical components with VLSI circuitry. A second key *in-situ* tool employed with the III-V growth reactor is the spectroscopic ellipsometer. Alloy fractions and layer thicknesses can thus be determined in real time, greatly facilitating growth experiments. III-V compound semiconductor structures based on the alloy family of (In,Ga,Al)(As,P) are grown for fundamental studies of photonic bandgap crystals and for application in fiber optic communications. The second gas source molecular beam epitaxy reactor was used for the growth of II-VI compound semiconductors using metalorganic, hydride and solid sources. Finally, the availability of an interconnected analytical chamber provides an *in-situ* tool to aid in the understanding of the chemistry and structure of various surfaces and interfaces, which are fabricated in the epitaxial reactors.

continued

Related Research Facilities

continued

Millimeter-Wave, THz, and Subpicosecond Facilities Professor Qing Hu

Professor Hu's laboratory is equipped with various millimeter-wave and infrared sources which can generate coherent and incoherent radiation from 75 GHz up to 30 THz. These include: Gunn oscillators at W-band frequencies (75 - 110 GHz); a frequency doubler, tripler, and quadrupler using Schottky diodes at 200, 300, and 400 GHz; an optically pumped far-infrared laser which generates coherent radiation from 245 GHz to 8 THz; and a far-infrared and an infrared Fourier transform spectrometer which are capable of performing linear spectroscopy from 45 GHz to 300 THz and beyond. This laboratory is also equipped with various cryogenic millimeter-wave and infrared detectors. These include: a Ge:Ga photoconductive detector, Si composite bolometers, InSb hot-electron bolometers, SIS (Superconductor-Insulator-Superconductor) receivers, and high T_c Josephson detectors. Recently, with the support of AT&T, a mode-locked Ti:sapphire laser that can generate optical pulses as short as 70 femtoseconds was purchased and installed.

Facility for High-Frequency Characterization of Devices and Structures Professor Clifton G. Fonstad

In this facility members of the MIT community can characterize the response of devices, circuits, and structures to sinusoidal signals at frequencies up to 40 GHz. The centerpiece of this facility is a Hewlett-Packard 8510 Vector Network Analyzer System with a 40 GHz s-parameter test set. Complementing this system is a Cascade Microwave Probe Station for direct, on-wafer measurements; packaged devices can also be measured in this facility. Other equipment which is available includes a Hewlett-Packard 4145 Semiconductor Parameter Analyzer and a Tektronix 370 Digital Curve Tracer, either of which can be used to select and maintain bias points for the active devices under test.

This facility was established in part through gifts made by Hewlett-Packard and Tektronix, and in part through contributions from MTL faculty members and researchers. The facility is available to members of the MIT community. At the present time no charge are made for the use of the facility, but users are required to supply their own probe tips for the Cascade prober.

continued

