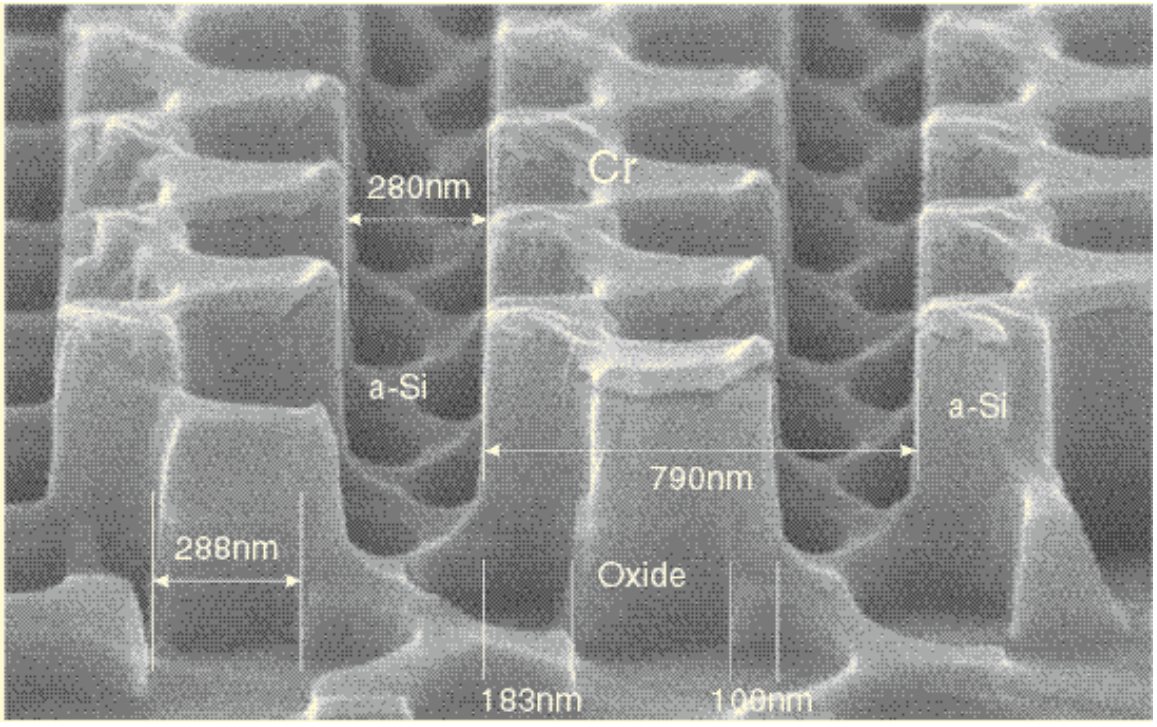
Optoelectronics



Scanning-electron micrograph of the patterned second layer of a 3-D photonic-bandgap structure, showing amorphous Si on top of the first-layer structure, with groves filled with SiO_2. The second layer structure is shifted by half of the periods in both x and y directions. An intentional overetch into the first layer is also observable.
Courtesy: M. Qi (J. Joannopoulos and H. I. Smith).

Optoelectronics

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Fabrication and Characterization of Bipolar Quantum Cascade Lasers

Personnel

G. S. Petrich and S. G. Patterson (L. A. Kolodziejski and R. J. Ram)

Sponsorship

ONR/MURI, MIT Lincoln Laboratories

The formation of series-coupled diode lasers allows the creation of high power optical sources and two-dimensional laser arrays. These series-coupled lasers can consist of discrete individual lasers interconnected together during the post-growth fabrication stage or individual lasers integrated together during the epitaxial growth process. However, interconnecting together discrete lasers suffers from the effects of parasitic resistances and capacitances. In bipolar quantum cascade lasers, a low resistance Esaki (tunnel) junction is created between the separate quantum well lasers during the epitaxial growth process to minimize these parasitic effects.

The bipolar quantum cascade laser was grown by gas source molecular beam epitaxy and consists of two identical epitaxially integrated lasers. Each laser is composed of 0.75 μm Si- and Be-doped InGaP cladding layers (nominally lattice-matched to a GaAs:Si substrate) with a single $In_{0.2}Ga_{0.8}As$ quantum well residing within the center of a 0.22 μm GaAs confinement layer. An Esaki junction, consisting of heavily Be- and Si-doped GaAs layers, each layer being 25 nm thick, couples the two lasers epitaxially. The fully processed lasers are 300 nm SiO_2 oxide-stripe, gain-guided, Fabry-Perot devices which were mounted to a heat sink with In solder.

A 5 μm wide, 450 μm long bipolar quantum cascade laser has been optically and electrically characterized at room temperature while operating in a continuous wave mode. From the voltage versus current measurements, the incremental resistance of the cascade laser is 6 ohms and the measured voltage drop across the device is double that of a single laser junction. The optical spectrum of a bipolar cascade laser that was biased just beyond the threshold of the second junction, exhibits two peaks at 991nm and 993nm, which correspond to the emission wavelengths of the two lasers. The laser's optical output power versus current clearly reveals two distinct thresholds at 1.95 kA/cm^2 and 2.18 kA/cm^2. An abrupt change in the output power was observed and is likely due to the p-n-p-n structure exhibiting a thyristor-type effect in which the location of the voltage drop within the device changed. The relatively large threshold currents are primarily due to current spreading, resulting in a wider injection region. Similar, but wider devices without heat sinking, have typically demonstrated threshold current densities of approximately 450 A/cm^2. The different threshold current densities of the two epitaxially-integrated laser junctions are believed to be indicative of the greater current spreading in the lower laser junction. Upon reaching the second laser's threshold, the slope efficiency abruptly switches from 0.313 W/A to 0.622 W/A per facet, corresponding to a differential quantum efficiency of 99.3%. These high efficiencies are characteristic of cascade devices. In addition, the clear doubling of the slope efficiency as the second laser diode junction exceeds threshold, provides strong evidence of the successful implementation of a bipolar cascade laser.

Further work will include optimizing of the device by thoroughly characterizing the existing devices and material properties, increasing the number of active regions in the stack, including oxidation layers to alleviate current spreading, and investigating the modulation properties of the device.

Development of Semiconductor Saturable Absorber Mirrors for Mode-locked Fiber Lasers

Personnel

L. A. Kolodziejski, E. P. Ippen, F. X. Kärtner, D. J. Jones,* M. Joschko, P. Langlois, E. M. Koontz, E. R. Thoen, and T. Schibli * University of Colorado and National Institute of Science and Technology, Boulder, CO

Sponsorship

MIT Lincoln Laboratory, MURI/AFOSR

Passive mode-locking is currently the most robust method of generating ultrashort (femtosecond) pulses in lasers. Due to the widespread use of semiconductor saturable absorber mirrors, it is important to characterize the devices so as to fully understand their principles of operation.

The saturable absorber mirrors fabricated thus far consist of gas source molecular beam epitaxially-deposited InP-based absorbers on GaAs-based Distributed Bragg Reflectors (DBRs). The DBR contains 22 pairs of quarter-wave AlAs/GaAs layers, producing a reflectivity greater than 99% centered at λ~1.55 μm. The InP-based absorber consists of four InGaAs quantum wells (λ~1.53 μm) centered within an InP half-wave layer. The absorption characteristics of the structure are tailored to specific laser cavities via the deposition of dielectric coatings.

Saturation fluence measurements (reflectivity change vs. incident energy density) of the aforementioned saturable absorber mirrors reveal the existence of Two-Photon Absorption (TPA). At low energy densities, the reflectivity change is due to absorption bleaching. As the energy density is increased, a large drop in reflectivity is observed, suggesting the presence of TPA. Incorporation of TPA in the commonly used fast absorber model generates an accurate fit to the experimental data, confirming the significance of TPA for these absorber mirror structures.

Since the magnitude of TPA is linearly dependent on the intensity incident on the absorber mirror, for a given structure, the TPA threshold will be determined by its absorption characteristics. Alteration of the absorption behavior by dielectric coatings is observable at both energy density extremes. Distributed Bragg reflectors without an absorber that were also measured over the same energy density range, exhibited no change in reflectivity and hence, verifying the presence of TPA within the half-wave InP absorber region.

As revealed by the saturation fluence measurements, TPA effectively limits the range of energy densities in which the absorber mirror will behave as a bleached absorber independent of other effects. Thus, for a given semiconductor saturable absorber mirror structure, there exists a limited energy density range over which it will provide a mode-locking mechanism for fiber lasers.

Development of High Speed DFB and DBR Semiconductor Lasers

Personnel

F. Rana, M. H. Lim and E. Marley (R. Ram, H. I. Smith and L. Kolodziejski)

Sponsorship

MIT Lincoln Laboratory

High-speed semiconductor DFB and DBR lasers are crucial for high-speed optical communication links. These lasers can be directly modulated at frequencies reaching 20 to 30 GHz. They have important applications in optical links based upon WDM (Wavelength Division Multiplexing) technology. Direct laser modulation schemes are much simpler to implement and integrate than modulation schemes based upon external modulators. However, modulation bandwidth of external modulators can easily go beyond 60 GHz. Thus, it is technologically important to have DFB/DBR lasers whose modulation bandwidths compete with those of external modulators. The goal of this project is to develop DFB and DBR lasers capable of being modulated at high speeds with low distortion and chirp.

High performance DFB and DBR lasers demand that careful attention be paid to the design of the gratings, which provides the optical feedback. Spatial-hole burning, side-mode suppression, radiation loss, laser linewidth, spontaneous emission in non-lasing modes, lasing wavelength selection and tunability, laser-relaxation oscillation frequency etc. are all features that are very sensitive to the grating design. Improved grating design can significantly enhance laser performance, especially at higher modulation frequencies. In the last few years various techniques have been developed in MIT NanoStructures Laboratory (NSL) that allow fabrication of gratings with spatially varying characteristics and with long-range spatial-phase coherence. Chirped optical gratings with spatially varying coupling parameter can be made using a combination of Interferometric lithography, spatially phase-locked electron-beam lithography and X-ray lithography. This provides us a unique opportunity for exploring a wide variety of grating designs for semiconductor DFB and DBR lasers. We plan to explore laser devices suited for high speed as well as for low noise operation.

We have developed techniques for fabricating high-speed, polyimide-planarized ridge waveguide laser structures that have low capacitance, and are therefore ideally suited for high frequency operation. Figure 1 shows the cross section of a polyimide-planarized InP DFB laser. The active region consists of strain compen-

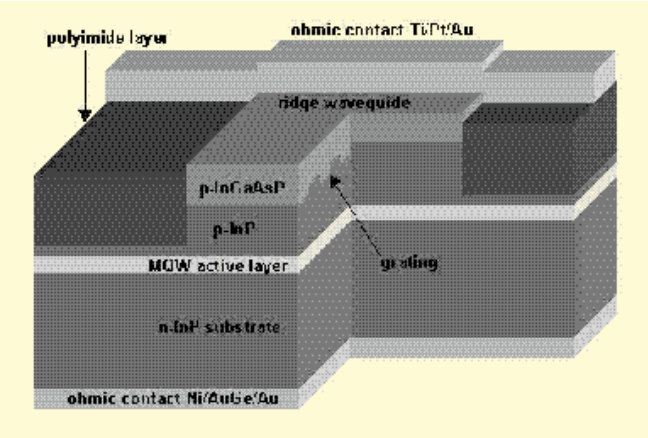

Fig. 1: Schematic of a polyimide-planarized In P DFB ridge-waveguide laser.

Fig. 2: Scanning electron micrograph of a polyimide-planarized InP ridge-waveguide laser.

continued

sated InGaAsP multiple quantum wells. The grating and the ridge are dry etched in RIE using a mixture of hydrogen and methane. Planarization is achieved by spinning multiple coatings of polyimide followed by a high temperature cure. Cured polyimide is dry etched in RIE using a mixture of oxygen and carbon tetra-fluoride until the top of the ridge gets exposed. Ohmic contact to the ridge is made by lift-off on top of the polyimide layer. The thick layer of polyimide significantly reduces the capacitance between the top metal contact and the substrate. A large value of this capacitance can short out the active region at high frequencies. Figure 2 shows a Scanning-Electron Micrograph (SEM) of a laser structure fabricated using this process.

We are also developing techniques to fabricate co-planar stripline structures for high-speed DFB/DBR lasers. Co-planar striplines offer improved microwave performance compared to microstrip structures. Figure 3 shows a polyimide based co-planar stripline laser structure. Fabrication of this structure requires etching polyimide such that the sidewalls do not become too steep so that metal interconnects can be continuous over them. We have successfully developed etching techniques for polyimide that allows us to control the sidewall angle. Figure 4 shows SEM of a metal interconnect running over the sidewall of a polyimide layer.

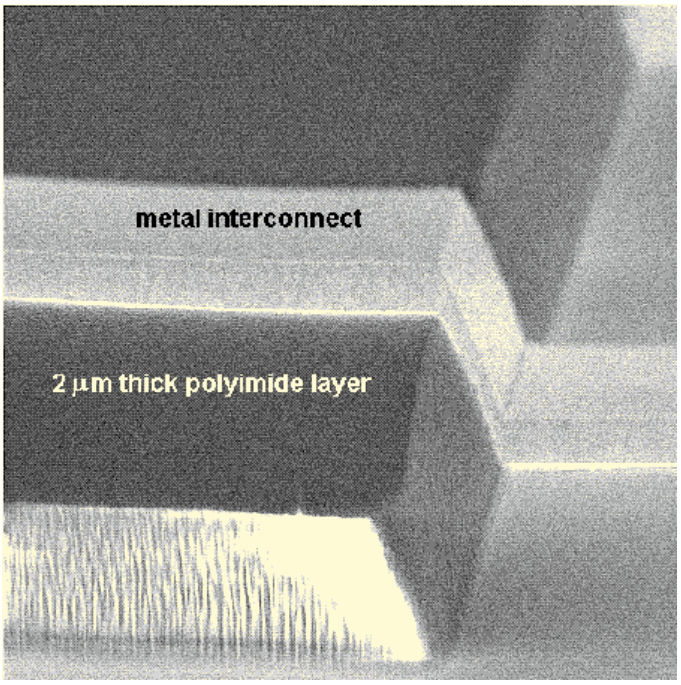

Fig. 4: Scanning electron micrograph of a low capacitance polyimide based metal interconnect.

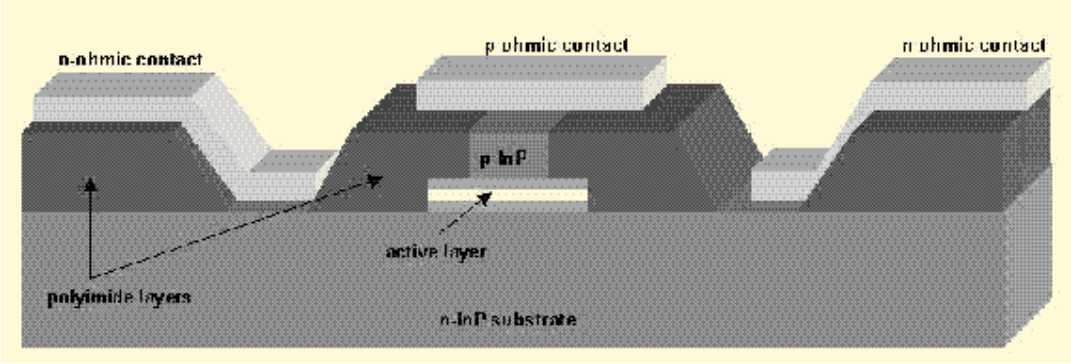

Fig. 3: Co-planar stripline laser structure.

Overgrowth of Rectangular-Patterned (In,Ga)(As,P) Surfaces

Personnel

G. S. Petrich, E. M. Koontz, G. D. U'Ren*, M. H. Lim, T. E. Murphy, and M. J. Khan (L. A. Kolodziejski, H. I. Smith, H. A. Haus and M. S. Goorsky, Department of Materials Science and Engineering, UCLA, Los Angeles, CA)

Sponsorship

MIT Lincoln Laboratory, MURI/AFOSR

The use of Wavelength Division Multiplexing (WDM) to expand the capacity of optical fiber communication systems is further enhanced by the minimization of the channel separation. This, in turn, leads to the need of narrow-band optical filters capable of selecting a single wavelength channel, while simultaneously leaving the remaining channels undisturbed. Waveguide-coupled Bragg-resonant filters provide a means of achieving narrow bandwidth filtering as required by high-density WDM.

In order to fabricate the Bragg-resonant filters, ~3.0 μm of InP must be epitaxially deposited on InGaAsP rectangular-patterned gratings without altering the grating profile. A low temperature atomic hydrogen-assisted oxide removal technique provides the means of minimizing the time at which the grating is exposed to the temperatures that are required for gas source molecular beam epitaxial growth, thereby minimizing mass transport effects. Using this technique, a grating similar to that required for the optical filter was fabricated, overgrown and analyzed to assess the grating fidelity.

The structure was microstructurally analyzed via reciprocal space maps that were generated by triple axis X-ray diffractometry. For an $In_{0.77}Ga_{0.23}As_{0.43}P_{0.57}$ rectangular-patterned grating that was fabricated via x-ray lithography and reactive ion etching, and overgrown with ~1 mm of InP, satellite reflections, which are due to the grating, are apparent in the reciprocal space maps near both the InGaAsP and InP peaks. The presence of $\pm 2^{nd}$ order satellite reflections indicates that the duty cycle was not 50%; the duty cycle was measured to be approximately 42% using scanning electron microscopy. As simulations of the actual grating showed, the intensity of the $\pm 2^{rd}$ order reflections should be similar to the intensity of the $\pm 3^{nd}$ order reflections. For the overgrown structure, the $\pm 2^{nd}$ order reflections are more intense than the $\pm 3^{rd}$ order reflections and the additional intensity is attributed to the presence of strain in both the InGaAsP grating teeth and the InP grating trenches.

In addition to the ±2 order satellite features, the asymmetric reciprocal space map exhibited additional intensity in the -1^{st} order satellite reflection about the InP Bragg peak, which corresponds to a shift in the diffraction envelope to negative Δq_x values. Similarly, the $+1^{st}$ order satellite reflection about the InGaAsP Bragg peak showed an intensity enhancement, corresponding to a shift of the envelope to positive Δq_x values. The presence of an asymmetric intensity distribution suggests that strain is present and is opposite in sense and of similar magnitude. A loss of in-plane symmetry occurs due to the one-dimensional surface grating, and hence, the unit cell of the material residing within the grating has assumed an orthorhombic Bravais lattice. The minimal orthorhombic strain is expected to influence the index of refraction, but by an amount that will not impact the optical performance of the Bragg-resonant filter. Thus, the successful preservation of rectangular-patterned surfaces following epitaxial growth suggests that devices incorporating abrupt refractive index variations will operate as designed.

Low Temperature Growth of Aluminum-Free InGaP/GaAs/InGaAs LED and Laser Diode Heterostructures by Solid Source MBE using a Special GaP Cell

Personnel

P. A. Postigo (C. G. Fonstad, Jr., in collaboration with D. Braddock, EScience, Inc.)

Sponsorship

DARPA, NSF

The use of InGaP instead of AlGaAs for the fabrication of light emitting heterostructures as Light Emitting Diodes (LEDs) and Laser Diodes (LDs) presents important advantages, such as the reduction of deep donor levels and lower InGaP/GaAs interface recombination velocity. In addition, InGaP is more suitable for the reduced-temperature Molecular Beam Epitaxy (MBE) required for the Epitaxy-on-Electronics (EoE) integration technology (475°C), since it is aluminum-free.

The use of phosphorous in MBE has traditionally been done through the introduction of phosphine (PH_3) as a gaseous source. However, the use of a solid source is also very attractive since it is easier to implement and to maintain in the MBE system, but it must be a solid source which gives a very high ratio of dimers to tetramers, i.e., P_2 to P_4 . The dimers have a higher sticking coefficient and are much better for MBE growth. Two methods have been used to produce P_2 from solid sources. One is based in a two-zone-cracker cell where the P_4 is cracked in P_2 by a very high temperature section (>1000°C), and where the source is solid red-phosphorous. The other method is based on the sublimation of phosphorous from phosphides as GaP, which produces the best P_2 to P_4 rate (around 170 compared to the 3.5 to 6 of the thermal cracker). The GaP decomposition cell has the same design as a common group-III effusion cell that operates at high temperatures (the typical temperature used for phosphide growth is around 1000°C) and it can be operated as a regular group-III cell. However, this type of cell can produce some residual amount of Ga, that can be reduced through an special design. This design implements a dome-shaped and disk-shaped Pyrolytic Boron Nitride (PBN) cap on top of the normal crucible, that acts as a trap for the Ga atoms. In collaboration with Dr. David Braddock, from EScience Inc., we have successfully demonstrated a high-capacity (100 gr.) GaP decomposition source that has produced high quality epitaxial InP and InGaP. The epilayers have been analyzed by Double-Crystal X-Ray diffraction (DCXR), Photoluminescence Spectroscopy (PL), and Secondary Ion Mass Spectroscopy (SIMS). The high purity of the P_2 beam obtained through this method and the good behavior of the cell have been used to produce InP/InGaAs photodetectors and InGaP/GaAs/InGaAs LEDs heterostructures at low growth temperature (475°C). Further work will focus on using this P_2 source for reduced-temperature growth of InGaP/GaAs/InGaAs laser diodes for integration on GaAs VLSI chips using the Epitaxy-on-Electronics process.

Monolithic Integration of Surface-Emitting Laser Diodes on GaAs VLSI Electronics

Personnel

A. Postigo, H. Choy and J. Ahadian (C. G. Fonstad, Jr., in collaboration with S. Choy and W. Goodhue of MIT Lincoln Laboratory and U. Mass-Lowell)

Sponsorship

NSF, Lincoln Laboratory

We are studying two surface-emitting laser diode designs for application in the Epitaxy-on-Electronics technology. The first is an In-Plane, Surface-Emitting Laser (IPSEL) design developed at MIT Lincoln Laboratory, and the second is the more common Vertical-Cavity, Surface Emitting Laser (VCSEL).

An important challenge we face with using aluminum-free heterostructures to fabricate IPSELs is the dry etching of the vertical end-mirror facets and of the angled deflector structures, because of the very different chemical make-up of the layers. In particular, the wider bandgap InGaAsP layers contain significant amounts of In and P, and relatively little or no As, whereas the narrow-gap GaAs and InGaAs layers contain roughly 50% As, no P, and relatively little or no In. Conventional chlorine-based and methane-based dry etch techniques do not work well with the aluminum-free heterostructures. We find, for example, that ion-beam assisted chlorine etching of InGaP is very slow at room temperature; at elevated temperatures where the InGaP etches satisfactorily, GaAs layers are etched without the need for the ion beam and severe lateral etching occurs, i.e., the etch is not directional and not anisotropic. While we can make use of this feature in the EoE process for removing polycrystalline deposits, it is not useful for facet etching.

The solution to this problem lies in changing the etchant from chlorine to bromine because the vapor pressures of the relevant bromides are much more similar than are those of the corresponding chlorides. Consequently, it is possible to find etch conditions for which the etch rates of InGaP and GaAs are sufficiently similar that vertical mirror facets can be successfully etched. We have used these results to produce the first etched-facet aluminum-free laser diodes. The threshold current densities of broad-area etched-facet laser diodes are a factor of two higher than adjacent cleaved-facet lasers. We are currently working on improving the quality of the etched facets and on fabricating IPSELs on the OEIC chip MIT-OEIC-6.

Vertical-cavity surface-emitting lasers (VCSELs) are particularly suitable as light sources for optoelectronics integration technologies, such as our Epitaxy-on-Electronics (EoE) process. The compact, vertical geometry and the completely epitaxial growth of VCSELs make mass fabrication and testing convenient and economical. The small size of the active region results in low threshold currents. Finally, the surface-emitting property results in an excellent beam profile of the emission, which simplifies coupling to optical fibers. VCSELs are emerging as ideal light emitters for high-density free-space interconnection, but they are very difficult to grow and present many challenges, especially for EoE integration.

We have done extensive modeling of a variety of p-type mirror designs (it is the p-, rather than the n-, mirror that is the more demanding), and are presently characterizing VCSEL mirrors and active regions grown at the reduced temperatures compatible with EoE integration. Our ultimate objective is to integrate VCSELs on OPTOCHIP, as a second generation improvement on the original LEDs.

Design and Analysis of VCSEL-Based Resonant Cavity Enhanced Photodetectors

Personnel

T. Knoedl and K. H. Choy (C. G. Fonstad, Jr.)

Sponsorship

University of Ulm, NSF

It is extremely desirable for monolithic optoelectronic integration to have emitters and detectors operating at the same wavelength, which can be fabricated from the same basic heterostructure. To this end we have modeled and studied (theoretically at this stage) the design of Resonant Cavity Enhanced Photodetectors (RCEPs) using heterostructure designed primarily for Vertical Cavity Surface Emitting Lasers (VCSELs).

A transmission matrix model was developed to compute the optical electric field and power in a complex, multi-layered heterostructure. The input to the program is the composition profile of the structure, and the program calculates the spectral response of the detector after first calculating the appropriate refractive indices, absorption coefficients, etc. The program can accommodate graded interfaces and doping profiles, as well as variations in temperature and in incident angle.

Simulation indicates that the most important parameter for the device designer is the top mirror reflectivity. As expected, there is a direct competition between the peak quantum efficiency of an RCEP and its spectral bandwidth. It is clear from the analysis that the narrow spectral bandwidth inherent in achieving a useful peak quantum efficiency from a single-resonant-cavity RCE fabricated from a modified VCSEL structure, and the significant shift of the resonance to longer wavelength seen with increasing temperature, that the usefulness of simple RCEP/VCSEL combinations is very limited. Consequently, we have also studied VCSEL-based RCEPs with broadened response spectra created by depositing additional, multiple-resonance mirror stacks on the top surface, after first modifying the original VCSEL top mirror stack. Initial indications from these studies, which are still in progress, indicate that this approach is very attractive.

A simple model allowing one to make a first order approximation to estimate the high speed behavior of RCEPs was also developed. The indication is that RCEPs can be twice as fast as PIN detectors with comparable quantum efficiencies.

This research was initiated by Thomas Knoedl during a six-month stay in our laboratories at MIT and was presented, in part, as his minor thesis (Studienarbeit) to the University of Ulm in January 1998. Mr. Knoedl returned to MIT in the Summer of 1998 and continued his work with an experimental investigation of resonant cavity enhanced photodetectors fabricated from VCSEL heterostructures.

MSM Photodetectors compatible with the Vitesse HGaAs-4 VLSI Process

Personnel
J. Ahadian (C. G. Fonstad. Jr.. in collaboration with J. M. Mikkelson of Vitesse Semiconductor)

Sponsorship
Vitesse Semiconductor

A clear choice for a photodetector to be used in a GaAs MESFET integrated circuit technology would be the Metal-Semiconductor-Metal (MSM) photodetector since it uses an interdigitated array of Schottky barriers on the surface of GaAs which structurally is very similar to the MESFET gate metal pattern, and it would appear that MSM detectors could be readily fabricated as part of a standard MESFET process. However, because a the gates in a modern GaAs IC process are self-aligned to the source and the drain by ion implantation, this basic process must be modified so that this same implant does not occur over the MSM detectors, thereby degrading their performance significantly. Furthermore, because the ideal operating conditions for an MSM detector involve fully depleting the regions under the finger pattern, and because MSM performance can suffer if the photo-injected carriers are not rapidly swept out of the active device area, additional precautions must be taken.

We have worked with Jim Mikkelson, the Chief Technical Officer of Vitesse Semiconductor, to make minimally intrusive modifications to Vitesse's new HGaAs-4 IC process which will allow Vitesse to produce GaAs ICs with integrated high performance MSM photodetectors. Cells containing these detectors have been included on the MIT-OEIC-7 chip scheduled to be received from the MOSIS service in February 1999; testing and characterization of the new MSM detectors will be undertaken in early 1999. The HGaAs-4 process includes deep n-type isolation implants to define separated p-type wells and heavy p-type implants and ohmic contacts to individual wells. These features, in conjunction with the process modifications, are expected to yield high sensitivity, high speed MSM detectors.

Monolithic Integration of 1550 nm Photodetectors on GaAs Transimpedance Amplifier Chips

Personnel
H. Wang (C. G. Fonstad, Jr., in collaboration M. Kuznetzov of MIT Lincoln Laboratory and R. Deming and J. M. Mikkelson of Vitesse Semiconductor)

Sponsorship
MIT Lincoln Laboratory

High data rate optical communication systems require increasingly complex integration of high performance electronic circuits with sophisticated optoelectronic devices. In the short run these needs can be met by hybrid assemblies. However the cost, performance compromises, and reliability concerns associated with hybrid integration, and the increasing need for specialized subcircuits which are not commercially available, make development of the monolithic integrated circuit technology extremely desirable.

We are using several techniques to monolithically integrate 1550 nm photodetectors with Gallium Arsenide (GaAs) TransImpedance Amplifiers (TIAs) to form monolithic OptoElectronic Integrated Circuits (OEICs) for fiber-based systems. Both Epitaxy-on-Electronics (EoE), described elsewhere in this report, and Aligned Pillar Bonding (APB), also described elsewhere in this report, are being considered. In the EoE process, optical devices are epitaxially grown on fully processed GaAs integrated circuits. For this application, high-speed photodetectors based on the lattice-mismatched InGaAs/GaAs material system are being developed and evaluated. For the wafer bonding process, fully lattice-matched photodetector heterostructures, grown under optimal conditions on InP, will be bonded onto the same GaAs circuits. After EoE epitaxy or wafer bonding, the device heterostructures will be processed and monolithically integrated with the pre-existing electronics, yielding high speed, compact, reliable monolithic OEICs.

continued

continued

The GaAs transimpedance amplifier test chip (MIT-OEIC-5/LL-MORX1), which incorporates modified versions of a commercial Vitesse transimpedance amplifier, has been obtained through the MOSIS service. Included on this chip are polarization diversity heterodyne photoreceivers, dual-balanced photoreceivers, and other functional cells; the chip is suitable for both EoE epitaxy and wafer bonding. Measurements of the high frequency performance of the amplifiers on these chips indicate that they will operate well to in excess of 600 MHz.

The performance of 1550 nm $In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As$ pin photodiodes grown on GaAs substrates using linearly graded buffers has been compared with that of detectors incorporating Graded Short-Period Superlattice (GSSL) buffers. Detectors on linearly-graded buffer were found to be superior to those on GSSL buffer. However, the best dark current levels seen (5µA for 50µm square detectors at 2V bias) must be reduced further to be acceptable for integration. Several ways of doing this have been investigated, but their success has been limited in the sense that device-to-device variations across a chip, as well as from chip to chip, remain large. Since the goal is to take advantage of the close matching promised by monolithic integration, this large variation is a serious concern. Initial indications are that this variation arises from the need to do lattice-mismatched growth of long-wavelength detectors best grown on InP, on GaAs substrates instead, and may be an intrinsic limitation. If this is true, the obvious solution is aligned pillar bonding (APB).

GaN/AlGaN UV Photodetectors

Personnel

J. Jacobs and R. Dutt (A. I. Akinwande)

Sponsorship

DARPA, Lockheed-Martin, Honeywell

Recent developments in III-nitride technology have led to the fabrication of GaN and AlGaN UV photodetectors with practical applications including missile detection systems and flame sensors. The AlGaN alloys are the most promising materials because of their direct bandgap which is tunable between 3.4 eV (364 nm) for Gan and 6.2 eV (200 nm) for AlN.

Several problems still exist which inhibit the development of these devices. Epitaxial layers of the materials grown by MOCVD still have high defect densities leading to high leakage currents. Other issues include poor ohmic contacts and low carrier concentrations of p-layers.

The objective of this project is to design and fabricate GaN solar blind UV detectors based on GaN/AlGaN nin/npn structures. The devices under consideration are back-illuminated (a) GaN/AlGaN heterojunction photodiodes with high quantum efficiencies were demonstrated and (b) GaN/AlGaN heterojunction phototransistors. The structure of the diode is as shown in Figure 5 below. The use of GaN/AlGaN heterojunction allows photons to be absorbed within the p-n junction. This improves efficiency primarily due to the elimination of carrier losses by surface recombination and diffusion processes.

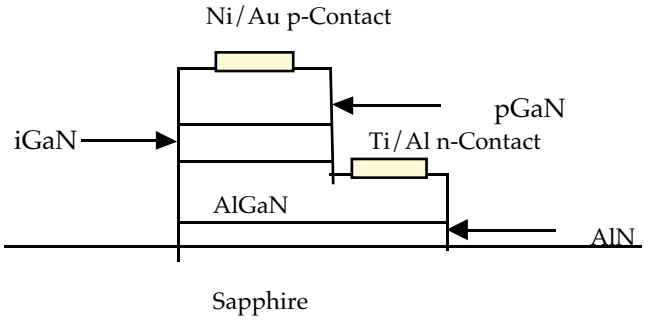

Fig. 5: Sxtructure of the diode.

High Performance (1Gbps/channel) Laser Drivers, Photoreceivers, and Photoreceiver Arrays

Personnel

J. Ahadian (C. G. Fonstad, Jr.)

Sponsorship

Optoelectronics Industry Development Association (OIDA)

As important to producing monolithic OEICs operating at 1 Gbps/channel, or more, as developing integration technologies and high performance optoelectronic devices, is designing suitable interface circuitry, i.e., laser and LED drivers and optical receiver circuits. We have done extensive work in this area and most recently have designed several laser driver and optical receivers in the new Vitesse Semiconductor HGaAs-4 process. These designs are included in three chips submitted to the MOSIS HGaAs-4 run in Fall 1998; the chips from this run are scheduled to be received in early February 1999. The three chips are a multi-design chip, MIT-OEIC-7, which contains several driver and receiver designs, and two 4 x 4 receiver array chips, MIT-OEIC-8 and MIT-OEIC-9, that were designed for the Optoelectronics Industry Development Association (OIDA). These array chips are designed to operate at 1 Gbps/channel and each 2.3 mm square chip will be housed in a 34-pin quad-flat-pack. They will be made available to optical interconnect systems researchers by OIDA through the Joint Optoelectronics Program (JOP).

The goal of any digital optical receiver is to generate a logic output on the basis of an optical input. To this end, the photocurrent generated by an illuminated MSM photodetector must be compared to a reference level to determine if the optical signal is high or low. In this work two basic types of receivers are being considered. One is an amplifier/comparator which continually produces a valid logic output reflecting its input; the other is a clocked receiver which latches its input value at a specified instant.

The array chips both use continuous-time receivers. On MIT-OEIC-8 the design consists of three linear amplifier stages followed by a Direct-Coupled FET Logic (DCFL) inverter. The third stage is a differential amplifier while the first two stages are single-ended. To reject supply noise, however, matched pairs of amplifiers are used in the first two stages. This scheme is used instead of three differential stages in order to eliminate level-shifting between stages which would greatly increase power consumption and reduce bandwidth. This design is simulated to operate above 1 Gbps, consume 4.5 mW, and respond to input signals as low as 50 μW. It occupies a space 80 μm by 230 μm. The second array chip, MIT-OEIC-9 uses a fully differential receiver design and a novel line-driver design optimally suited for array applications to maintain a high bandwidth. This design also operates above 1 Gbps, is more sensitive (responding to 25 μW input) than the other design and should be more robust and less sensitive to noise, but it consumes considerably more power (23 mW).

The test chip, MIT-OEIC-7, contains several variations on the circuits described above, as well as a clocked receiver which is much more compact (40 μm by 120 μm), and is expected to consume much less power (1.8 mW), than either of the continuous-time designs. We are interested in getting experience with receivers of this type and comparing their performance with that of continuous-time receivers.

Development of Semiconductor Optical Amplifiers for All-Optical Signal Processing

Personnel

L. A. Kolodziejski, K. L. Hall*, M. Kuznetsov*, J. Donnelly*, G. S. Petrich, E. M. Koontz and S. Saini* MIT Lincoln Laboratory

Sponsorship

MIT Lincoln Laboratory

Ultrafast all-optical time-division-multiplexed communication networks with data rates of 100 Gbits/s are currently being developed. At these speeds, significant data processing can not be accomplished. Thus, network elements incorporating all-optical switches that are capable of operating at 100 Gbit/s and higher, are needed. The use of a Semiconductor Optical Amplifier (SOA) as the nonlinear medium in all-optical switches, as opposed to a fiber amplifier, is attractive; semiconductors have a greater intensity-dependent refractive index modulation and more amplification within a given length. The current work, in collaboration with MIT Lincoln Laboratories, involves the development of a SOA optimized for an ultrafast nonlinear interferometric all-optical switch operating at 100 Gbit/s.

In preparation for processing the SOA, InP-based passive waveguides were fabricated. The waveguide structure consisted of an organo-metallic vapor phase epitaxy-grown InGaAsP/InP heterostructure (comprised of InGaAsP guiding and cladding layers, surrounded by InP). The strip-loaded geometry was defined by standard photolithographic techniques. The ridges were defined via Reactive Ion Etching (RIE) and wet chemical etching. Although RIE defines the ridges with straight sidewalls, the resulting trench basal plane can have a roughness of ~0.1 ßµm. The role of the wet etch is to remove the remaining material within the trenches, and to smoothly terminate on the InGaAsP etch stop layer. This leads to a more uniform refractive index contrast resulting in better lateral waveguide confinement. Following the definition of the ridges, the waveguides were covered with a protective oxide layer, and the InP substrate was thinned. Finally, the devices were cleaved to various lengths.

The passive waveguides were characterized by loss measurements. For these measurements, the output from a distributed feedback laser was coupled into the waveguide layer, and a Vidicon camera recorded the transmitted intensity. Constructive or destructive reflections within the waveguide Fabry-Perot cavity, as a function of wavelength, produces an oscillatory output intensity. The facet reflectivity and the active layer absorption loss were both determined from the output intensity peak-to-valley ratio. A loss of $a \approx 0.6\ cm^{-1}$ and a reflectivity of $R \approx 0.3$ were measured for the processed devices. These measurements are comparable to those waveguides that were previously processed from this same heterostructure. The InGaAsP loss calculation provides a lower limit for the loss, which is determined by the intrinsic material quality.

Epitaxy on Electronics Integration Technology

Personnel

J. Ahadian and P. A. Postigo (C. G. Fonstad, Jr., in collaboration with J. M. Mikkelson of Vitesse Semiconductor and S. Choy and W. Goodhue of MIT Lincoln Laboratory and U. Mass-Lowell)

Sponsorship

DARPA, Lincoln Laboratory, ONR

The development of optical interconnects has been hampered by the lack of a viable source of complex OptoelEctronic Integrated Circuits (OEICs), circuits which will ultimately need to contain thousands of optoelectronic devices tightly integrated with VLSI-complexity electronics. Hybriding, wafer-bonding, and epitaxial lift-off have made progress in addressing this need, however issues of density performance, reliability, and yield suggest that monolithic integration is the best answer, as it has been in conventional microelectronics manufacturing. To answer this need we have developed a process, termed Epitaxy-on-Electronics (EoE), for monolithically integrating optoelectronic devices on commercially processed gallium arsenide ICs.

The EoE process begins with custom-designed GaAs VLSI circuits. The electronics technology (the Vitesse Semiconductor HGaAs-3 and HGaAs-4 processes) provides enhancement- and depletion-mode MESFETs and four layers of aluminum-based electrical interconnect, as well as OPtical Field-Effect Transistor (OPFET) and Metal-Semiconductor-Metal (MSM) photodetectors. Molecular Beam Epitaxy (MBE) is used to grow device heterostructures on regions of the GaAs substrate which are exposed by cutting through the interconnect dielectric stack. Established fabrication techniques complete the integration procedure. The unrestricted placement of the optoelectronic devices occurs as part of the routine layout of the integrated circuit; the interconnect dielectric stack in the regions designated for these devices is partially etched at the GaAs foundry forming Dielectric Growth Windows (DGWs). The etch is completed, exposing the underlying GaAs substrate, upon receipt of the ICs from the manufacturer. The source/drain implant is used as the bottom n-contact of the optoelectronic device. Epitaxial material is then grown in the DGWs, while polycrystalline material is deposited on the overglass. Standard processing techniques are then used to remove the polycrystalline material, to fabricate the optoelectronic devices, and to interconnect the top-side electrical contacts of the devices to the electronics.

As in standard silicon technologies, the gallium arsenide VLSI process uses aluminum-based electrical interconnects. We have shown that these interconnects degrade when exposed to temperatures in excess of 475˚C. Conventional MBE practice uses a 580˚C temperature excursion to desorb the native oxide on the GaAs surface prior to growth, and even this brief high temperature exposure (which was used in previous EoE work) results in appreciable damage to the interconnect lines. Interconnect degradation is now effectively eliminated by using cracked hydrogen to remove the native oxide at as low as 350˚C.

The epitaxy must also be carried out below 475˚C. This is not compatible with the growth of high quality AlGaAs suitable for emitters (although it can be used in passive applications) due to aluminum's high affinity for oxygen. To circumvent this difficulty, current EoE efforts use the aluminum-free InGaAsP materials system, which is routinely grown a reduced temperatures.

Process innovations in the areas of DGW preparation, low temperature GaAs native oxide removal, and gas-source MBE growth of EoE compatible optoelectronic devices have removed limitations present in previous EoE demonstrations. Ring oscillator measurements made before and after EoE processing have verified sub-100 picosecond gate delays, consistent with sub-nanosecond, multi-gigahertz electronics operation. The present EoE technology is now being applied to a variety of applications benefiting from the integration of high performance heterostructure devices with VLSI-complexity electronics.

Aligned Pillar Bonding: Full-wafer Selective-area Bonding of Optoelectronic Devices on GaAs Integrated Circuits

Personnel

G. Lullo, H. Wang and D. Crankshaw (C. G. Fonstad, Jr.)

Sponsorship

NSF

A new integration technique is under development which uses aligned, selective-area bonding to integrate III-V heterostructure devices, such as laser diodes and p-i-n detectors, with commercially-processed electronic integrated circuits to create OptoElectronic Integrated Circuits (OEICs) with VLSI levels of density and complexity. This technique has been named Aligned Pillar Bonding (APB). The APB technique is similar in function to the Epitaxy-on-Electronics (EoE) technique in which III-V device heterostructures are first grown epitaxially in dielectric growth windows exposing the substrate surface in selected areas on fully-processed GaAs integrated circuit wafers. The heterostructures are then processed into optoelectronic devices interconnected with the pre-existing electronics to create monolithic OEICs. Like EoE, APB combines established commercial electronics processes with standard optoelectronic device fabrication sequences, to minimize the development effort necessary to achieve complex optoelectronic integration.

One of the limitations of the EoE process is that the epitaxy must be done at under 475˚C; another limitation is that the epitaxy must be done on a GaAs substrate. While the EoE process successfully addresses these limitations, it would be very desirable in certain applications to have a technique available which does not have these two restrictions: APB fills this need.

A key element in the APB process is the use of bonding rather than direct selective area epitaxy. In the APB technique, the heterostructure for an optoelectronic device, such as a laser diode, is first grown under optimal conditions on the optimal substrate. The heterostructure is then patterned into pillars, which are in turn wafer fusion bonded into dielectric windows on a suitably prepared integrated circuit wafer (i.e., into the same windows that would be used for epitaxy in the EoE process). Doing this requires something more complex than encountered in previous III-V bonding experiments, namely alignment. The wafer on which the device heterostructure is grown and the pillars are formed, called the “source” wafer, must be aligned with the dielectric windows on the integrated circuit wafer onto which the devices are to be bonded. This wafer is called the “target” wafer.

In the past year we have developed a technique for achieving this alignment, and have demonstrated for the first time the successful aligned fusion of III-V pillars in dielectric windows on a GaAs IC chip. We have also demonstrated the subsequent removal of the substrate of the source wafer to complete the transfer of the pillars to the target wafer. This initial work involved direct semiconductor-to-semiconductor bonding and required substantial pressure to achieve contact and bonding. Subsequent work has investigated palladium-to-GaAs bonding and, more recently, layered gold alloy-to-GaAs bonding. Both have been successfully demonstrated, and work is continuing to refine the process. At the same time, contacts with groups growing Vertical-Cavity Surface-Emitting Laser (VCSEL) layers are being pursued with the goal of establishing a collaboration with such a group to use the APB technique to integrate VCSELs on, for example, OPTOCHIP die.

Si-on-GaAs:
Monolithic Heterogeneous Integration of Si CMOS with GaAs Optoelectronic Devices using EoE, SOI, and MEMS Techniques

Personnel

J. London and J. Ahadian (C. G. Fonstad, Jr.)

Sponsorship

DARPA, General Motors Fellowship

Researchers have long recognized the desirability of monolithically integrating III-V semiconductor optoelectronic devices, such as laser diodes and p-i-n detectors, with complex high density, high performance silicon electronic integrated circuits, ideally CMOS, to economically produce robust optoelectronic integrated circuits for a wide variety of applications. To this end, work was begun many years ago growing GaAs epitaxially on silicon, and this GaAs-on-Si research continues to this day, but with limited success. While most people focus on the lattice constant mismatch between Si and GaAs (and other III-V's) as the main difficulty with this approach, the more important issue is the large difference in Thermal Expansion Coefficient (TEC) between these materials. Very large stresses are induced in epitaxial III-V layers on silicon by even relatively small temperature changes because of the TEC difference; and such stresses are fatal to many optoelectronic devices.

We feel that the key to III-V/silicon monolithic optoelectronic integration lies in recognizing that optoelectronic devices are intrinsically very thick devices (typically at least a micron thick) which are very sensitive to stress, and silicon MOS transistors need only be a few tens of nanometers thick and are much less stress sensitive. Silicon-On-Insulator, SOI, transistors, for example, are routinely formed in Si films less than 10 nm thick. It is also well known from Silicon-On-Sapphire, SOS, processing that such thin silicon can withstand very high stresses induced by a large difference in TEC, in this case between Si and sapphire (which has a TEC similar to that of GaAs.)

Clearly the solution to monolithically integrating Si CMOS and GaAs-based optoelectronics is (1) to take advantage of the fact that one is not restricted to using silicon as the substrate for Si CMOS, and (2) to retain a GaAs substrate so that the intrinsically thick, inherently strain- and defect-sensitive optoelectronic devices see their optimum substrate, i.e., GaAs. In particular one can imagine using wafer bonding and SOI techniques to produce Si CMOS electronics on gallium arsenide substrates without sacrificing any of the performance of the CMOS while at the same time gaining access to state-of-the-art performance optoelectronic devices, e.g. laser diodes and photodetectors. This is the approach we are pursuing in developing a technology we term Silicon-on-Gallium Arsenide (SonG). The SonG process combines silicon and gallium arsenide substrates by wafer bonding. It builds expertise at MIT in the areas of wafer bonding, Silicon On Insulator (SOI) MOS IC technology, and Epitaxy on Electronics (EoE) optoelectronic integration technology.

In the past year we have demonstrated, for the first time, 100 nm thick silicon single crystal layers bonded by intervening oxide layers on 4" diameter GaAs wafers. These Si-on-GaAs (SonG) wafers have been shown to be able to withstand temperature cycles to in excess of 700˚C, and thus to be suitable for CMOS fabrication using a reduced-temperature SOI process and for Epitaxy-on-Electronics (EoE) integration of optoelectronic devices using molecular beam epitaxy. The same process used to create Si-on-GaAs wafers can also be used to transfer fully-processed SOI circuits to GaAs wafers (to be followed by EoE optoelectronic integration).

Work is now in progress to (1) demonstrate the growth of III-V device heterostructures on SonG substrates, and (2) planarize and bond processed SOI CMOS wafers to GaAs wafers using the SonG process. Success in these areas will open the way subsequently for the full integration of III-V light emitters (LEDs and laser diodes) with silicon CMOS electronics.

The OPTOCHIP Project

Personnel

J. Ahadian (C. G. Fonstad, Jr., in collaboration with J. M. Mikkelson, Vitesse Semiconductor)

Sponsorship

DARPA/ONR

The OPTOCHIP Project is a research foundry offering intended to provide prototype OEICs to selected university groups doing research on optical interconnect systems. The first generation OPTOCHIPs use InGaP/GaAs Light Emitting Diodes (LEDs) monolithically integrated using the Epitaxy-on-Electronics (EoE) technology on commercially fabricated GaAs integrated circuit chips containing Optical Field Effect Transistor (OPFET) and metal-semiconductor-metal (m-s-m) photodetectors, and enhancement- and depletion-mode Metal-Semiconductor Field Effect Transistors (MESFETs). A solicitation for participation was made in late 1995 and in early 1996 nine groups from eight universities were selected to participate; the universities represented are California Institute of Technology, Colorado State University, George Mason University, McGill University, Texas Christian University, University of Southern California, and University of Washington. These groups began work in February 1996 on the designs for 2 mm by 2 mm OEIC chips which were combined into a larger die and submitted to the MOSIS service in May 1996. The chips were fabricated by Vitesse Semiconductor Corporation, Camarillo, CA, in the summer and fall of 1996, and the EoE integration process was initiated early in 1997. Fabrication of the integrated LEDs was completed in May 1997, and the completed OPTOCHIP die were sawn into individual 2 mm by 2 mm chips and returned to the designers for deployment in their optical interconnect architectures. We have continued working throughout 1998 with the various groups which did OPTOCHIP designs as they have done measurements on their chips and employed them in systems demonstrations.

Electrical tests on the completed OPTOCHIP die show that there was no degradation in the electrical performance of the circuitry due to the EoE process. The performance and yield of the LEDs were poorer than had been achieved on previous test runs, due it appears to problems in the growth system, but several functional die were provided to each participating group. The amount of work done with the completed chips varies between the various groups, but several groups have performed extensive testing of their OEIC chips and have successfully employed them in systems-level situations. In one case, communication between a pair of OPTOCHIPs has been demonstrated. Work is continuing on the testing of the chips, and our group at MIT is working to be able to supply the participants with another set of die processed using the new GaP phosphorous source recently installed on our MBE.

The completed, overall 7mm by 7mm square OPTOCHIP die each contain over 200 LEDs integrated with numerous different circuits and subsystems containing thousands of transistors. As such they represent some of the most complex LED-based monolithic OEICs ever fabricated. The OPTOCHIP project was also unique in that the OPTOCHIP die incorporate designs from a diverse selection of groups and in that minimal constraints were placed on the circuit designs. Our intention is that there will be future OPTOCHIP offerings, and that the processing of subsequent OPTOCHIPs will be done on a semi-professional basis using the facilities of the Technology Research Laboratory (TRL) of the Microsystems Technology Laboratory (MTL) at MIT. We are also anxious to make surface-emitting lasers (SELs) available to OPTOCHIP users in the near future.

Normal-Incidence Quantum Well Infrared Photodetectors (QWIPs) for Monolithic Integration

Personnel

J. Pan and C. G. Fonstad, Jr.

Sponsorship

NSF, ONR, Lockheed-Martin

Band gap engineering allows us to design the peak responsivity of a Quantum Well Intersubband Photodetector (QWIP) to be at anywhere in the infrared region beyond about 2 μm. This wavelength region is useful for spectroscopy and identification of unknown gases, as well as for imaging in the Earth's atmosphere in the transparent spectral regions of 3 to 5 μm and 8 to 12 μm. Modern epitaxy techniques can achieve high uniformity of semiconductor parameters across entire III-V (GaAs and InP) wafers, which allows for the realization of large Focal Plane Arrays (FPAs) of QWIPs with low spatial (fixed) pattern noise. Furthermore, the growth of QWIPs on GaAs substrates is compatible with the integration of QWIPs with standard GaAs detector circuits using one of our monolithic optoelectronic integration technologies.

QWIPs which respond to normal incident radiation without the need for an optical grating, or other surface patterning, are of special interest because they can be fabricated with fewer process steps and increased expected yield. An important contribution of our work has been the demonstration of the first n-type QWIP (n-QWIP) which showed a significant detectivity without the use of an optical grating. The detectivity of these devices was large enough that focal plane array performance would be limited by the uniformity of the processing rather than by the single pixel detectivity.

Another important result of our work in the past year has been the development of numerically accurate physical models yielding simple analytical expressions for the QWIP leakage current and photocurrent, as well as for the number of wells, and the distance, over which carriers are depleted from quantum wells whenever the photocurrent is larger than the leakage current. This depletion capacitance is expected to be important at high frequencies, in situations where the photocurrent is larger than the leakage current, and in QWIPs designed with a small number of quantum wells (as when the quantum efficiency is large or an optical cavity is used).

Studies of the microscopic physics of quantum wells were undertaken to elucidate the physical origin of the intersubband absorption of normally incident radiation. A key result of this work was the derivation of selection rules for intersubband absorption of normally incident radiation by hole subbands in a p-doped QWIP (p-QWIP). It was found that the absorption of normally incident radiation by holes in a p-QWIP is largest for heavy hole to light hole transitions. The intersubband absorption of normally incident radiation by electrons in an n-QWIP is found to be much smaller than that in a p-QWIP. It is also found that uniaxial strain does not have a large effect on the strength or the selection rules of intersubband absorption because the Hamiltonian describing uniaxial strain has the same tetragonal symmetry as that carriers confined to quantum wells along the growth direction.

Finally, common QWIP designs used in industry have been evaluated. The commonly used n-QWIP design with superlattice confinement barriers intended to reduce thermionic leakage by pushing the three-dimensional continuum energy further up in energy while having the photocurrent flow in the superlattice miniband, was studied in detail. It was found that this QWIP design will in fact have a tunneling leakage current which is, at best, commensurate with (rather than much better than) a conventional QWIP made with a barrier material having a band edge matching that of the average band edge of the superlattice.

The research on QWIPs described here will be continued by Prof. Janet Pan at Yale University.

The Theory of Microscale Thermophotovoltaic Energy Conversion

Personnel

J. Pan and K. H. Choy (C. G. Fonstad, Jr.)

Sponsorship

Unfunded

The theoretical treatments of radiative heat transfer between bodies in close proximity in the literature tend to be highly numerical and, consequently, relatively non-physical and non-intuitive; they also tend to be wrong, or at least to contain errors which are obscured by the numerical calculations. The same problem has extended to the much more limited literature on microscale thermophotovoltaic conversion. The proximity effect is, however, relatively easy to understand if one thinks in terms of evanescent field coupling between two surfaces, and recalls a simple experiment involving two prisms and a laser which is often performed as a demonstration in undergraduate electromagnetics courses.

When the two prisms are positioned with their long faces parallel, but separated, a laser beam incident on the input face of the one prism will experience total internal reflection at the long face and exit the output face of the same prism; this is normal prism action. However, if the separation of the two prisms is decreased to a fraction of a laser light wavelength, some of the laser beam will transfer evanescently through the long face and into the second prism. As the separation decreases, the amount of transfer increases toward 100%.

To relate this experiment to microscale radiative transfer one need simply realize that only a fraction of the radiation within a black body escapes from it and is "seen" by a distance cold surface; the fraction is that which impinges on the radiating surface at less than the critical angle for total internal reflection. If we can increase the amount of the radiation within the body that can "escape", we can extract more energy radiatively from that black body. This is exactly what is done by bringing the cold surface close enough to the radiating surface that there is evanescent coupling across the gap.

We have recently developed an analytical model which quantifies this picture and allows us to predict the proximity effect enhancement of the output of TPV cells as a function of the separation between the cell and the black body. The largest enhancement occurs when the indices of refraction of the blackbody and the TPV cell are the same, and we see that there is a maximum proximity factor, given by this index of refraction squared. At a given separation the enhancement is greatest for the longer wavelength cells and the cell output is also greater for the smaller energy gap cells. However, if one does not want to have to cool the cell, one must realize that a 0.35 eV cell is about the narrowest gap cell which can be used at room temperature, i.e., without significant cooling. This appears to be the best choice of cell for the first experimental demonstration of this effect.

The enhancement is actually larger for the lower blackbody temperatures, but the overall cell output increases quickly as the blackbody temperature is increased, so it is desirable to operate with the highest blackbody temperature compatible with a given application. For the initial experiments it is felt that it will be relatively straightforward to operate with a blackbody as high as 500˚C, but that going higher will unnecessarily complicate the initial experiments. It is also worthwhile noting that significant levels of power can be generated even from 200˚C blackbodies by taking advantage of the proximity effect. This means that it will be possible to use MTPV to recover waste heat energy, converting it to electricity, in situations which are now impractical for TPV energy conversion.

Fabrication and Characterization of Microscale Thermophotovoltaic Cells

Personnel

K. Waithe and M. Masaki (C. G. Fonstad, Jr., in collaboration with R. DiMatteo of C. S. Draper Laboratory)

Sponsorship

C. S. Draper Laboratory

We have begun a program of research to provide the first experimental demonstration that a dramatic increase in ThermoPhotoVoltaic (TPV) energy conversion (i.e., a 5 to 10x increase) is obtained by positioning the active diode surface in extreme close proximity to the radiator (i.e., on the order of a tenth of the wavelength of the radiation, or less). The demonstration of this proximity effect is the first step in the creation of a new class of Microscale ThermoPhotoVoltaic (MTPV) devices which promise to make the extraction of electrical energy from a wide variety of heat sources practical and to provide a new class of compact, portable sources of electricity. Moreover, MTPVs will be able to utilize thermal energy now discarded as waste heat, and will enable significant increases in the overall efficiency of many complex systems.

The realization that the conventional blackbody radiation "law" is not valid within a wavelength of a source is not new; that his model was limited to large separations was appropriately pointed out by Max Planck in his original derivation. The fact that the rate of radiative energy transfer is significantly higher than predicted by Planck's law when the source and sink are in such close proximity, however, is a much more recent discovery, and is a phenomenon that has been studied by only a very few individuals interested in radiative heat transfer. And while increased radiative heat transfer between closely spaced bodies has been demonstrated experimentally, this effect remains largely unknown. In 1996, our collaborator, Robert DiMatteo recognized that this same enhanced energy transfer can be exploited to advantage for thermal-to-electrical energy conversion. However to date, there has been no experimental verification or exploration of this microscale thermophotovoltaic effect; our effort that will provide this confirmation and lay the experimental foundation for further development of MTPV systems.

We intend, first, to design and fabricate photovoltaic cells specifically for MTPV applications. These cells will be narrow band gap diodes with highly planar front surfaces. These cells will then be placed in an apparatus which allows a flat, hot surface (the "source") to be brought from greater than 1 μm away to within 0.1 μm of the MTPV cell surface. A plot of the short circuit current of the MTPV cell verses the cell-to-source spacing should show a many-fold increase in the current as the spacing approaches zero. This result would unambiguously confirm the validity of the MTPV concept, and mark the first milestone on the road to practical, widespread MTPV generation of electricity. A full array of experiments are planned, in addition to this basic short circuit current measurement, to fully characterize and quantify MTPV cell operation.

Photonic Bandgap Structures

Personnel

G. S. Petrich, S. Fan, P. R. Villeneuve, G. Steinmeyer, K.-Y. Lim, and D. J. Ripin
(L. A. Kolodziejski, J. D. Joannopoulos, E. P. Ippen, H. I. Smith)

Sponsorship

NSF/MRSEC, ARO

This project represents the combined efforts of the research groups led by Professors John D. Joannopoulos, Leslie A. Kolodziejski, Erich P. Ippen, and Henry I. Smith. Prof. Joannopoulos' research group designs the structures and theoretically calculates the optical properties. Prof. Kolodziejski's group fabricates the various devices with embedded one- and two-dimensional photonic bandgap crystals using III-V compound semiconductor technologies. Prof. Smith's group provides the expertise in nanoscale fabrication. Finally, Prof. Ippen's research group optically characterizes the devices. The complexity of the design, fabrication and characterization of these structures necessitates a strong interaction between the various research groups. In addition, the Microsystems Technology Laboratory (MTL), the NanoStructures Laboratory (NSL) and the Building 13 Microelectronics Fabrication Laboratory are being used to fabricate the PBG structures.

A photonic crystal is a periodic dielectric structure that prohibits the propagation of photons within a certain range of frequencies in all directions. This forbidden band of frequencies translates into a Photonic BandGap (PBG). A defect state can be introduced in the photonic bandgap when the selective removal or addition of dielectric material breaks the dielectric periodicity of a photonic crystal. This defect results in the spatial localization of the defect mode into a volume of approximately one cubic wavelength, yielding a low modal volume, high quality factor resonant microcavity.

- One-Dimensional Photonic Bandgap Devices: Monorail and Air-Bridge Microcavities

The one-dimensional photonic bandgap devices that are being investigated are referred to as monorail and air-bridge microcavity devices. In the monorail microcavity, the photonic crystal consists of a GaAs waveguide with an array of holes etched through the waveguide. The holes are spaced periodically and by introducing additional separation between the holes in the middle of the array, a defect is created. The photonic crystal resides on a layer of aluminum oxide (Al_xO_y) which has a much lower refractive index than GaAs. In the air-bridge microcavity, a photonic crystal that is similar to the photonic crystal in the monorail microcavity device, is suspended in air, resulting in a higher index contrast between the photonic crystal and its surroundings. The devices are designed to resonate at a wavelength of 1550 nm. Both the monorail and air-bridge microcavities have waveguides coupled into and out of the devices to facilitate the optical characterization of these devices.

The fabrication process for the devices utilizes a heterostructure of $GaAs/Al_{0.9}Ga_{0.1}As$ that was grown by gas source molecular beam epitaxy. Subsequently, a series of plasma-enhanced chemical vapor deposition, electron-beam lithography, reactive ion etching, photolithography and wet etch processing steps are employed to fabricate the final devices. The samples are thinned and then cleaved to create the mirror-smooth facets at the waveguide ends for optical coupling.

Using a continuous-wave $NaCl:OH^-$ color center laser with an emission wavelength range of approximately 1500 nm to 1670 nm as a source, the optical transmission spectra from both the monorail and air-bridge microcavity devices were measured. The transmission spectra of the monorail structures exhibited resonances from 1522 nm to 1566 nm with Q ranging from 117 to 136 depending on the cavity size. An increase in the defect size resulted in a shift of the resonance peak to longer wavelengths. The transmission spectra of the air-bridge structures exhibited resonances from 1521 nm to 1633 nm with Q ranging from 230 to 360 depending on the cavity size. As expected, due to the stronger modal confinement in the air-bridge microcavity, the cavity quality factors were larger for the air-bridge structures as compared to the monorail structures.

continued

- Two-Dimensional Photonic Bandgap Light-Emitting Diode

A two-dimensional photonic bandgap crystal inhibits the propagation of light within a range of frequencies in any direction within the plane of the crystal. In the device currently being investigated, the two-dimensional photonic bandgap effect is being used to enhance the extraction efficiency of a Light Emitting Diode (LED) by creating a two dimensional PBG crystal within the top cladding layer of an InGaP/InGaAs quantum well structure. The photonic crystal is designed such that the emission wavelength of the quantum well lies inside the photonic bandgap and hence, does not couple to the guided modes within the active region. Coupling to the guided modes is a considerable source of loss in conventional light-emitting diodes. In the structure being fabricated, this problem is expected to be greatly reduced and the amount of light radiated from the device is enhanced.

The 2-D PBG LED, which is designed to emit at a wavelength of 980 nm, consists of an InGaAs quantum well that is clad by InGaP, an Al_xO_y "spacer-layer" and an Al_xO_y/GaAs distributed Bragg reflector (DBR). The various layers of the LED were first deposited on a GaAs substrate using gas source molecular beam epitaxy. At this stage, the "spacer-layer" is a layer of $Al_{0.98}Ga_{0.02}As$ and the DBR consists of alternating layers of AlAs and GaAs. Using plasma enhanced chemical vapor deposition, direct-write electron beam lithography and reactive ion etching, a 2-D PBG crystal is created within the upper InGaP cladding layer. After the device mesa is formed using photolithography and reactive ion etching, the Al containing layers are oxidized at 435°C using steam carried by N_2. To further improve the extraction efficiency of the LED, the active quantum well region lies on top of a Al_xO_y/GaAs DBR that is designed to reflect the 980 nm light that was initially emitted towards the substrate. The high dielectric contrast between the GaAs and Al_xO_y layers causes the DBR to have a large high-reflectivity bandwidth. By separating the active region from the DBR with a low index Al_xO_y "spacer-layer," a larger portion of the emitted light will be normally incidence on the DBR, thereby increasing the amount of light being extracted from the device.

Currently, the devices are being optically characterized using cathodoluminescence and scanning photoluminescence. The intensity of the λ=980 nm light emitted from a device containing the 2-D PBG crystal is compared to the intensity of the light emitted from a device without the PBG crystal. Simulations have shown that the structure with the PBG crystal should demonstrate at least a five-fold increase in extraction efficiency as compared to the same device without the presence of the photonic crystal.

A Two-Dimensional Photonic-Band-Gap Super-luminescent Light-Emitting Diode

Personnel

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Sponsorship

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A Photonic Band Gap (PBG) is the optical analog of an electronic band gap in a semiconductor. A periodic variation in the dielectric constant forbids certain photon energies within the semiconductor. Specifically, a two dimensional PBG inhibits the propagation of light within a certain range of frequencies in any direction in a plane. In this work, a two dimensional PBG is fabricated in the top cladding layer of an InGaP/InGaAs quantum well structure emitting at $\lambda = 980$ nm. The photonic crystal is designed such that the emission wavelength lies inside the photonic band gap and hence does not couple to guided modes within the semiconductor. Coupling to the guided modes is a major source of loss in conventional light-emitting diodes. In the structure being fabricated, this problem is greatly reduced and the amount of light radiated from the device is enhanced.

The 2-D PBG LED consists of an InGaP/InGaAs active region, an Al_xO_y spacer layer and an Al_xO_y/GaAs Distributed Bragg Reflector (DBR). Figure 6 shows a schematic of the structure along with a completed structure. The 2-D photonic crystal is created by a hexagonal lattice of holes within the upper InGaP cladding layer with a hole-to-hole spacing of 315 nm, and hole diameter of 220 nm. These dimensions center the photonic band gap around the 980 nm emission wavelength of an InGaP/InGaAs quantum well structure. The holes do not penetrate the InGaAs quantum well region, however, to minimize surface carrier recombination. Moreover, the active quantum well region lies on top of a DBR designed to reflect the 980 nm light. The DBR consists of alternating layers of GaAs and Al_xO_y to achieve high dielectric contrast between the layers which leads to a DBR with a wide stop band. The active region is separated from the DBR by an Al_xO_y buffer layer. Separation by a low index layer forces a larger portion of the emitted light to have normal incidence on the DBR which increases the amount of reflected light.

The fabrication of the 2D PBG LEDs utilizes gas-source molecular beam epitaxy, direct-write electron-beam lithography, Reactive-Ion Etching (RIE) and oxidation processes. The device structure is grown using gas-source molecular beam epitaxy. The separation layer is initially grown as $Al_{.98}Ga_{.02}As$ and the DBR consists of AlAs and GaAs layers. A SiO_2 layer is deposited on the grown structure using plasma enhanced chemical vapor deposition. The holes are defined in PMMA by direct-write electron-beam lithography. The electron beam writes a square pattern in the PMMA to represent each hole. The beam size, however, is larger than the step size for translating the electron beam. This leads to the desired circular pattern following development.

The PMMA is used as a mask in transferring the hexagonal pattern to the SiO_2 layer using RIE. This is accomplished by RIE with a CHF_3 plasma using 15 second steps in between 1 minute cool-down steps, during which the electrode is back-cooled with He gas flow. The purpose of the cool-down step is to prevent flowing of the PMMA mask. The SiO_2 mask is subsequently used in the RIE of the holes into the upper InGaP cladding layer using RIE with a CH_4/H_2 plasma in a 1:4 gas flow ratio. The mesas are next defined using photolithography followed by RIE. The final step in the device fabrication is the wet thermal oxidation of the $Al_{.98}Ga_{.02}As$ separation layer and the AlAs DBR layers. Figure 7 is a scanning electron micrograph of the hexagonal array of holes within the upper InGaP cladding layer.

continued

Currently, the devices are being tested using cathodoluminescence. A high energy beam of electrons excites carriers within the active region which subsequently recombine in the quantum well. The intensity of the $\lambda = 980$ nm light emitted from the quantum well is measured using a Ge detector. The intensity of light extracted from a device containing the 2-D PBG is compared to that of a device without the PBG. Simulations have shown that this structure should demonstrate at least a five-fold increase in extraction efficiency as compared to the same device without the presence of the photonic crystal.

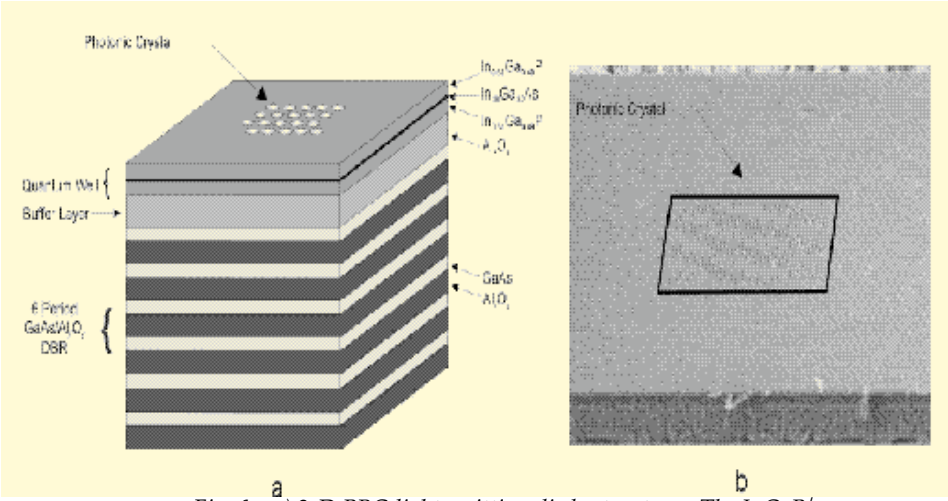

Fig. 6: a) 2-D PBG light emitting diode structure. The InGaP/InGaAs quantum well structure emits at $\lambda = 980$ nm. The active region is separated from the DBR by a low refractive index Al_xO_y separation layer. This separation increases the amount of emitted light reflected from the DBR. A hexagonal lattice of holes in the top layer of the device eliminates coupling of emitted light to guided modes. b) SEM micrograph of 2-D PBG light emitting diode.

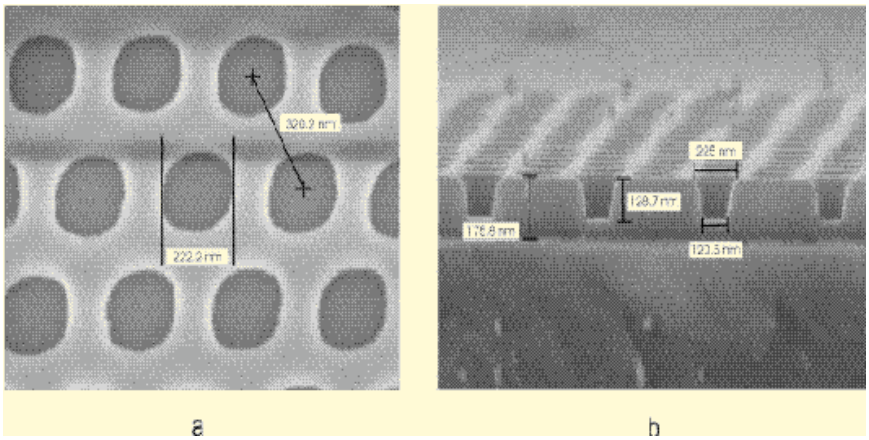

Fig. 7: a) Hexagonal array of holes forms a photonic crystal in the top InGaP layer of the LED. The holes are designed to forbid the guiding of $\lambda = 980$ nm light and hence increase the amount of light radiating from the device. b) Cross-sectional view of 2-D PBG. The holes do not penetrate the InGaAs quantum well to avoid surface recombination.

Silicon Photonic Band Gap, Microcavity and Waveguide Structures

Personnel

T. Chen, K. Chen, D. Lim and K. Wada (L.C. Kimerling)

Sponsorship

NSF/MRSEC, and NTT

In this project, we have been developing a key element for Si microphotonics, i.e. microcavities functioning in the range of $\lambda = 1.54$ μm. This wavelength is compatible with fiber optic communication systems. These structures are key devices for large scale WDM networks on Si LSI chips. In order to realize the microcavities, we have employed two approaches: photonic bandgap and microring resonators. The PBG is the optical analog of a semiconductor. An electromagnetic wave travelling through a PBG structure encounters a large, periodic change in the dielectric constant. This periodicity causes bands of frequencies to be disallowed for propagating through the material. We have employed two methods to fabricate photonic crystals: chemical vapor deposition and sol-gel method. First, we have fabricated this structure using chemical vapor deposition (CVD) processes. The periodic dielectric constant consists of alternating films of Si and SiO_2, which are most widely used in Si-CMOS LSI processes. Er has been implanted into a polysilicon microcavity layer. We have developed a polysilicon:Er process that yields emission of light at comparable intensities to single crystals.

Based on coupling of photons with the μ-cavity, the Er spontaneous emission would be enhanced by the order of quality factor Q of the cavities, which is around 100 to 1000 in our case. We are currently measuring the emission enhancement by photoluminescence.

The periodic dielectrics are now being fabricated by wafer bonding and delamination. Single crystalline Si layers and thermally grown SiO_2 layers were bonded in four layers to form a one-dimensional PBG. Preliminary data show high quality PBG in excellent agreement with theory prediction.

The sol-gel technique is an inexpensive method for producing a wide variety of thin oxide-based films amenable to large-scale manufacturing. In brief, the method involves the controlled hydrolysis and polymerization of an organometallic precursor followed by densification at elevated temperatures. For thin film applications, a variety of techniques are available for depositing the film. In our work, all films have been spin-coated. We choose TiO_2 (n=2.8) and SiO_2 (n=1.45) for their relative ease of preparation and large refractive index contrast (Dn = 2.8/1.45 [a] 2.0). Other materials systems to consider include various ferroelectrics that have high n. We have built an interference filter using TiO_2/SiO_2 with a PBG centered around λ=1.5 μm and reflectivity greater than 85%. We are currently fabricating the very first microcavity device based on the sol-gel technique.

Three-dimensional PBGs operating in the near-IR and optical regimes can be used for enhanced light emission and waveguiding. To obtain a full, omnidirectional bandgap, 3D PBGs must exhibit certain configurations of refractive index periodicity. Self-assembly of monodisperse colloidal particles is an elegant method for producing an FCC arrangement, which can lead to a full bandgap when the index contrast between the particles and matrix is Dn>3. With the aid of polyelectrolyte surfaces, it may be possible to pattern specific designs on a substrate on which to conduct the self-assembly. An understanding of the self-assembly process is needed and techniques to obtain highly ordered particle arrays are being investigated.

continued

Novel microring resonator structures have also been designed, fabricated, and implanted with Er. Resonances with Qs of 250 were observed at $\lambda = 1.55$ µm with rings of 3 to 5 µm in radius) Large diameter rings (100 mm radius) have recently been fabricated and implanted with erbium. The large diameter rings are designed to resonate with the Er transition line at 1.54 µm. We are currently measuring the luminescence enhancement from a ring resonator.

Our ring resonators have demonstrated cavity resonances with Q's around 300. They are prime candidate device structures for luminescence enhancement of Er-doped silicon. Rings with 3 to 5 µm radii exhibit a Free Spectral Range (FSR) of about 20 µm between resonance peaks. Because the linewidth of the Si:Er main transition is less than 10 µm, a ring resonator with a smaller FSR is required. Ring resonators with a radius of 100 µm were computed to manifest a FSR of less than 10 µm and were designed to have Q's around 10,000. These rings have been fabricated and doped with Er. Their spectral properties are currently under investigation.

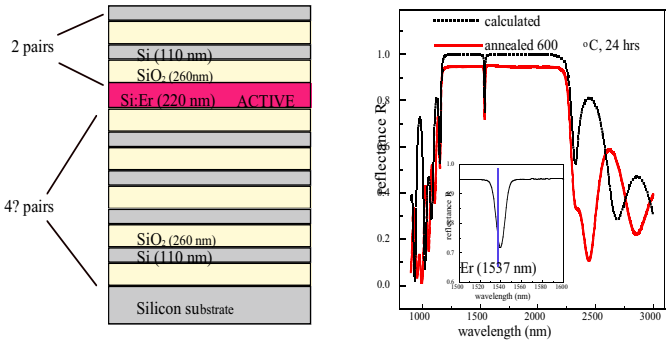

Fig. 8: (left) Si/SiO_2 microcavity with Si:Er active layer. The cavity has an active layer that is tuned for 1537 nm. (right) Reflectance spectrum of microcavity with resonance at 1537 nm. The cavity quality factor is ~300.

(fabricated at Polaroid-Norwood).

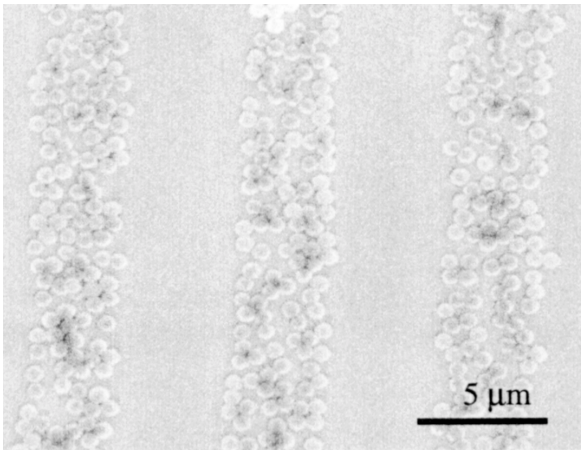

Fig. 9: SEM micrograph of SiO_2 spheres (diameter 0.7µm) deposited on bilayers of LPEI/PAA polyelectrolyte stripes. The stripes are patterned via micrcontact printing, and have a width of 4µm.

Fabrication of 3-D Photonic Bandgap Structures

Personnel

M. Qi (J. Joannopoulos and H. I. Smith)

Sponsorship

NSF

Three-dimensional Photonic Bandgap Structures (PBG) are true optical analogs of semiconductors in a sense that they present omni-directional bandgaps for photons. Figure 10 illustrates the 3D structure we are attempting to fabricate using planar fabrication techniques. Modeling indicates that it has a large, complete bandgap, and allows defects to be introduced in a controlled manner. Figure 11 illustrates the completion of the first two layers of the structure. The amorphous silicon layers are sputter deposited at room temperature, and the patterns are aligned and defined using our VS2A Scanning-Electron-Beam Lithography (SEBL). The misalignment is shown to be within 45 nm, which is sufficient to support the upper layer structures. Then SiO_2 is conformally deposited via high-density plasma-enhanced CVD at 80°C, which also provides planarization. The etch back of the SiO_2 to the level of the Si is done by a combination of controlled dry etching with CHF_3/O_2 and wet etching with diluted HF. This approach should be extendable to five to seven layers, which are required to achieve the true 3-D bandgap.

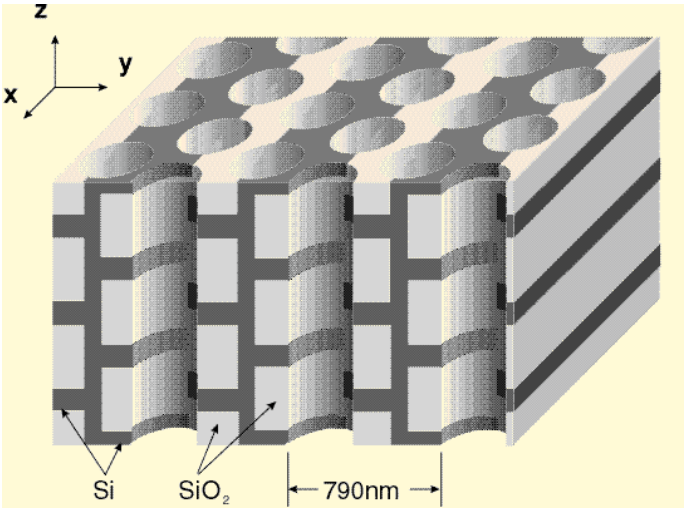

Fig. 10: Depiction of a 3D photonic-bandgap (PBG) crystal to be fabricated at a 790 nm period. The dark gray and light gray regions correspond to Si, with a high index (3.4), and SiO_2, with low index (1.4), respectively. The SiO_2 can be removed after the structure is formed, and that will increase the ideal bandgap from 14% to 21 % of the midgap frequency, which c orresponds to a wavelength of 1.53 μm. The design enables planar fabrication techniques to be applied.

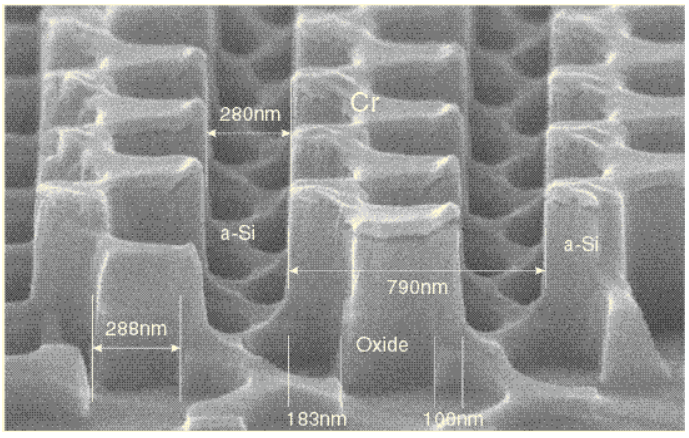

Fig. 11: Scanning-electron micrograph of the patterned second layer of a 3-D photonic-bandgap structure, showing amorphous Si on top of the first-layer structure, with groves filled with SiO_2. The second layer structure is shifted by half of the periods in both x and y directions. An intentional overetch into the first layer is also observable.

Fabrication of an Integrated-Optical Grating-Based Matched Filter for Fiber-Optic Communications

Personnel

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Sponsorship

AFOSR

For future all-optical communications systems, filters are needed for a wide variety of network functions including dispersion-compensation, wavelength multiplexing, gain flattening, and noise suppression. This project seeks to develop the technology for building such filters, using integrated Bragg gratings. Integrated gratings provide a convenient way to perform filtering operations, in a package that can be integrated on a chip, along with other electronic and optical components of the communications system.

Figure 12 depicts the structure of a novel integrated-optical filter we are developing in the Nanostructures Lab. The filtering action is performed by the shallow corrugation etched into the top surface of the Ge-doped silica waveguide. As depicted, the period of the grating is ~530 nm, which places the spectral response in the 1550-nm communications band. In order to separate the reflected filtered signal from the incident input signal, a Mach-Zehnder interferometer is used. In this configuration, light is launched into the top waveguide and a codirectional coupler splits the signal between the upper and lower arms of the interferometer. The reflected signals are recombined in the coupling region and emerge in the lower port of the device.

The spectral response of this device can be tailored by adjusting the geometry of the Bragg grating. For example, to achieve a notch-type filter with high out-of-band rejection, the grating amplitude can be apodized over the length of the device. To construct a grating filter for dispersion-compensation, the grating period could be gradually chirped over its length. In this project, our goal is to build a grating filter that has a spectral response that is matched to a communications signal of interest. The integrated Bragg-grating is an ideal filter for such an application, because if the length and shape of the grating are properly selected, the reflection spectral response of the grating can be made to have a characteristic sinc shape which is matched to that of a binary communications signal.

Other laboratories are developing similar devices using fiber-Bragg-gratings. In such devices, the grating is formed via a UV-induced index change in the core of an optical fiber. Some researchers are attempting to construct integrated filters by applying the same UV-induced technique to a planar waveguide structure. Our work is unique in that the grating is formed by physically etching a corrugation onto the integrated waveguide structure. This approach allows us to: (1) tailor the shape of the grating on an almost tooth-by-tooth basis, (2) take advantage of existing nanoalignment techniques to achieve accurate alignment of the grating to the waveguides without any kind of in-situ monitoring, and (3) circumvent the inherent limitations of photorefractive gratings. For these reasons, we believe our approach is not only more flexible, but also more suitable for mass-production of highly integrated optics.

As described in our related article concerning the InP channel-dropping filter, we have developed a flexible and robust method of constructing integrated Bragg-grating-based devices which solves some of the critical problems of alignment, period selection and grating fidelity. This approach is also applied to these silica waveguide devices.

Our fabrication sequence uses photolithography to define the waveguide features of the device, and a combination of interferometric lithography, e-beam lithography, and x-ray lithography to print the fine-period grating structures.

continued

At present, we have fabricated and measured a set of preliminary waveguide-coupler devices. These initial devices, which do not have a corrugated grating on the top surface, allow us to measure the propagation loss, fiber-coupling loss, polarization dependence and waveguide-to-waveguide directional coupling. For these coupler devices, we measured a total insertion loss lower than 1 dB, which includes propagation loss, fiber-coupling loss, and bending loss. Having characterized the waveguide structure, we have now turned our attention to the Bragg grating. Our current efforts focus on investigating the overgrowth properties of silica cladding over fine-period grating structures.

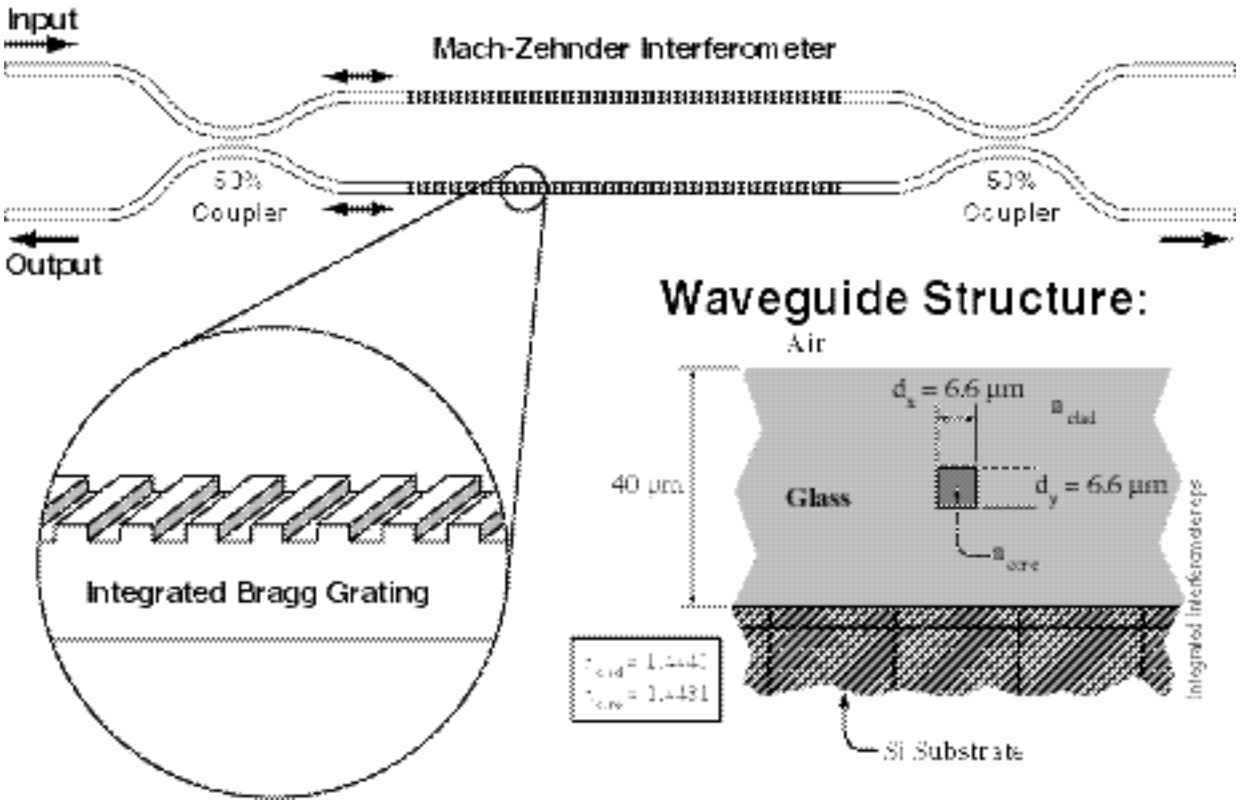

Fig. 12: Diagram of an integrated optical matched-filter. The waveguide consists of a germanium-doped SiO_2 core, 6.6 μm wide and tall, surrounded by SiO_2 cladding. The 10 mm-long Bragg grating is formed by etching a shallow, 535 nm-period grating onto the top of the waveguide before the upper cladding layer is deposited. The waveguide interferometer is designed to redirect the reflected, filtered signal to a separate output port.

Fabrication and Design of an Integrated Channel-Dropping Filter in InP

Personnel

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(J. N. Damask, L. A. Kolodziejski, and H. I. Smith)

Sponsorship

AFOSR

Wavelength-Division Multiplexing (WDM) is a strategy for utilizing the enormous bandwidth capacity of optical communications systems by multiplexing many data signals, each placed at a different wavelength. In order to realize the full potential of WDM, narrow-band filters are needed to differentiate between the many wavelength channels of interest.

The Channel-Dropping Filter (CDF) is a critical component for such WDM systems. The function of the CDF is to drop (or add) one wavelength channel from a multi-channel bus. The key advantage of the CDF approach over many currently employed technologies is that one wavelength channel may be accessed without disturbing any of the remaining channels, and without ever converting the data into an electronic signal. Thus, it offers a flexible and extendable means of all-optical routing.

Although it is widely recognized that WDM will play an increasingly important role in future communications systems, the fabrication of integrated optical components needed for WDM presents some unique challenges that have not been fully appreciated or adequately addressed. In this project, we demonstrate a novel process for fabricating integrated grating-based optical devices, which addresses some of these unique challenges.

Figure 13 depicts the Channel-Dropping Filter (CDF) which we are in the process of building in the Nanostructures Lab. The filtering action takes place in the quarter-wave-shifted Bragg gratings located above and below the bus waveguide. These gratings act as narrow-band resonators, which are only excited by one resonant wavelength channel.

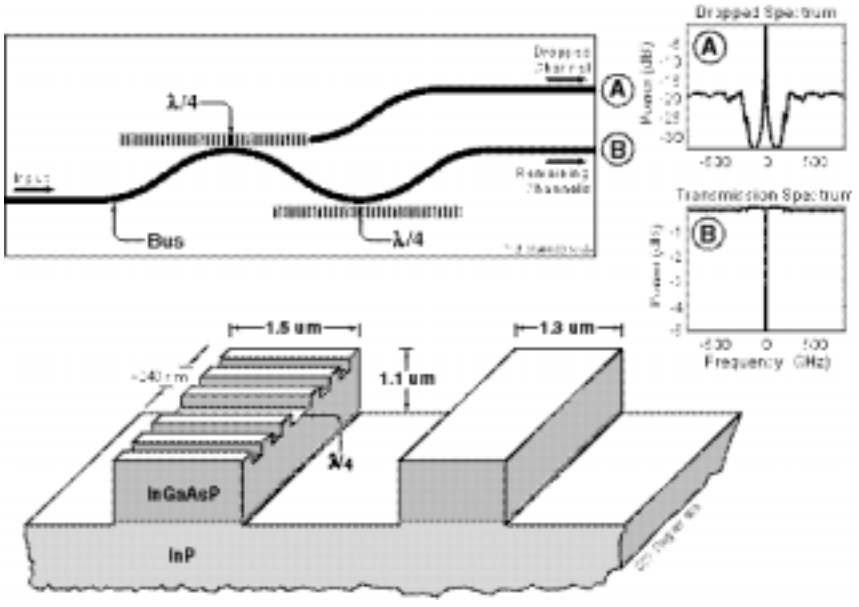

Fig. 13: Diagram of the channel-dropping filter. As depicted in the upper portion, a multi-wavelength input signal is launched along the bus waveguide. One resonant wavelength-channel is dropped in the upper port of the device. As shown in the lower portion of the Figure, the waveguide is composed of InGaAsP, surrounded by an InP cladding. Note: the final top layer of InP is not depicted.

continued

Some of the fabrication challenges presented by this device are: (1) a fine-pitch (244.4 nm) grating must be etched into the top of the much taller (1.2 μm) waveguide, and its period must be controlled to within 0.1 nm. (2) The k-vector of the grating must be aligned with the axis of the waveguide to within 1.7 milliradians; any misalignment greater than this will cause the mode to lose guidance and scatter excessively. (3) Abrupt quarter-wave phase shifts must be placed at specified locations in the grating. (4) The InP must be grown over the grating without altering the square-wave shape of the underlying quaternary.

To meet these requirements, we have developed a "Dual-Hardmask Process" (DHP), depicted in Figure 14. This DHP enables us to avoid the difficult problem of lithographically patterning 0.1 micron features over extreme topography. We first lithographically define the grating in a hardmask, using x-ray lithography. We then deposit a second hardmask directly on top of the grating, and define the waveguide pattern in it using contact photolithography.

Once the two hardmasks are patterned, the waveguides and gratings are formed by a sequence of dry etching steps. The only constraint on the choice of hardmask materials is that the one on top can be removed without affecting the one below. We use Ni for the waveguide-level mask and Ti for the underlying grating-level mask. Figure 14 includes a micrograph of a structure fabricated using this process.

The grating-level x-ray mask is written using a technique which we call Spatially-Phase-Locked E-Beam Lithography (SPLEBL). In SPLEBL, interferometric lithography is first used to generate a coherent grating pattern on the x-ray mask. Then e-beam lithography is used to write the arbitrary patterns required by the device. During the e-beam writing, the interferometrically-generated grating pattern on the mask is sampled in order to determine the absolute beam position. This technique ensures that the e-beam writes a coherent grating, free of stitching errors.

The waveguide mask is written at a commercial mask supplier using a MEBES tool. Both the x-ray mask and the optical photomask have complementary alignment marks to enable angular alignment of the grating k-vector with the waveguide axis.

We believe that the fabrication techniques developed for this device will prove useful for constructing a variety of related, active and passive grating-based devices.

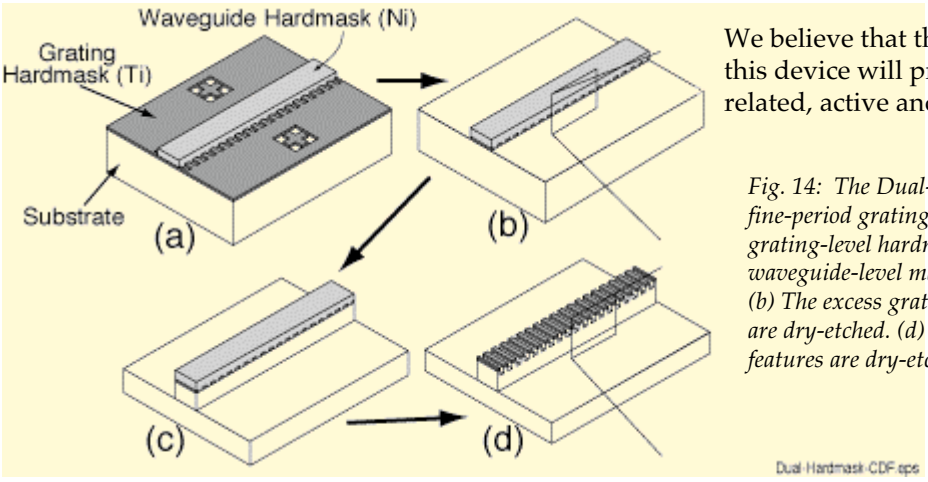

Fig. 14: The Dual-Hardmask Process is used to pattern the fine-period gratings atop the InGaAsP waveguides. (a) First the grating-level hardmask is patterned over the substrate, then the waveguide-level mask is patterned over the grating-level mask. (b) The excess grating mask is stripped. (c) The waveguide features are dry-etched. (d) After removal of the waveguide mask, the grating features are dry-etched.