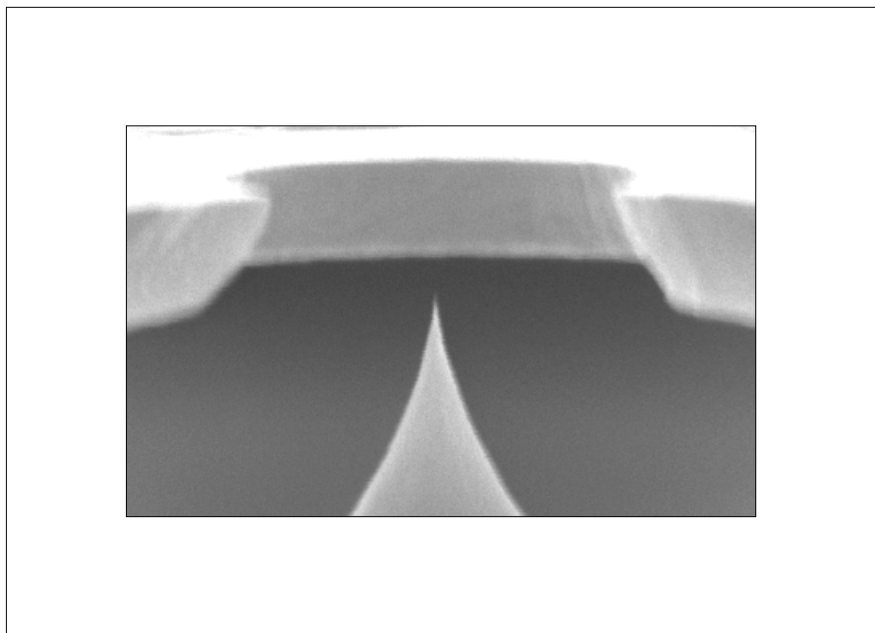

Modeling and Simulation



SEM of the Si Field Emitter tip. (Courtesy of S. D. Senturia and A. I. Akinwande)

Modeling and Simulation

- *Modeling of Advanced Device Structures*
- *MOSFET Scaling and Device Design for Low Temperature Operation*
- *First-Order CMOS Device Model*
- *Efficient 3-D Interconnect Analysis*
- *Numerical Techniques for Integral Equations*
- *Modeling the Effect of Interconnect Variation on Circuit Performance*
- *Simulation Algorithms for RF Circuits*
- *Software Tools for Process-Sensitive Reliability Assessments of IC Designs*
- *Modeling of Grain Growth in Thin Films*
- *Modeling of Interconnect Reliability*
- *Simulation of Electromigration-Induced Failure of IC Interconnects*
- *Electric Field Simulations for Field Emission Devices*
- *Simulation Tools for Micromachined Device Design*

Modeling of Advanced Device Structures

Personnel

I. J. Djomehri, Z. Lee, M. B. McIlrath (D. A. Antoniadis)

Sponsorship

SRC

As MOSFET dimensions are reduced to the submicron level, the electrical performance is critically dependent on the two-dimensional (2D) distribution of dopant concentrations in the semiconductor. In order to accurately characterize, predict, and control the device topology, and therefore the device behavior, it is essential to obtain an accurate description of the 2D doping profile. Moreover, knowledge of an accurate 2D distribution enables one to calibrate transport and mobility models, making possible accurate device simulations.

However, the lack of a mature 2D doping profiling technique has been an obstacle in achieving such goals. Here, we have demonstrated a modern, comprehensive technique for the extraction of 2D profiles in submicron MOSFETs: inverse modeling. The main advantages of this technique include: (1) the ability to extract 2D doping profiles (including effective channel length) of very small devices (down through sub-100 nm); (2) immunity to parasitics; (3) low dependence on mobility model; (4) non-destructive measurement; and (5) simplicity of data preparation and ease of use. Data from subthreshold I-V characteristics is a strong function of doping and can accurately determine a profile, especially near the channel. Data from Cgds-V curves promises to provide more information (and thus more accurate and faster convergence) near the source/drain regions.

The approach of inverse modeling is flexible and can be used to engineer sub-100 nm devices. For instance, one may specify various desired electrical properties (e.g., high drive current, low DIBL, low off current) and generate a doping profile that will achieve these results. Hence, a set of "well-tempered" devices (those with desirable characteristics) in the sub-100 nm regime are being created which will be used to compare advanced simulation techniques and models. Also, the technique has been applied to a variety of device structures, including asymmetric designs.

We have applied the inverse modeling technique to the Super-Steep Retrograde (SSR) devices fabricated at MIT. The extracted profile of a 0.1 μm effective channel length device is shown in Figure 1. We have also demonstrated the accurate device performance prediction capability that is possible with this technique, once appropriate mobility models have been calibrated. Figure 2 shows a comparison between the measured and predicted I-V characteristics of a 0.1 μm channel length SSR device. The potential power of this method is apparent.

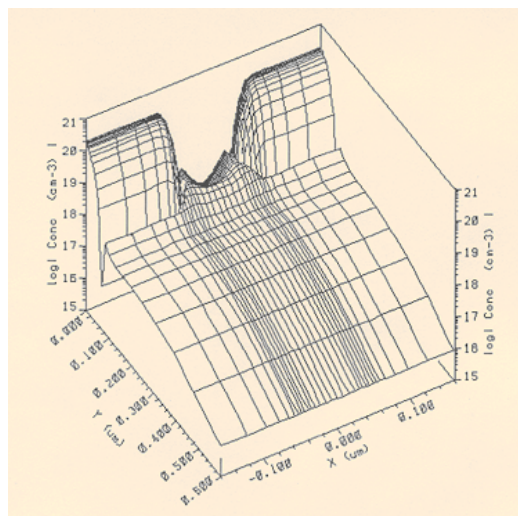


Fig. 1: Extracted 2D doping profile of a SSR device having source/drain halo dopings. The device has $L_{\text{gate}} = 0.1 \mu\text{m}$, $t_{\text{ox}} = 50 \text{ \AA}$, and $W = 10 \mu\text{m}$.

continued

MOSFET Scaling and Device Design for Low Temperature Operation

Personnel

K. M. Jackson, A. Lochtefeld
(D. Antoniadis)

Sponsorship

DARPA, SRC

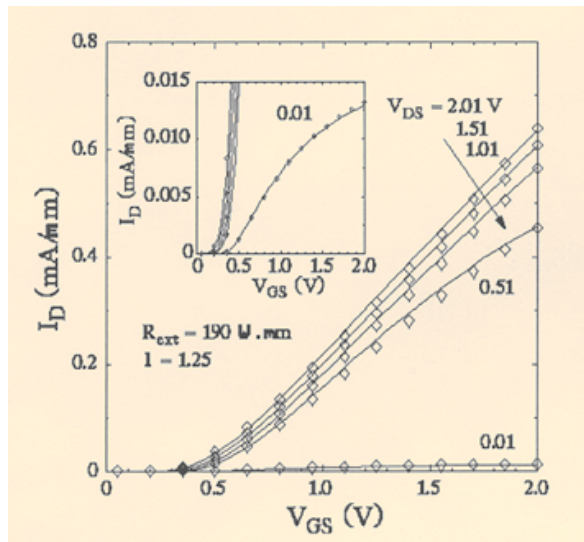


Fig. 2: Comparison between measured and predicted I - V characteristics using calibrated mobility models. The device has a SSR channel profile with $L = 0.1 \mu\text{m}$, $t_{ox} = 50 \text{ \AA}$, and $W = 10 \mu\text{m}$. Simulated data are denoted by symbols.

Lowering the operating temperature of a device has long been viewed as a way to extract the ultimate performance out of a given gate length device. This project is exploring the concept of using temperature as a scaling parameter to eliminate the ever more pressing tradeoff between device performance and leakage current (I_{off}). In addition to describing a general device design space, this project is exploring the tradeoff between performance at lower operating temperatures and testability at room temperature.

The traditional parameters for device design, channel doping and oxide thickness, have little effect on the inverse subthreshold slope. Thus as the threshold voltage is scaled, the device's off-current increases. However, since the inverse subthreshold slope is proportional to absolute temperature, scaling temperature by the same factor as V_{th} will keep I_{off} constant (Figure 3).

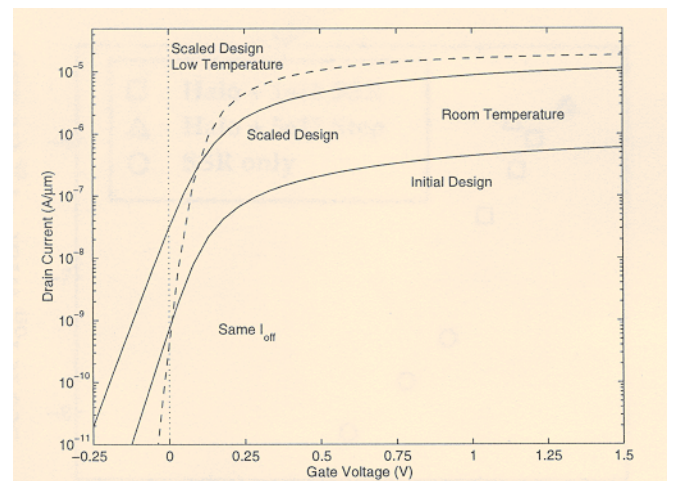


Fig.3: Schematic comparison of I_{ds} - V_{gs} curves of an initial design to a scaled design (L & V_{th}) demonstrating the constant I_{off} possible with lower operating temperatures.

In order to map out the design space of I_{off} and performance, optimizations constrained by three different scaling scenarios were used to create device designs for channel lengths from 220 nm to 40 nm. The optimizations used a set of analytical equations for short channel device characteristics which have been shown to match a family of N-MOSFETs from $L_{eff}=5 \mu\text{m}$ to 100 nm, and thus model SCE and velocity saturation well.

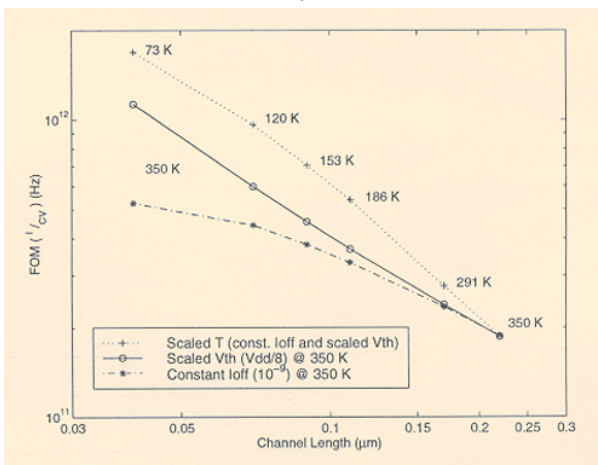


Fig. 4A: Comparison of switching speed ($FOM=I/CV$) for the three different scaling scenarios.

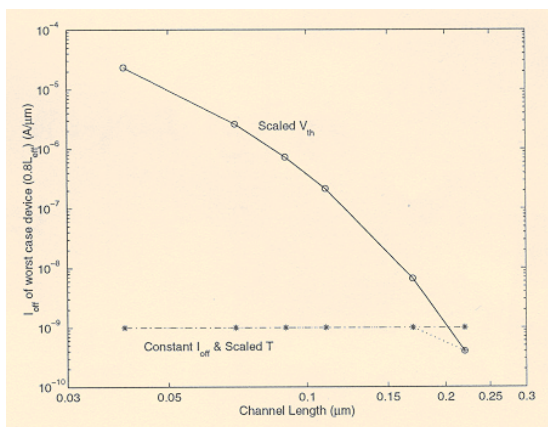


Fig. 4B: Corresponding I_{off} of the worst case device ($0.8L_{eff}$) for the scaling scenarios in Figure 4A.

The results of these optimizations are shown in Figure 4 A&B with each point having a unique V_{dd} , t_{ox} , and N_b that give the characteristics shown. The results show that fixing I_{off} (V_{th} does not decrease) yields a figure of merit (I/CV) that scales more slowly than $1/L$, while scaling V_{th} with V_{dd} (a constant field scaling like approach) yields a FOM that grows at $1/L$ as would be expected, but gives unacceptably high off-currents (Figure 4B). In the scaled temperature scenario, where T , N_b , and V_{bs} (substrate bias) are free to be adjusted (V_{dd} and t_{ox} are the same as the scaled V_{th} case), both the fixed I_{off} and scaled V_{th} constraints can be met. The resulting performance is up to 1.6x that of the scaled V_{th} scenario, because of the increased mobility and saturation velocity at lower temperatures.

To further investigate the design space for 50 nm channel lengths, a set of simulations using the 2-D numerical device simulator MEDICI were performed. Device designs using a non-uniform channel doping created with either Halos or a SSR profile were picked to achieve a low threshold voltage (V_{th}) at low temperature (using a forward biased V_{bs}) as well as to a reasonable off-current at room temperature (using a reverse biased V_{bs}) which would allow room temperature wafer-level tests and even burn-in of circuits.

The results of these simulations suggest a tradeoff between performance at low temperatures and off-current at room temperature (Figure 5). Devices with heavier sub-surface doping have a large back-bias (V_{bs}) control, which results in a greater ability to lower the off-current at room temperature. However, these devices have significantly higher drain capacitances and slightly lower drive currents than devices with lower sub-surface doping, resulting in lower performance.

The design space evaluation and simulations done so far in this project demonstrate the viability of device design for room temperature testing of 50 nm devices optimized for low temperature operation. Current efforts are focused on fabricating a set of 50 nm devices to evaluate the simulated results.

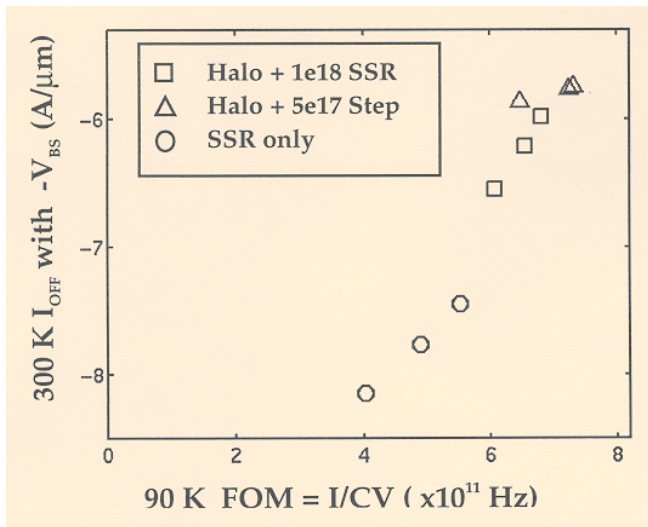


Fig. 5: Room temperature I_{off} (with substrate bias) versus device performance at 90K for 9 different 50nm devices, illustrating the tradeoff between low temp. performance and room temp. testability.

Personnel

T. Payakapan (J. A. del Alamo)

Sponsorship

SRC

CMOS device design is usually carried out using complex two- and three-dimensional device modeling tools. While these tools provide an accurate simulation environment, they require a complex grid management system and a large number of input parameters, which often times, are not accurately known. There is a need for a simple, first-order device model that can be used in road map planning, sensitivity analysis, and microelectronics education.

In this project, we are constructing an analytical framework to form the basis for a compact and efficient physics-based device simulation environment for CMOS. Over the years, a wealth of analytical models have been developed to describe a variety of MOSFET device physics aspects. The range of applicability of these models is often limited. As a consequence, it is essentially impossible to develop a simple analytical formulation that can be reasonably accurate for any choice of device parameters. To overcome this difficulty, our model is constructed to be reasonably accurate for “well-designed” devices, since these are the only ones that eventually reach the manufacturing stage. A well-designed device is a device with sufficient electrostatic integrity, that is, good isolation between the output and the input. The demand of good electrostatic integrity substantially narrows down the range of required models and simplifies their development.

Using only five input parameters: polysilicon gate length, effective channel length, oxide thickness, junction depth, and well doping level, we have demonstrated that an analytical first-order CMOS device model has the capability of predicting key device figures of merit for digital applications. The simplicity of the model makes it easier to understand the role of important parameters in the design process and the trade-offs that device designers face.

The accuracy of the model is tested by comparing against measurements from actual devices fabricated at MIT. Ongoing work is directed at improving the model to better match device characteristics. Towards that end, source and drain resistance has been added to the model (see Figure 6). This has resulted in an improvement in the predictive power of deep-submicron devices. Next the body effect, inversion-layer quantization, and a gate-induced drain lowering will be added to make the model more accurate.

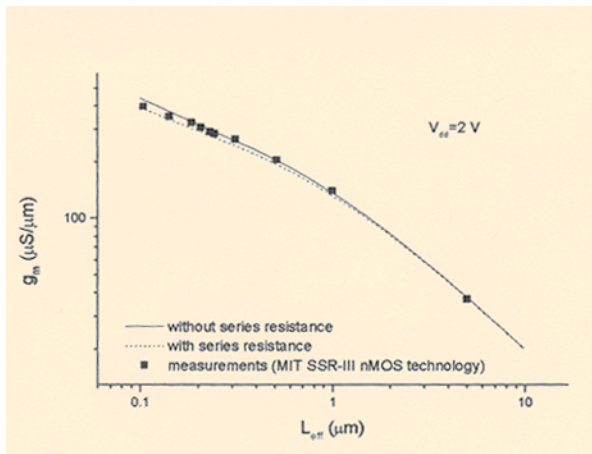


Fig. 6: Measurements and Model Predictions for Transconductance vs. Effective Gate Length for a supply voltage of 2V. The data is from devices fabricated at MIT.

Personnel

I. Balk, M. Chou, J. Kanapka, F. Wang, J. F. Wang, J. Tausch (J. White)

Sponsorship

DARPA, SRC, IBM, Harris Semiconductor, MAFET Consortium

We have developed multipole-accelerated algorithms for computing capacitances and inductances of complicated 3-D geometries, and have implemented these algorithms in the programs FASTCAP and FASTHENRY. The methods are accelerations of the boundary-element or method-of-moments techniques for solving the integral equations associated with the multiconductor capacitance or inductance extraction problem. Boundary-element methods become slow when a large number of elements are used because they lead to dense matrix problems which are typically solved with some form of Gaussian elimination. This implies that the computation grows as N^3 , where N is the number of panels or tiles needed to accurately discretize the conductor surface charges. Our new algorithms, which use Krylov subspace iterative algorithms with a multipole approximation to compute the iterates, reduces the complexity so that accurate multiconductor capacitance and inductance calculations grow nearly as NM where M is the number of conductors. For practical problems which require as many as 10,000 panels or filaments, FASTCAP and FASTHENRY are more than two orders of magnitude faster than standard boundary-element based programs. Manuals and source code for FASTCAP and FASTHENRY are available from our web site (rle-vlsi.mit.edu).

In more recent work, we have been developing an alternative to the fast-multipole approach to potential calculation. The new approach uses an approximate representation of charge density by point charges lying on a uniform grid instead of by multipole expansions. For engineering accuracies, the grid-charge representation has been shown to be a more efficient charge representation than the multipole expansions. Numerical experiments on a variety of engineering examples arising indicate that algorithms based on the resulting "precorrected-FFT" method are comparable in computational efficiency to multipole-accelerated iterative schemes, and superior in terms of memory utilization.

The precorrected-FFT method has another significant advantage over the multipole-based schemes, in that it can be easily generalized to some other common kernels. Preliminary results indicate that the precorrected-FFT method can easily incorporate kernels arising from the problem of capacitance extraction in layered media. More importantly, problems with a Helmholtz equation kernel have been solved at moderate frequencies with only a modest increase in computational resources over the zero-frequency case. An algorithm based on the precorrected-FFT method which efficiently solves the Helmholtz equation could form the basis for a rapid yet accurate full-wave electromagnetic analysis tool.

Reduced-order modeling techniques are now commonly used to efficiently simulate circuits combined with interconnect. Generating reduced-order models from realistic 3-D structures, however has received less attention. Recently we have been studying an accurate approach to using the iterative method in the 3-D magnetoquasistatic analysis program FASTHENRY to compute reduced-order models of frequency-dependent inductance matrices associated with complicated 3-D structures. This method, based on a Krylov-subspace technique, namely the Arnoldi iteration, reformulates the system of linear ODE's resulting from the FASTHENRY equation into a state-space form and directly produces a reduced-order model in state-space form. The key advantage of this method is that it is no more expensive than computing the inductance matrix at a single frequency. The method compares well with the standard Pade approaches and may present some advantages because in the Arnoldi-based algorithm, each set of iterations produces an entire column of the inductance matrix rather than a single entry, and if matrix-vector product costs dominate then the Arnoldi-based algorithm produces a better approximation for a given amount of work. Finally, we have shown that the Arnoldi method generates guaranteed stable reduced order models, even for RLC problems.

Our recent work has focussed on fast techniques of model reduction which generate low order models of the interconnect directly from the discretized Maxwell's equations under the quasistatic assumption. When combined with fast potential solvers, the overall algorithm efficiently generates accurate models suitable for coupled circuit-interconnect simulation.

The design of single chip mixed-signal systems which combine both analog and digital functional blocks on a common substrate is now an active area of research, driven by the relentless quest for high-level integration and cost reduction. A major challenge for mixed-signal design tools is the accurate modeling of the parasitic noise coupling through the common substrate between the high-speed digital and high-precision analog components. We are working on a sparsification method based on eigendecomposition which handles edge effects more accurately than previously applied multipole expansion techniques, and then combine the sparsification approach with a multigrid iterative method which converges more rapidly than previously applied Krylov-subspace methods. Results on realistic examples demonstrate that the combined approach is up to an order of magnitude faster than the sparsification plus a Krylov-subspace method, and orders of magnitude faster than not using sparsification at all.

Numerical Techniques for Integral Equations

Personnel

T. Korsmeyer, J. Singer, J. Tausch, J. F. Wang (J. White)

Sponsorship

SRC, DARPA, MURI

Finding computationally efficient numerical techniques for simulation of three dimensional structures has been an important research topic in almost every engineering domain. Surprisingly, the most numerically intractable problem across these various disciplines can be reduced to the problem of solving a three-dimensional potential problem with a problem-specific Greens function. Application examples include electrostatic analysis of sensors and actuators; electro- and magneto- quasistatic analysis of integrated circuit interconnect and packaging; and potential flow based analysis of wave-ocean structure interaction.

Although the boundary element method is a popular tool to solve the integral formulation of many three-dimensional potential problems, the method become slow when a large number of elements are used. This is because boundary-element methods lead to dense matrix problems which are typically solved with some form of Gaussian elimination. This implies that the computation grows as cubically with the number of unknowns tiles needed to accurately discretize the problem. Over the last decade, algorithms with grow linearly with problem size have been developed by combining iterative methods with multipole approximations. Our work in this area has been to develop precorrected-FFT techniques, which can work for general Greens functions, and Wavelet based techniques, which generate extremely effective preconditioners which accelerate iterative method convergence.

The development of fast boundary-element based solvers has renewed interest in developing well-conditioned integral formulations for a variety of engineering problems. We have developed second-kind formulations for the electrostatics problem that directly yields the surface charge distribution on conductors, and have developed techniques which insure accuracy in the numerically computed capacitances given arbitrarily shaped dielectric materials of arbitrarily high permittivity.

Modeling the Effect of Interconnect Variation on Circuit Performance

Personnel

V. Mehrotra
(D. Boning and J. Chung)

Sponsorship

DARPA, PDF Solutions, IBM

In order to study the impact of long range spatial and pattern dependent variation on circuit performance, CAD tools must be extended and integrated in innovative ways. In this work, we are developing the CAD infrastructure to study device and interconnect variation impact on circuit performance.

In previous work, we developed a method to accurately extract a global path geometry that includes both nearby interconnect structures and accounts for variation in the thickness of interlevel dielectrics (ILD) as a function of position on the layout. Capacitance extraction (using FastCap) was performed on this 3D geometry, followed by Spice analysis to study clock skew in a balanced H-bar distribution network.

A new methodology has been developed to overcome time and computation limitations in the previous approach. In particular, the goal is to enable the study of hundreds or thousands of global paths to understand the impact of spatial variation. An IBM 1GHz microprocessor circuit design and layout was used as the case study. In our approach, a single circuit extraction is performed for each net of interest, and key geometric information kept for nodes in that net. This information, combined with spatial variation information, enables one to consider the incremental (linearized) change to capacitance due to variation. The modified net undergoes timing analysis (rather than Spice simulation) to extract delay information. In this way, a distribution of net delay variations can be generated.

Personnel

O. Nastov (J. White)

Sponsorship

Cadence Design Systems, Motorola Semiconductor,
Harris Semiconductor, MAFET Consortium

RF integrated circuit designers make extensive use of simulation tools which perform nonlinear periodic steady-state analysis and its extensions. However, the computational costs of these simulation tools have restricted users from examining the detailed behavior of complete RF subsystems. Recent algorithmic developments, based on matrix-implicit iterative methods, is rapidly changing this situation and providing new faster tools which can easily analyze circuits with hundreds of devices. We have investigated how these new methods by describing how they can be used to accelerate finite-difference, shooting-Newton, and harmonic-balance based algorithms for periodic steady-state analysis.

Software Tools for Process-Sensitive Reliability Assessments of IC Designs

Personnel

Y. Chery, S. Riege, W. Fayad, Y.-J. Park (D. Troxel and C.V. Thompson)

Sponsorship

DARPA, SRC

Integrated circuits are currently designed using simple and conservative 'design rules' to ensure that the resulting circuits will meet reliability goals. This simplicity and conservatism leads to reduced performance for a given circuit and metallization technology. There have been recent significant advances in the understanding of the dependence of integrated circuit interconnect reliability on interconnect geometries, circuit layout, and interconnect processing. In addition, it is now known that many interconnect elements are immune to electromigration-induced failure under the conditions of their actual use. Incorporation of these improved understandings of interconnect reliability into the circuit design and layout process will lead to more accurate reliability assessments and to less overly conservative designs, allowing the design and layout of higher-performance circuits.

We are developing a TCAD tool, ERNI, which will allow process-sensitive and lay-out specific reliability estimates for fully laid out or partially laid out integrated circuits. We have developed a set of filtering algorithms which allow identification of highly reliable or immortal interconnect elements based on increasingly more complex analyses. By using these algorithms in a hierarchical analysis, we expect that large circuit-level analyses will be made computationally tractable. The availability of a tool such as ERNI will allow assessment of the impact of materials, processes, circuit-design and circuit-layout modifications on circuit reliability. This will lead to the manufacture of higher performance circuits with more accurately assessed reliabilities.

Modeling of Grain Growth in Thin Films

Personnel

S. Seel, W. Fayad, S. Riege, H.J. Frost, G. Straub (C.V. Thompson)

Sponsorship

NSF, SRC

We have developed computer simulations for normal and abnormal grain growth during deposition and subsequent heat treatments of polycrystalline thin films. We have included the effects of grain boundary drag due to surface grooving and due to the presence of solutes. The former leads to stagnation of normal grain growth at a point where the grain sizes are lognormally distributed and the average grain diameter is about three times the film thickness. This simulation result closely matches experimental results in a wide variety of systems. To account for observations of texture evolution during abnormal grain growth in thin films, we have included the effects of surface, interface, and strain energy anisotropy in our simulations of grain growth in films. These simulations allow investigations of the effect of energetic anisotropies on the evolution of texture and grain orientation distributions, as well as on the evolution of the average grain size and the distribution of grain sizes. Predictive simulations of the evolution of the distribution of grain sizes and orientations can be made as a function of materials selection, film thickness, and processing conditions, in both continuous and patterned films.

In the past year we have modified our grain growth simulation tool to account for the effects of second phase precipitates and of rough interfaces for both continuous and patterned films. These features have been included to account for experimental observations of grain growth made during in situ heating of continuous and patterned films in a transmission electron microscope. In addition, we have studied the evolution of soap froths in 3D volumes in order to characterize grain structure evolution in volumes in which 2 or more dimensions are comparable to the average grain size. We are developing analytic models which describe such evolution, and comparing these models and results from froth studies with fully-3D simulations of grain growth carried out at Los Alamos National Laboratory. Analytic models for

continued

grain structures and grain structure evolution are being incorporated into tools for simulation of stress evolution and for analysis of the reliability of micrometer and nanometer-scale materials in device and circuit structures.

Personnel

Y. Chery (C. V. Thompson and D. E. Troxel)

Sponsorship

DARPA

Recent research has demonstrated interconnect failure due to electromigration effect to be strongly dependent not only on current density but also on metal film crystal grain size distribution and geometries of interconnect patterns. This type of failure is manifest as a depletion of interconnect metal forming a "void" (open-circuit) or an accumulation possibly forming a "short" to neighboring interconnect.

Our research work focuses on:

1. Developing abstract, physically-based, microstructural interconnect failure models to more accurately predict electromigration induced failure.
2. Electromigration Reliability for Network Interconnect (ERNI), our prototype computer-aided design tool based on these abstracted microstructurally based models.

A release of ERNI 2.0 is expected soon with extensions supporting hierarchical designs and utilizing higher performance circuit simulation engines. This release will incorporate client and server programs implemented in Java. With this, multiple designers at different locations will be able to cooperatively design integrated circuitry which incorporates electromigration reliability models.

Simulation of Electromigration-Induced Failure of IC Interconnects

Personnel

V. Andleigh, Y.-J. Park, C. Hau, S. Riege, W. Fayad (C.V. Thompson)

Sponsorship

SRC, DARPA

We have developed a software tool for structure-sensitive simulation of electromigration and electromigration-induced failure of interconnects. A web-based version of this tool, MIT/EmSim, can be accessed at nirvana.mit.edu/emsim/. The tool generates grain structures with known statistical variations as a function of median grain size and line width, and predicts failure statistics as a function of various failure criteria, and as a function of the current density and of the temperature. The effects of wide-to-narrow transitions, junctions, and thermal history have also been included, and are now being tested through comparisons with experiments. MIT/EmSim has been used to simulate electromigration-induced failure in pure Al and Al-Cu interconnects, and is currently being adapted for use in simulation of electromigration-induced failure in pure Cu and Cu alloy interconnects. MIT/EmSim allows the user to study failures based on void nucleation, void growth, and compressive failures. Future upgrades will incorporate the effects of precipitate nucleation and growth, redistribution of alloy additions, and post-patterning grain structure evolution.

In the conventional interconnect reliability assessment methodology, accelerated lifetime tests are carried out at elevated current densities and temperatures, and specific scaling behavior is assumed in predicting lifetimes at in-service current densities and temperatures. For example, it is assumed that lifetimes scale with the current density j to the power -2 for void-nucleation-limited failure, and j to the power -1 for void-growth-limited failure. Using simulations we have shown that there can be a transition in scaling behavior in going from test to service conditions, leading substantial scaling errors when this is not accounted for. Further, we have shown that short lines can display conventional scaling behavior at test conditions but be immune to failure at service conditions. These simulation results are consistent with a growing body of experimental results. This complex behavior must be accounted for in order to make accurate reliabil-

ity projections, and in order to take advantage of the greatly improved reliabilities of short lines. To catalog scaling behavior we have developed 'failure-mechanism maps' which show the scaling behavior as a function of current density and line length. Such maps can be used in reliability assessments and in developing optimum circuit layout strategies. MIT/EmSim can be used to generate these maps for different metallization materials and processes.

Electric Field Simulations for Field Emission Devices

Personnel

Y-J. Yang
(S. D. Senturia in collaboration with A. I. Akinwande)

Sponsorship

DARPA

The goal of this project is to develop a CAD tool for prediction of electron emission from field emitter tips, their trajectory to the phosphor screen and the resulting spot size on the screen for an array of field emitters. The basic structure studied is shown in Figure 8. It consists of a field emitter cone with a tip radius of 10 nm, a 0.2 μm thick gate with 1 μm aperture, a 0.5 μm thick focusing electrode located 0.5 μm above the gate. The anode is about 1 mm above the field emitter.

The project raises two key challenges: the very different dimensional scales surrounding the emitter tip (10 nm), the gate (1 μm) and the anode (1 mm) and the need to adapt boundary element based solvers for (Dirichlet and Neumann) mixed boundary conditions. The potential gradient is calculated on surfaces with Dirichlet conditions and potential on surfaces with Neuman conditions using a Green's Theorem kernel. A source formula is used to calculate an equivalent pseudo-charge distribution on all surfaces from which electric field is determined at any point of interest is determined.

Using this approach, electric field at the tip surface is determined and the field emission current density is calculated using the Fowler-Nordheim equation. The electron trajectories are obtained by integrating the Lorentz equation from various points on the emission tip to the anode. The spot size and current distribution on the phosphor screen for an array of field emitters can be calculated using superposition using the trajectories weighted by the emission surface areas and the current densities.

Figure 9 shows a typical Si FEA structure that was fabricated and characterized. Figure 10 shows a comparison of the experimental simulated current per tip as function of the gate voltage for a 60x60 Si tip FEA. The only adjustable parameter is the radius of curvature. The radius of curvature that matched the simulation is 8.4 nm while the experimentally measured radius is about 10 nm.

Figure 11 shows a comparison between the spot size measured for a phosphor screen which is biased at 5000 V and is 1 cm away from the FEA. The experimental spot size is about 2 mm while the simulated spot size is 1.8 mm.

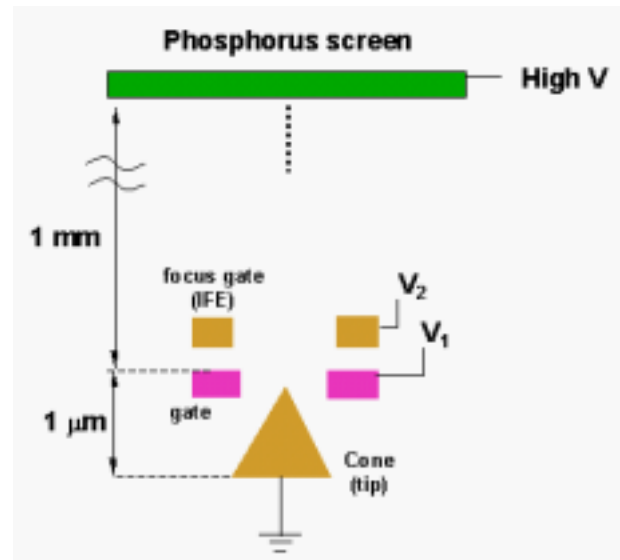


Fig. 8: The Integrated Focus Electrode Field Emitter Display structure.

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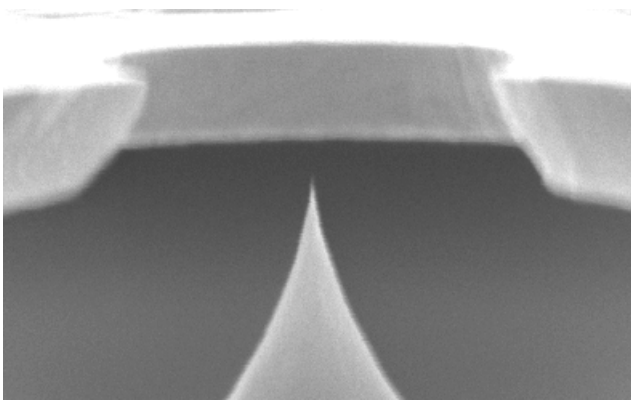


Fig. 9: SEM of the Si Field Emitter tip.

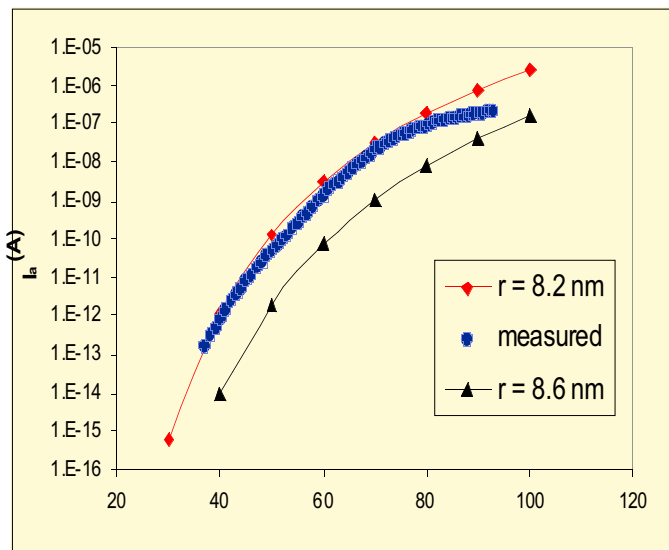
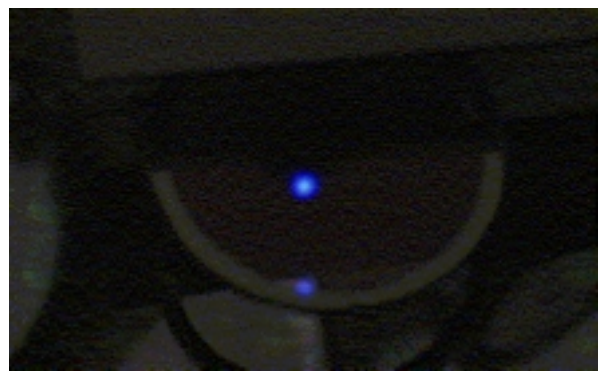
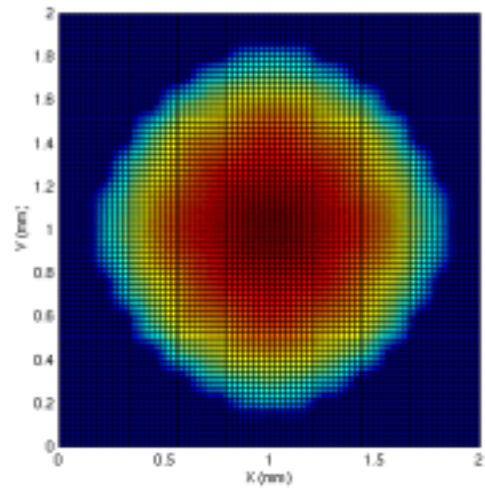


Fig. 10: Comparison between the experimental and simulated current density for a Si field emitter array. The only adjustable parameter was the tip radius.

Fig. 11: Experimental and simulated spot size on phosphor screen for a 60×60 $4 \mu\text{m}$ -pitch FEA with the phosphor screen biased at 5000 V at a distance of 1 cm from the FEA.

Simulation Tools for Micromachined Device Design

Personnel

X. Wang, W. Ye, Y. Massoud, D. Ramaswamy (J. White)

Sponsorship

DARPA, SRC

Micromachining technology has enabled the fabrication of several novel microsensors and microactuators. Because of the specialized processing involved, the cost of prototyping even simple microsensors, microvalves, and microactuators is enormous. In order to reduce the number of prototype failures, designers of these devices need to make frequent use of simulation tools. To efficiently predict the performance of micro-electro-mechanical systems these simulation tools need to account for the interaction between electrical, mechanical, and fluidic forces. Simulating this coupled problem is made more difficult by the fact that most MEMS devices are innately three-dimensional and geometrically complicated. It is possible to simulate efficiently these devices using domain-specific solvers, provided the coupling between domains can be handled effectively. In this work we have developed several new approaches and tools for efficient computer aided design and analysis of MEMS.

One of our recent efforts in this area has been in developing algorithms for coupled-domain mixed regime simulation. We developed a matrix-implicit multi-level Newton methods for coupled domain simulation which has much more robust convergence properties than just iterating between domain-specific analysis programs, but still allows one to treat the domain analysis programs as black boxes. In addition, we developed another approach to accelerating coupled-domain simulation by allowing physical simplifications where appropriate. We refer to this as mixed regime simulation. For example, self-consistent coupled electromechanical simulation of MEMS devices face a bottleneck in the finite element based nonlinear elastostatic solver. Replacing a stiff structural element by a rigid body approximation which has only 6 variables, all variables associated with the internal and surface nodes of the element are eliminated which are now a function of the rigid body parameters. Using our coupled domain approach has made it possible to perform coupled electromechanical analysis of an entire comb drive accelerometer in less than 15 minutes.

Analysis of the resonance behavior of micromachined devices packaged in air or fluid requires that fluid damping be considered. Since the spatial scales are small and resonance analyses are typically done assuming a small amplitude excitation, fluid velocities can often be analyzed by ignoring convective and inertial terms and then using the steady Stokes equation. For higher frequency applications, the convective term may still be small, but the inertial term rises linearly with frequency. Therefore, analyzing higher frequency resonances requires the unsteady Stokes equations, though the small amplitudes involved make it possible to use frequency domain techniques. We have developed a fast Stokes solver, FastStokes, based on the precorrected-FFT accelerated boundary-element techniques. The program can solve the steady Stokes equation or the frequency domain unsteady Stokes equation in extremely complicated geometries. For problems discretized using more than 50,000 unknowns, our accelerated solver is more than three orders of magnitude faster than direct methods.

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