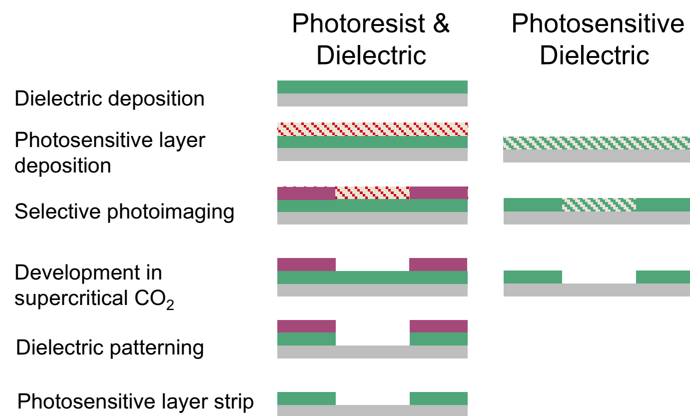
Materials



Solventless Lithography
Courtesy: Hilton G. Pryce Lewis (Karen K. Gleason)

Materials

- *Si/SiGe Nanostructures*
- *SiGe and Ge Photodetectors for Si Microphotonic Circuits*
- *Epitaxial Films for Micromechanical Devices*
- *III-V/GeSi/Si Heterointegration*
- *Silicon Microphotonic Data Link with Modulation and Gain Elements*
- *Novel Semiconductor LED and Laser Materials*
- *Co-Evolution of Stress and Structure in Polycrystalline Thin Films*
- *Structure Evolution in Electrodeposited Materials for Microfabrication*
- *Device Degradation*
- *Defect Engineering*
- *Oxygen Insertion into $LnMO_{4+\delta}$ Compounds*
- *Structure and Properties of Single Crystal Bismuth Nanowire Arrays*
- *Ferroelectrics for High Strain Actuation*
- *Ceria-Praseodymia Solid Solutions*
- *Cluster Ion Beam Processing*
- *Solventless Low Dielectric Constant Thin Films*
- *Solventless Lithography*
- *Process Analysis and Simulation for PV and IC Applications*

Si/SiGe Nanostructures

Personnel

M. Currie, T. Langdo, G. Taraschi, C. Leitz, and M. Lee (E. Fitzgerald)

Sponsorship

NSF/MRSEC, DARPA

We are developing two dimensional electron and hole gases in the Si/SiGe system. Such structures require the useof relaxed, defect-engineered SiGe on Si substrates. The epitaxial films can be pattered laterally to produce low-dimensional structures. We are exploring new novel methods of controlling the lateral size of Si and SiGe devices. We are investigating the physics of carrier transport in SiGe/Si heterostructures and we are also interested in mesoscopic device sizes which will be encountered as Si CMOS technology matures. We have started a collaborative program with EE to investigate low-temperature selective Si and SiGe growth in 100nm-sized windows. Successfully controlling this process will allow the fabrication of Si nanostructures and vertical nano-MOSFETs. In addition, we have recently demonstrated high quality Ge growth in nano-openings in SiO_2 masks on Si substrates.

SiGe and Ge Photodetectors for Si Microphotonic Circuits

Personnel

L. M. Giovane, H-C. Luan, D. Lim, K. Lee, A. M. Agarwal, K. Wada, J. Michel, and L. C. Kimerling

Sponsorship

SRC, AT&T and DOD Fellowships

We are studying SiGe heterostructures in collaboration with Professor E. A. Fitzgerald. We have grown $Si_{1-(x+0.25)}Ge_{x+0.25}$ / $Si_{1-(x-0.25)}Ge_{x-0.25}$ strained-balanced-superlattices on high quality $Si_{1-x}Ge_x$ relaxed buffers. Photodiodes were fabricated. The absorption spectra were modeled by deformation potential theory and confirmed with photocurrent spectroscopy. EBIC was used to determine the threading dislocation density of PIN junctions grown on SiGe relaxed buffer junction with different grading rates. Mesa isolated PN diodes were used to determine bulk leakage current densities. The bulk leakage current density scales directly with the threading dislocation density. Bulk leakage current density per dislocation length agrees with the value calculated from literature data on capture cross-section and defect density per dislocations in Si and SiGe materials.

We are also studying the UHV-CVD growth of high quality Ge on Si for the integration of Ge photodetectors with polysilicon waveguides and Si CMOS devices. Ge provides high absorption coefficient at 1.54 μm and is an ideal material for photodetection at optical communication wavelength. High quality Ge with low threading dislocation density can be grown directly on Si by a two-step growth technique followed by an annealing treatment.

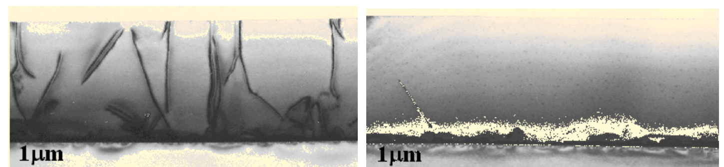


Fig. 1: (Left) Cross sectional TEM micrograph of 1μm of Ge grown on Si by UHV-CVD. (Right) Cross sectional TEM micrograph of 1 μm of Ge on Si after annealing.

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The electrical properties and optical properties of Ge films grown on Si are being characterized. Based on our measurements, the effect of threading dislocations on the GHz operation of Ge photodetectors will be studied.

We are designing a process for the integration of Ge photodetectors with polysilicon waveguides and Si CMOS devices. This process technology makes use of our ability to grow Ge selectively on patterned Si wafers. SiO_2 is used to protect Ge materials from traditional Si CMOS process chemistries such as the RCA and Piranha cleans. The goal of this project is the demonstration of a functional Si microphotonics circuit.

Fig. 2: Cross sectional TEM micrograph of 1mm of Ge selectively grown on Si.

Epitaxial Films for Micromechanical Devices

Personnel

M. Currie and Nicole Gerrish (E. Fitzgerald)

Sponsorship

Draper Laboratories

Miniature, high-quality microphones, accelerometers, gyroscopes and other sensors can be fabricated from thin, unsupported semiconductor films. These films are fabricated by using selective etches. Currently, B diffusion is used to create a highly doped region. Unsupported films are created by using the selective etch to remove the substrate. Our research has shown that the diffusion process leads to a metastable balance between strain relief by dislocations and mismatched strain created by high boron concentrations. Epitaxial layers in the GeSiB system appear to be promising films for defect-free micromachined structures. We have recently discovered that the relaxed SiGe alloys have unique etching properties that can be exploited in the fabrication of micromachined structures. We are currently optimizing the relaxed SiGe materials for micromachined structures and studying the etch-stop mechanism.

III-V/GeSi/Si Heterointegration

Personnel

S. Ting, M. Groenert, M. Currie, T. Langdo, V. Yang, and L. McGill (E. Fitzgerald)

Sponsorship

NSF/MRSEC, ARO

Recent advances in heteroepitaxy have allowed the fabrication of lattice-mismatched, relaxed GeSi layers on Si with very few dislocations penetrating the upper layers. This larger GeSi lattice can be subsequently used for the lattice-matched growth of III-V materials like InGaP and GaAs. The ultimate goal is the co-habitation of III-V optical devices and Si integrated circuitry, allowing functionality and cost improvements in data storage, high quality printing, and high speed processing systems. The materials challenges are decreasing the residual dislocation density even further, improving the III-V/VI interface, and establishing process integration. Recent research results have revealed the critical nature of the materials processing at the GaAs/Ge interface. Without performing epitaxial growth within certain process windows the GaAs grown on this near-lattice matched substrate can possess a dislocation density as high as $10^9 cm^{-2}$, whereas the optimized process results in GaAs with a defect density as low as 10^4-$10^5 cm^{-2}$. Using these optimized interfaces, we have been able to integrate GaAs on Si with unprecedented perfection. Such films can now be used for prototyping GaAs devices integrated on Si substrates.

Silicon Microphotonic Data Link with Modulation and Gain Elements

Personnel

A. Agarwal, S. Ahn, T. Chen, X. Duan, K. Lee, D. Lim, H.-C. Luan, J. Michel and E. Ouellette (L. C. Kimerling)

Sponsorship

DARPA, Rome Laboratory (Hanscom AFB), and SRC

Silicon microphotonics is a basic building block for optical sensing circuits, optical networking for telecommunications, and IC level optical interconnection. This program examines the performance and process optimization of integrated emitters and waveguide components, and studies the key materials integration issues for SOI, SiGe and Ge based structures. While these materials are excellent performers, polycrystalline silicon provides necessary flexibility in processing and photonic circuit architecture. We have demonstrated small radius bends and high angle splitters in poly-Si strip waveguides with 0.2x0.5 µm cross sections. Bend radii between 1 and 100 µm have been tested with losses less than 5 dB. Y-branch, 3dB power splitters with splitting angles of 20º and 30º have been fabricated and are currently being tested. The real estate required for integrated devices using these waveguide components is greatly reduced compared to more typical III-V or SiO_2 waveguide systems.

A different splitting scheme called a MMI (Multi Mode Interferometer) is fabricated in poly-Si, and is expected to exhibit lower splitting loss than simple Y-branch type splitters. MMIs significantly reduce the real estate used for splitting optical signals into multiple outputs due to their design and loss advantages. The first 1x16 fanout was demonstrated in a poly-Si waveguide system. High dielectric contrast of poly-Si/SiO_2 and design optimization led to the smallest 1x16 power distribution system ever built, where an area as small as $1x10^{-4} cm^{-2}$ was used for such distribution.

We envision using a 1x16 power distribution system to build the first optical clock on-chip. The area advantage of our system relaxes area constraints on the limited on-chip real estate. The performance of the power distribution system was evaluated by developing a model, which related the power output uniformity to optical clock skew. Based on the measured power uniformity of our 1x16 power splitters, we have calculated the clock skew

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in an optical clock distribution system. The calculations in our model show that the optical clock skew is not determined by variations in the optics, but by the receiver electronics. The clock skew should be well below the critical skew level for operations at several GHz, given sufficient performance of the receiver electronics.

We have designed light modulators based on both free carrier absorption and free carrier refraction. One example is a modulator based on parallel silicon dielectric waveguide mode coupling. The index of refraction of one guide is controlled by free carrier injection and results in a change in the total power coupled from one waveguide to the other. This modulator is capable of 30 MHz bandwidth with 20 dB contrast at 0.5W power desorption with a 600 mm coupling length.

Novel Semiconductor LED and Laser Materials

Personnel

A. Kim and S. Ting (E. Fitzgerald)

Sponsorship

NSF/MRSEC, ARO

AlGaAs/GaAs and InGaAsP/InP laser materials have been developed due to the lattice-matching potential of the materials. However, there are an increasing number of applications needing wavelengths and power levels that can not be produced by these materials. Removal of the lattice-matching requirement allows one to design lasers that will emit at a variety of new wavelengths when fabricated on conventional substrates like GaAs and Si. In particular, visible light emitters in the InGaP system and 1.3 µm emitters in the InGaAs are being explored. The effect of engineered defect structure on the reliability of these devices will be a key issue in defining the utility of these lasers.

We have developed an understanding of work hardening in graded InGaAs/GaAs and InGaP/GaP relaxed layers grown by OMCVD. We have discovered that the formation of planar defects in the ternary compounds can lead to high dislocation densities in the relaxed InGaAs/GaAs and InGaP/GaP. We have developed a model that explains this dislocation increase, and through application of this model, we have been able to produce relaxed $In_{30}Ga_{70}As$ on GaAs and relaxed $In_{30}Ga_{70}P$ on GaP with low threading dislocation densities.

Co-Evolution of Stress and Structure in Polycrystalline Thin Films

Personnel

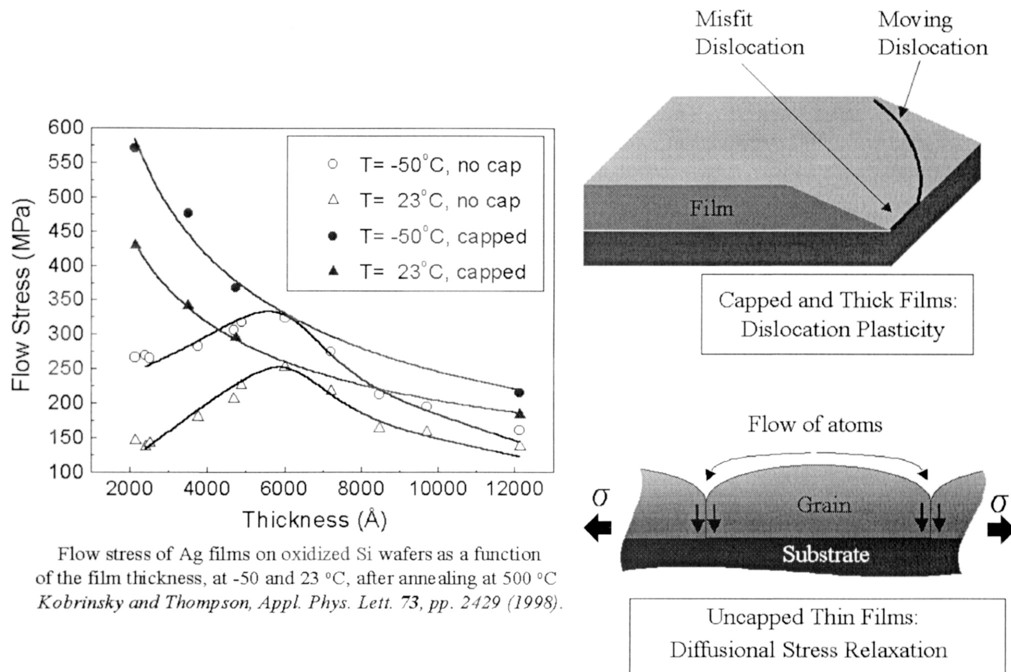
M. Kobrinsky, S. Seel (C.V. Thompson)

Sponsorship

NSF

It is known that the evolution of grain sizes and orientations in polycrystalline films can be driven in part by the strain energy resulting from deformation. However, to accurately calculate the strain energy, a better understanding of the film thickness, grain size, and orientational dependencies of deformation mechanisms in thin films must be developed. We are carrying out experiments to characterize stress and structure evolution during film formation and during post-deposition annealing. These experiments are used as the basis for development of modeling and simulation capabilities for engineering optimization of film stresses and structures.

In the past year we have shown that the flow stress in uncapped Ag films can increase or decrease with decreasing film thickness (see Figure 4). An increasing flow stress with decreasing film thickness is well known and is thought to be the result of geometrical constraints on dislocation motion. We have demonstrated that decreasing flow stresses with decreasing film thicknesses indicate the effects of diffusive stress relaxation processes. Analytic kinetic models for these processes are under development. Both diffusive and dislocation-mediated plasticity are strongly affected by the gain structures of polycrystalline films. We are carrying out experimental studies of stress and structure evolution in films on wafers, in films on MEMS devices, and in films on micromachined membranes. The latter allows in situ transmission electron microscope observations of dislocation motion.



Flow stress of Ag films on oxidized Si wafers as a function of the film thickness, at -50 and 23 °C, after annealing at 500 °C *Kobrinsky and Thompson, Appl. Phys. Lett. 73, pp. 2429 (1998).*

Fig. 4.

Diffusional

Structure Evolution in Electrodeposited Materials for Microfabrication

Personnel

R. Krishnan, S. Riege and M. Gross
(C.V. Thompson)

Sponsorship

Singapore-MIT Alliance

Electrodeposition is used to fabricate integrated circuit interconnects, is used in the manufacture of thin film magnetic heads, and is used in fabrication of a variety of microelectromechanical devices. While much is known about the evolution and control of grain structures during vapor deposition of polycrystalline micro and nano-structures, less is known about the control of grain structure evolution during electrodeposition of very small structures. Electrodeposition is in many ways a very controllable process in that there are chemical, electrical hydrodynamic control parameters available for process modification. However, impurity incorporation is more of a concern than is generally the case in vapor-deposition, and impurities can affect post deposition structure evolution as well as the performance and reliability of electrodeposited films in microdevices.

We have initiated basic studies of processing-structure-property relationships in electrodeposited films and micro-structures. Our goal is develop process models and methodologies that will allow optimization of the structures and properties of electrodeposited polycrystalline films for specific device and circuit applications.

Device Degradation

Personnel

M. Groenert (E. A. Fitzgerald)

Sponsorship

NSF/MRSEC

Current electronic and optical devices are successful in the marketplace if performance, cost, and reliability are optimized. Achieving higher device reliability hinges on knowing the microstructural detail of the failure mechanisms. Techniques like transmission electron microscopy, electron beam induced current, chemical etching, electrical measurements, and statistical analysis can be used to determine the most important failure modes of device structures. In particular, the reliability of experimental laser structures that can possess a larger number of intrinsic defects is being explored, and methods for extending device lifetime are being developed.

Defect Engineering

Personnel

A. Kim, T. Langdo, M. Currie, V. Yang, G. Taraschi, L. McGill and C. Leitz (G. Fitzgerald)

Sponsorship

NSF/MRSEC, DARPA

Completely relaxed mismatched epitaxial layers with relatively low threading defect densities can be achieved using graded-composition GeSi layers grown at high temperatures. Alternatively, completely strained and very metastable GeSi layers can be produced by limiting the number of dislocations which can readily nucleate. Yet, a complete understanding of dislocation nucleation and interaction in these structures is still absent. The details of nucleation of dislocations, how they interact, and new methods of decreasing threading dislocation densities in relaxed materials are being explored. Improvements in tailoring both strained and relaxed layers will be used in novel GeSi/Si structures which can absorb 1.3 µm light in relatively short lengths of material (1-5 µm). In the III-V materials systems, relaxed InGaP, InGaAs and GaAsP layers on GaAs are being engineered to have few defects, resulting in short wavelength and infrared LEDs and lasers on GaAs and GaP. Our research has led to an increased understanding of work hardening in graded epitaxial layers.

Recently, we have capitalized on our increased understanding of the interaction between the epitaxial surface and the buried misfit dislocation structure. By inserting a planarization step within the relaxed SiGe graded layer, we have been able to drastically decease the number of dislocation pile-ups that form in the material. The result is that we can produce strain-free Ge at room temperature with low threading dislocation densities ($\sim$1-2x10^6 cm^{-2}). Due to the high-quality of the Ge, we were able to fabricate Ge photodiodes integrated on Si with near ideal characteristics and reverse leakage currents 2 orders of magnitude less than other reported Ge on Si photodiodes.

Oxygen Insertion into $LnMO_{4+\delta}$ Compounds

Personnel

H. Fritze (H.L. Tuller)

Sponsorship

NSF/MRSEC and Alexander von Humboldt Foundation

We are studying the electrochemical insertion of oxygen into pulsed laser deposited films of $LnMO_{4+\delta}$ (Ln = La, Pr, Nd; M = Ni, Cu) with the aid of a quartz microbalance (QCM). This allows, in principle, for greater flexibility in control of properties and room temperature processing. Cyclic voltammograms showed oxidation and reduction peaks typical for these oxides. The change in oxygen stoichiometry was determined by *in-situ* QCM measurements during potential step experiments. The resulting maximum mass change, on the order of 50 ng, corresponded to an excess oxygen content of $\delta = 0.12$ in $Nd_2NiO_{4+\delta}$. The time dependence of the mass change was described by a transport model which yielded room temperature oxygen diffusion coefficients in the range from $2 \cdot 10^{-12}$ to 10^{-11} cm^2/s depending on δ and the redox direction. Studies are now being directed on the role of morphology on kinetics.

Structure and Properties of Single Crystal Bismuth Nanowire Arrays

Personnel

Z. Zhang, X. Sun, G. Dresselhaus, M.S. Dresselhaus, J.Y. Ying, G. Chen, J. Heremans, C.M. Thrush and D.T. Morelli

Sponsorship

US Navy, ONR MURI

We have succeeded in fabricating arrays of parallel bismuth nanowires, which are single crystals with the same crystallographic structure as bulk bismuth and the same lattice constants. The bismuth nanowires are embedded in an alumina matrix and can have diameters ranging from 10—110 nm and lengths up to 150μm. Because of the very small effective mass components in bismuth, quantum confinement effects can be observed in nanowires in this size range. We have an interest in utilizing the large anisotropy in the Fermi surface and other desirable properties of bismuth for thermoelectric applications.

However bismuth in bulk form is a semimetal and therefore is not a good thermoelectric material because of the approximate cancellation between the electron and hole contributions to the Seebeck coefficient. However, quantum confinement can be introduced by making bismuth in the form of small diameter nanowires, thus moving the lowest conduction subband edge up and the highest valence subband edge down to get a one-dimensional (1D) semiconductor at some critical wire cross sectional width a_c. A theoretical model based on the basic electronic band structure of bulk Bi has been developed to predict the dependence of the transport properties of bismuth on nanowire width. By carefully tailoring the Bi wire width a and carrier concentration, substantial enhancement in the thermoelectric figure of merit is expected for small nanowire widths. Bismuth nanowires of cross-sectional width less than about 10 nm are predicted to have a thermoelectric figure of merit $Z_{1D}^{x}T$ of about 1.

A detailed experimental study has also been made of the electrical transport properties of single crystal bismuth nanowire arrays embedded in a dielectric matrix. Measurements of the resistance of Bi nanowire arrays with different wire diameters (28 -110 nm) have been carried out over a wide range of temperatures (1.4 - 300K) and magnetic fields (0 - 5.4T). The transport properties of a heavily Te-doped Bi nanowire array have also been studied. At low temperatures, we show through measurements of the magnetoresistance that the wire boundary scattering is the dominant scattering process for carriers in the undoped single crystal Bi nanowires, while boundary scattering is less important for a heavily Te-doped sample. The temperature dependences of the zero-field resistivity and of the longitudinal magneto-coefficient of the Bi nanowires were also studied and were found to be strongly dependent on the wire width. The quantum confinement of carriers plays a central role in determining the overall temperature dependence of the zero-field resistivity. A theoretical model based on the basic electronic band structure of bulk Bi has been developed to interpret these measurements in the context of the transition of bismuth from a semimetal to a semiconductor as the wire diameter is decreased.

Ferroelectrics for High Strain Actuation

Personnel

Y. Avrahami, H.L. Tuller in collaboration with
Y.-M. Chiang, M. Cima, and N. Hagood

Sponsorship

ARO

Lead perovskite systems are being explored as potential candidates for high strain actuators with large thermal stability and low hysteresis. Field-induced antiferroelectric-ferroelectric transitions show high strain levels in polycrystalline materials. Compositions have been identified which show a morphotropic phase boundary and consequently temperature insenstive strain-field characteristics. Efforts are presently focused on the growth of single crystal high strain relaxor ferroelectrics.

Ceria-Praseodymia Solid Solutions

Personnel

P. Knauth (H.L. Tuller in collaboration with
E. Logothetis, Ford)

Sponsorship

NSF

The Ceria-Praseodymia Solid Solutions show extensive deviations from stoichiometry, intermediate ordered structures, and a variety of transport mechanisms which render them of interest as the active component of gas sensors. These are being systematically investigated by a variety of methods including impedance spectroscopy, coulometric titration and X-ray diffraction.

Cluster Ion Beam Processing

Personnel

A. Agarwal, H-C. Luan, K. Wada (L. C. Kimerling)

Sponsorship

Collaboration with Professor Isao Yamada, Kyoto University

As ULSI technology in silicon moves to permit a billion transistors on a chip, the SIA (Semiconductor Industry Association) defines the need to address four crucial materials-related issues: interconnect materials, thin gate oxides, accurate materials-based mesoscopic modeling and ultra-shallow junction formation. This project addresses two of the challenges, ultra-shallow (<40μm) junction formation and modeling non-equilibrium mesoscopic fabrication processes. The specific objective is the understanding of the pathways of defect reactions during the fabrication of ultra-shallow junctions, formed by an emerging technique called **cluster ion implantation**, and application of this knowledge to process simulation.

The novel technique of cluster ion implantation enables the formation of ultra-shallow junctions in silicon (<40?m) due to a high energy and hence controllable cluster ion beam that maintains a low energy per atom, given the large number of atoms in each cluster. Alternative methods for shallow junction formation, namely, solid-state diffusion through metal-silicides and low energy ion implantation, although very successful, have not shown great promise in realizing junctions shallower than 100μm. Furthermore, devices fabricated using cluster implantation have shown better electrical characteristics than current state-of-the-art technology.

The goal of this defect mechanisms project is to identify the defects created during a cluster implant, to understand their interactions with one another and with dopants, and to mesoscopically model their behavior. The first phase of the project proposes to discover the mechanisms of defect reaction kinetics from the dose, energy and heat treatment dependence of defect formation using standard materials and process characterization tools. The second and final phase of the project will develop materials-based mesoscopic models for the defect reaction kinetics. This new knowledge base that we create will be used to define an enhanced process window. For example, relevant to cluster ion implantation, we can develop new materials using non-equilibrium processing at low temperatures. In this research, we focus on the $B_{10}H_{14}$ cluster ion implantation because it has been demonstrated to form reliable p-type junctions shallower than 40nm, and can easily be integrated into process research.

Solventless Low Dielectric Constant Thin Films

Personnel

Kenneth K. S. Lau (Karen K. Gleason)

Sponsorship

NSF/SRC Engineering Research Center for Environmentally Benign Semiconductor Manufacturing

The semiconductor industry faces a formidable challenge in its future materials technology as ultra large scale integration (ULSI) dimensions are reduced below 0.25 microns. Line transmission RC delay becomes an increasingly significant bottleneck to circuit performance and speed. There is presently a great effort to replace the current dielectric material, silicon dioxide, with a dielectric material having a lower dielectric constant (κ). This reduces not only RC time constant but also cross talk and power dissipation. Furthermore, by considering environmental, safety and health (ESH) impact in developing these new materials and processes at the research level advantages a more manufacturable and sustainable system. Because ESH impact scales with the number of interconnect layers applied, a lower κ material already provides an intrinsic ESH benefit since fewer layers are required as a result of an increase in the possible areal packing density.

Potential low κ dielectric materials are produced either by spin on or chemical vapor deposition (CVD) processes. Spin on application, which is also used for photoresist, requires solvents for dispensing the low κ material and for subsequent cup rinsing. This raises potential concerns about liquid waste disposal and worker exposure to volatile organic compounds (VOCs). On the other hand, CVD is an enclosed vacuum process that avoids solvent usage, minimizes worker exposure to chemicals, and is also compatible with the move towards dry processing and cluster tool development. Of the CVD dielectric candidates, fluorocarbon (CF_x) films have the lowest κ, 1.9-2.4, depending on composition and structure. Perfluoronated compounds (PFCs) have been used to deposit CF_x films and may be present in the reactor effluent during deposition or post-chamber clean.

Our laboratory has successfully utilized pulsed plasma enhanced CVD and pyrolytic CVD to control the final molecular architecture of CF_x films. Figure 5 shows derivative films ranging from amorphous crosslinked networks to linear perfluoroalkyl chains much like

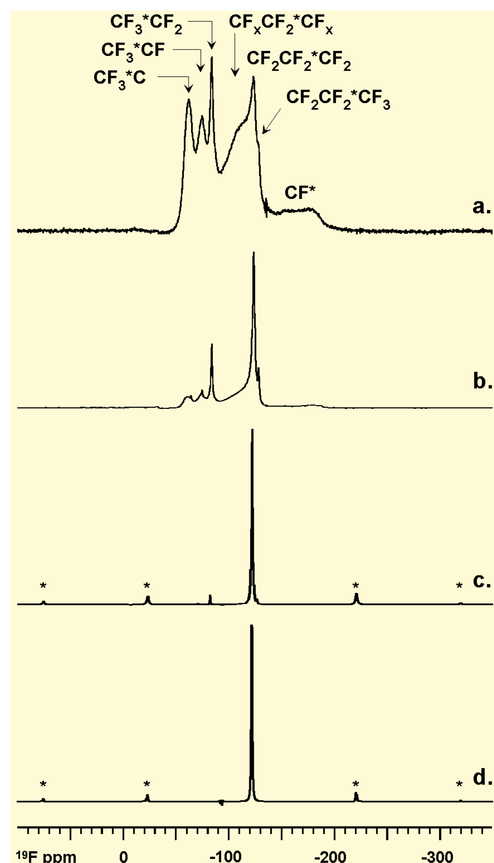


Fig. 5: ^{19}F 25 kHz MAS NMR spectra of fluorocarbon films from (a) 10/50 ms on/off time pulsed PECVD HFPO plasma, (b) 10/400 ms on/off time pulsed PECVD HFPO plasma, (c) pyrolytic CVD HFPO, and (d) bulk PTFE. Asterisk denotes spinning sideband.

poly(tetrafluoroethylene) (PTFE) can be produced, having κ values as low as 1.9 and loss tangents < 0.01. Film characterization by solid-state nuclear magnetic resonance (NMR) spectroscopy allowed film structure to be related to processing conditions and thermal annealing. Thermal decomposition has been found to shift from a loss in terminal CF_3 groups in more crosslinked matrices to desorption of low molecular weight PTFE oligomers as the amount of linear CF_2 structures increased. Films with essentially linear PTFE chains were shown to be thermally stable even after an in-situ 1 h 400ºC vacuum anneal. Gas phase FTIR measurements of reactor effluent during deposition provided a quantitative assessment of process ESH impact. Pulsed PECVD gave lower MMTCE (million metric tons of carbon equivalent) contributions to global warming compared to similar continuous PECVD processes while pyrolytic CVD produced no known global warming gases.

The versatility of pulsed PECVD and pyrolytic CVD stems from (i) varying the modulation frequency of plasma discharge in pulsed PECVD, (ii) varying precursor gas chemistries in pulsed PECVD, and (iii) shifting mechanistically from electrical activation in pulsed PECVD to thermal activation in pyrolytic CVD. The ability to control CF_x film architecture enables the correct structure-property-processing relationships to be developed so that a suitable low κ material which satisfies the diverse requirements of an interconnect dielectric can be achieved.

Solventless Lithography

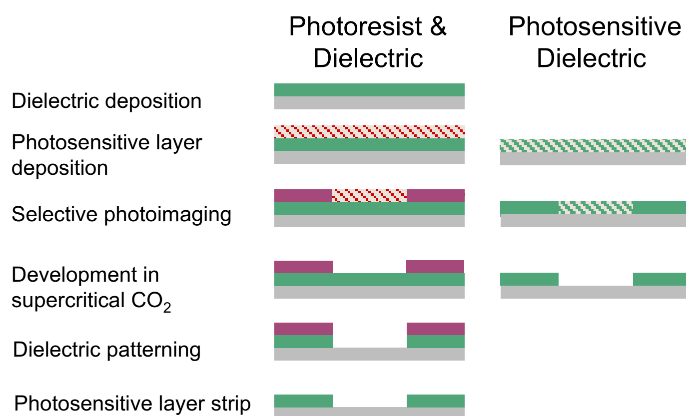
Personnel

H. G. Pryce Lewis (K. K. Gleason)

Sponsorship

NSF/SRC Engineering Research Center for Environmentally Benign Semiconductor Manufacturing

Conventional photoresists are applied by solvent-based spin-on technology. Typically, only a few percent of the material that is dispensed onto the wafer actually becomes the photoresist layer. Thus, spin-on resists result in large volumes of waste material which require safe and costly disposal. Thin films grown by Chemical Vapor Deposition (CVD) are proposed as alternative photoresist materials. The ESH impact of CVD processes can be minimized through design of the deposition chemistry. In addition, the use of a dry resist holds the promise of performance improvement, as precursor gases can be purified to a higher degree than conventional photoresist solutions.



As feature sizes have decreased, properties of the solvent used as developer have become increasingly important. Aqueous liquid developers lack high selectivity and tunable solvating power for advanced applications, and generate large amounts of environmentally harmful waste. Supercritical fluids possess characteristics beneficial for development of small, high-aspect ratio features: good selectivity, high diffusivities and viscosities, low surface tension, and solvating capabilities tunable through pressure and temperature control. Supercritical CO_2 is of particular interest as an environmentally benign developing medium, as it is nontoxic, nonflammable, cost-efficient and recyclable.

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continued

Proposed processes for solventless lithography

Two possible lithography processes are under investigation. The first is an "all-dry" scheme in which a photoresist is deposited using CVD, selectively exposed, and then developed in supercritical CO_2. This would eliminate wet chemistry used in existing photolithography processes. The second is a direct dielectric patterning process in which a photosensitive dielectric film is deposited, exposed and developed. Dry patterning of a low-k dielectric in such a scheme would greatly simplify future photolithographic processing.

Two CVD methods will be implemented for controlling the reaction pathways for deposition of dry resists: pulsed plasma-enhanced CVD (PECVD) and pyrolytic CVD. With these two CVD methods, the as-deposited films are anticipated to have fewer crosslinking sites than their continuous PECVD counterparts. Thus, irradiation resulting in the production of cross-linking groups or scission of polymeric chains can result in dramatic differences in chemical structure. Increasing structural differences between the as-deposited and irradiated films should correlate to higher photolithographic contrast. In addition, growth rates for the pyrolytic processes are very high. These excitation techniques allow tailoring of the film framework and incorporation of photosensitive and chemical amplification moieties. In this way, the concepts being developed for conventional photoresists can be incorporated into dry lithographic processes.

Fluoropolymers and organosilicons are being considered as dry resist materials. Their solubility in supercritical CO_2, low dielectric constants, and photosensitivity at short optical wavelengths make them attractive choices for use in dry lithographic processing. In particular, the aliphatic fluoropolymers are particularly exciting for 157 nm lithography, because many other materials are too absorbing at this wavelength. CVD fluoropolymer films are also under active investigation as low dielectric constant materials for advanced interconnects. PECVD-deposited organosilicon films have previously been investigated as potential photoresists and found to be optically transparent at 193 nm. Both fluorocarbon and organosilicon thin films can be deposited by pulsed PECVD and pyrolytic CVD.

To implement and optimize the necessary processing parameters for supercritical CO_2 development, research will be conducted to determine compatible photoresists which will satisfy existing feature size requirements, CO_2 solubility requirements, and 157 nm sensitivity and transparency requirements. Through sequential variation of film composition, solubility will be controlled and optimized for development. Examination of photoacid generating species for chemical amplification and film sensitivity control may be conducted as necessary.

A variety of pulsed plasma and pyrolytic CVD polymer films have been deposited and tested for solubility in supercritical CO_2. Optimum conditions for dissolution of the potential resist before exposure was determined by evaluating dissolution characteristics of the film at different pressures, temperatures, flow rates of CO_2 and times of development. Pyrolytic CVD organosilicon films and pulsed PECVD organosilicon films have shown promising results in initial testing. In addition, a model fluorocarbon film of composition $C_{20}F_{42}$ has demonstrated 100% solubility at moderate supercritical CO_2 conditions.

Process Analysis and Simulation for PV and IC Applications

Personnel

S. Ahn, A. Kelley, A. Smith, E. Wu, (L. C. Kimerling In collaboration with Siemans Solar (Camarillo, Ca.))

Sponsorship

NREL, Wafer Engineering & Defect Science Consortium

Our research effort continues to focus on the structure, stability, and kinetics of lifetime degrading defects in Si for the optimization of solar cells and integrated circuits. We are using experimentation and computational tools to generate fundamental models of gettering and point defect evolution. A program to model Fe gettering during processing for IC wafers or for Al back surface contact formation in solar cell manufacturing incorporates our understanding of dopant enhanced solubility, internal gettering, and our results from Al gettering experiments. A second program models defect reaction kinetics. An extensive set of defect reaction equations describes the role of defect, dopant concentrations and processing conditions. The process models provide a means of optimization of materials specifications and processes to achieve a desired minority carrier diffusion length.

We have constructed an Fe gettering model that quantifies the design and effectiveness of gettering treatments. The model includes the competing gettering mechanisms of internal gettering (IG), segregation to molten Al or epilayer substrates, and dopant enhanced solubility. The contamination, processing time-temperature profile of the gettering step, the material specifications, and the device structure are the relevant parameters. The resulting contamination profile of the wafer is the output that determines the minority carrier diffusion length. We have produced experimental results to verify the model. Gettering experiments by Al back surface contact formation were performed at various annealing temperatures using a quench to study the instantaneous contamination levels. The data, analyzed according to the model, gives values of precipitate density and size that are consistent with the Cz silicon used. Fe a lifetime limiting contaminant and understanding its removal is of primary importance. The principles of the model are generally applicable to other transition metal contaminants.

The point defect reaction model allows for the analysis of the interaction of point defects to determine material specifications required for a desired minority carrier lifetime. The interactions among self-interstitials (Si_i), vacancies (V), impurities (C,O), and dopants (B,P) in silicon not only lead to the formation of undesirable point defect products which affect device operation, but they also generate defect associates that control processes such as diffusion of dopants. Within the framework of reaction kinetics, for the first time, we have successfully modeled the defect reaction process.

This modeling program can be used to construct the interstitial defect reaction hierarchy diagram, to predict defect behavior in device processing and to characterize background dopant and impurity concentrations (e.g., [B], [P], [O], and [C]) in Si by combined electron irradiation and DLTS measurement techniques. With our point defect experimental data from 1MeV electron irradiation, the program has been applied to the case of a reactive ion etch (RIE), a process which induces point defect reactions, and the predicted defect depth profiles are consistent with those measured in the photoluminescence (PL) experiments.

In addition to Fe, Molybdenum is another transition metal of interest. Mo can easily contaminate Si wafers from the CVD susceptor made out of Mo, and Mo is incorporated together with BF_2 during BF_2 implantation due to the same mass to charge ratio. Mo can severely degrade the minority carrier lifetime in PV devices and bipolar transistors with its concentration beyond $10^{12}cm^{-3}$ in silicon. However, its structure in silicon is poorly understood, and its solubility and diffusivity in silicon are unknown. It is known that soluble Mo is electrically active with a defect state at 0.3eV above the valence band of Si. In collaborative experiments with Lucent, Bell Laboratories, Mo was implanted just below the surface of silicon and MeV Si was implanted to create two separate regions: vacancy-rich and interstitial-rich regions.

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Subsequently, Si:Mo samples were annealed and we profiled electrically active Mo using deep level transient spectroscopy and compared the Mo profile with that in the sample without MeV silicon implantation. We observed that more Mo diffused into samples that received MeV Si implantation. The Mo became electrically active at the vacancy-rich region than in samples without MeV Si implantation. We have deduced that substitutional Mo is stable and electrically active. Further verification of the Mo structure is under way with EPR (electron paramagnetic resonance), and Mo diffusivity is being determined.

The IC industry standard wafer is becoming an epitaxial layer on heavily doped substrates. The distribution of native point defects such as vacancy and self interstitials are expected to change for this structure. Since the interaction of Au diffusion with point defects is well understood, we use Au to study the native defects in epitaxial wafers. Samples have been heat-treated at 700C and 1000C for different durations and Au profiles are being obtained with spreading resistance profiles, deep level transient spectroscopy, and neutron activation method. The data at 1000C suggests that self-interstitial sinks are present at the interface to accumulate Au.

Experiments are underway to increase our quantitative knowledge of point defect and transition metal kinetics and their interactions for the development of a comprehensive model for predictive process simulation.