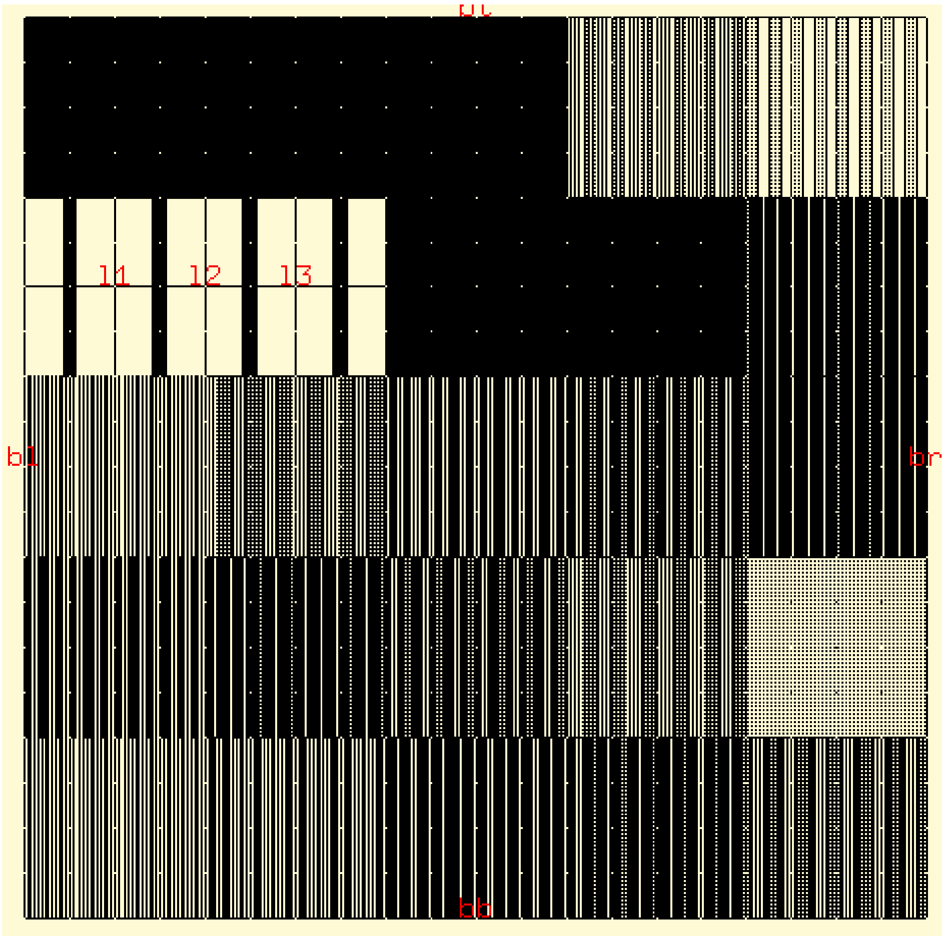
Manufacturing



Dielectric CMP Characterization Mask
Courstesy: D. Ouma, B. Lee and T. Park (D. S. Boning, J. Chung)

Manufacturing

- *Process Control System Architecture*
- *Novel Methods for Run by Run Process Control*
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Process Control System Architecture

Personnel

Aaron E. Gower and M. B. McIlrath (D. S. Boning)

Sponsorship

NIST ATP with On-Line Technologies

We have developed a distributed control system architecture and implemented a software/hardware prototype for the run-by-run control of semiconductor processes. The modular controller architecture includes sensor communication and analysis; controller communication and execution; equipment communication and recipe download; and user interface. Currently, we are working on the application of this architecture to epitaxial silicon fabrication. The goal of this work, undertaken in conjunction with On-Line Technologies and Applied Materials, is to develop cell controller software which will obtain data from in-line resistivity and thickness sensors, analyze the data to determine drifts in the epitaxial film process, and modify and download new process recipes to the fabrication tool.

Novel Methods for Run by Run Process Control

Personnel

T. Smith, A. Gower, and E. Stuckey (D. S. Boning)

Sponsorship

NSF, SRC, and NIST Advanced Technology Program

Novel methods are being explored for the run by run control of semiconductor fabrication processes. In such approaches, periodic recipe modifications from one run to the next are made in order to maintain specified quality, throughput, environmental, and other objectives. This research has included implementation of an Exponentially Weighted Moving Average (EWMA) controller, a Predictor-Corrector Controller (PCC), and Artificial Neural Network (ANN) controllers with application to different unit processes including plasma etch, sputter deposition, silicon epitaxy, and chemical-mechanical polishing. These control methods have been explored with respect to their stability, responsiveness (optimal or otherwise), ability to incorporate practical issues and their applicability to spatial uniformity and other multiple objective control goals.

Key contributions to run by run control methods have been made in three areas. First, extensions to the run by run controller have been made to address practical issues in dealing with time-dependent data in a manufacturing environment. In particular, data that is non-periodic (that is, appears at a random time interval), has missing or intermittent values, and which suffers recurring events (e.g. kit changes) are problematic for many control approaches. These have been addressed in an extension of the EWMA and predictor-corrector controllers (PCC), and demonstrated for the control of metal sputter deposition.

The second key contribution is the development of a framework for benchmarking of run by run control algorithms and implementations. A network-based interface has been developed that consists of (a) a number of process “simulators” that deal with successively challenging control problems and scenarios (e.g. plasma etch, CMP); (b) a standard message-based interface for candidate external controllers to use to communicate with the benchmark system; and (c)

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example implementations and interfaces for both C and Java-based run by run controllers. Elements of the framework are being extended to enable new distributed communication and implementation architectures for run by run control.

Finally, the third key contribution has been the application of run by run control to significantly improve the environmental as well as reduced variation performance of CMP processes. These advances have been enabled by (a) better sensor data availability, and (b) integration of advanced process models with the run by run controller.

CMP Sensors and Process Control for Reduced Consumption

Personnel

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Sponsor

NSF/SRC ERC for Environmentally Benign Semiconductor Manufacturing, Texas Instruments

Chemical-mechanical polishing is a process that is still in its adolescence. Despite poor understanding and poor control in the process, it is being widely pressed into service because it is the only process able to deliver the global planarity required in present and future IC technology. The use of CMP is expanding beyond oxide planarization; it is widely used in metal polishing for plug formation, polysilicon polishing for DRAM cell formation, is crucial to device isolation using shallow trenches (STI), and will be essential for future damascene processes. These expanding applications place stress on water and slurry consumption, pad consumption, monitor and look-ahead wafer usage, and generation of waste and potentially hazardous materials. Most CMP process development is currently conducted without consideration of environmental issues. It is the objective of this project to reduce the consumption of slurry, water, and excess wafers. More broadly, the intent is to develop process control and optimization methods that incorporate environmental objectives as a key concern. For example, there is considerable research and development effort in copper damascene metallization approaches; very little attention has been paid to date to the environment issues in copper waste production or other environmental issues in the copper slurries being considered.

The approach being developed in this research is the practical run by run control of the CMP process, through which the process can be optimized for minimal consumption, and the use of monitor and look-ahead wafers eliminated.

One key barrier is the lack of in-situ sensors for the measurement of polishing uniformity across the wafer. We are developing an approach to indirectly sense and monitor the uniformity of a wafer being polished in-situ. The system incorporates an InfraRed (IR) sensor which is used to monitor the temperature of the polish pad immediately after it has been in contact with the wafer. An IR temperature profile can be obtained by monitoring

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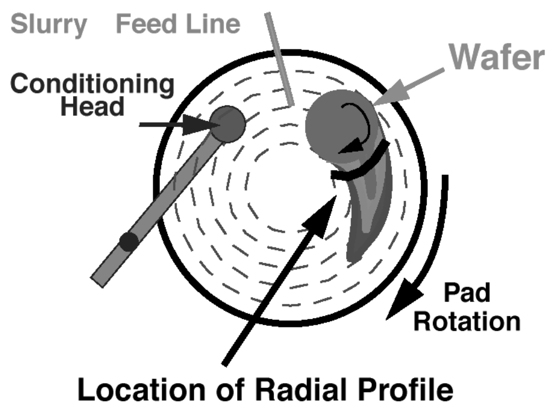
a series of points corresponding to varying radii along the pad surface, as illustrated in Figure 1. This profile is then analyzed spatially to determine the non-uniformity of the polishing conditions. By understanding the correlation between the pad temperature and the spatial wafer temperature profile during polishing we hope to predict the nonuniformity of the wafer that has been polished in-situ eliminating the need for look-ahead wafers.



IR Image of Cu CMP Polishing

Fig. 1: Infrared sensor for examination of pad thermal profile during polishing. IR Image shown during polish of a 4″ copper blanket wafer.

In order to overcome other practical barriers to adoption of run by run control for CMP, additional key issues are being examined. First, integration with an in-line film thickness measurement tool (the Nova sensor) has been accomplished. This approach enables the elimination of substantial monitor and water usage, and results in better control over run to run polish variations. For example, integrated control can reduce lot throughput time from 4 hours 15 minutes with three cleans (in the case where a look-ahead is required) to 2 hours and 22 minutes with one clean step.

Second, a new method for addressing film thickness differences among different products has been developed and demonstrated. Using new semi-physical models of the CMP process, it is now possible to determine the best process design points for minimal and optimal oxide film deposition thickness needed, together with the minimal polish time, in order to achieve the best within-die planarity results. An exciting development has been the integration of these die-level CMP models (which identify product layout-specific polish performance) with a run-by-run control algorithm, as shown in Figure 2. The integrated controller has been able to achieve run by run control to within 200 angstroms of target thickness across two product die types.

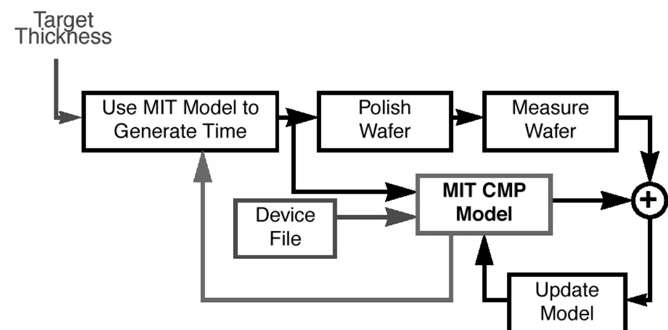


Fig. 2: Integration of MIT CMP pattern dependent model with EWMA time-based run by run controller.

Remote Monitoring and Diagnosis

Personnel

Gower, H. Chen and D. White (D. S. Boning and M. McIlrath)

Sponsorship

MIT Leaders for Manufacturing, NIST Advanced Technology Program

In billion dollar factories, the penalty for down time for any individual piece of manufacturing equipment is very high, not only in lost production, but also in potentially undetected problems in in-process inventory. Early detection of problems, preferably before they become serious, and rapid response to repair or compensate are a high priority for all manufacturing facilities. The problem is made more complex because the number of machines at any location is typically small and there is little sharing of information between locations, even within the same company. The trend towards increased equipment instrumentation and data collection is pervasive, and applies across a large spectrum of manufacturing domains, including semiconductor, automotive, and other industries. As the amount of information that is gathered during normal operation increases with improved instrumentation, the difficulty of assimilating that information also increases making the problem of detection and diagnosis more difficult.

In this project, we have teamed with Stanford University to examine two key aspects of the problem. First, software and network architectural issues to support and enable remote access and monitoring of advanced equipment and manufacturing lines is being explored. For example, an interesting trend is toward the embedding of ubiquitous network interfaces and real time operating systems (e.g. via variants of Java) on individual pieces of equipment and sensors. Led by Stanford, the team is exploring the impact of such interfaces on diagnostic system architectures.

Second, we are developing the algorithmic basis for dealing with the large volumes of manufacturing data that will become available via such interfaces. In particular, "data rich" situations in which hundreds or thousands of time-sampled data streams are available pose interesting challenges and opportunities for monitoring, detection, and diagnosis. We have been exploring variants of multivariate modeling approaches to incorporate the issue of time, including principal component analysis (PCA), partial least squares (PLS), multiway PCA, and other variants. Applications to both semiconductor manufacturing (e.g. plasma etch endpoint) and problems in other industries (e.g. automotive with GM) are being pursued in conjunction with LFM Research Group 4 (Variation Reduction).

Multivariate Methods Using Optical Emission Spectra for Plasma Etch Endpoint Detection

Personnel

D. White, B. Goodlin and H. Chen (D. S. Boning and H. Sawin)

Sponsorship

MIT Leaders for Manufacturing, SRC

This research has examined an approach for automatically identifying endpoint (the completion in etch of a thin film) during plasma etching of low open area wafers. Since many endpointing techniques use a few manually selected wavelengths of emitted light from the plasma, or simply time the etch, the resulting endpoint detection determination may only be valid for a very short number of runs before process drift and noise render them ineffective. Only recently have researchers begun to examine methods to automatically select and weight spectral channels for estimation and diagnosis of process behavior.

This research is exploring the use of Principal Component Analysis (PCA) based T^2 formulation to filter out noisy spectral channels and characterize spectral variation of Optical Emission Spectroscopy (OES) correlated with endpoint. This approach has been applied and demonstrated for patterned contact and via etching using Digital Semiconductor's CMOS6 (0.35 micron) production process. As shown in Figure 3, we have been able to detect endpoint not only in blanket (100%) polysilicon and 10% open area in oxide etch cases, but also get a signal for endpoint detection with 1% open area oxide etch cases. This extremely difficult detection in 1% cases has been accomplished by utilizing the correlation information in several hundred channels from the optical emission spectrum.

Further multivariate methods are being explored for detection of different stages of a complex manufacturing process through multivariate "signature" analysis of the process. In this novel approach, we have applied PCA, but examine both the "loadings" and "scores". That is, we are interested not only in the projection of the data on the eigenvectors of the data as in traditional PCA, but also on the orientation and directionality of those eigenvectors. The application to error detection and diagnosis, as well as to improve low-open area oxide etch endpoint detection, is being explored.

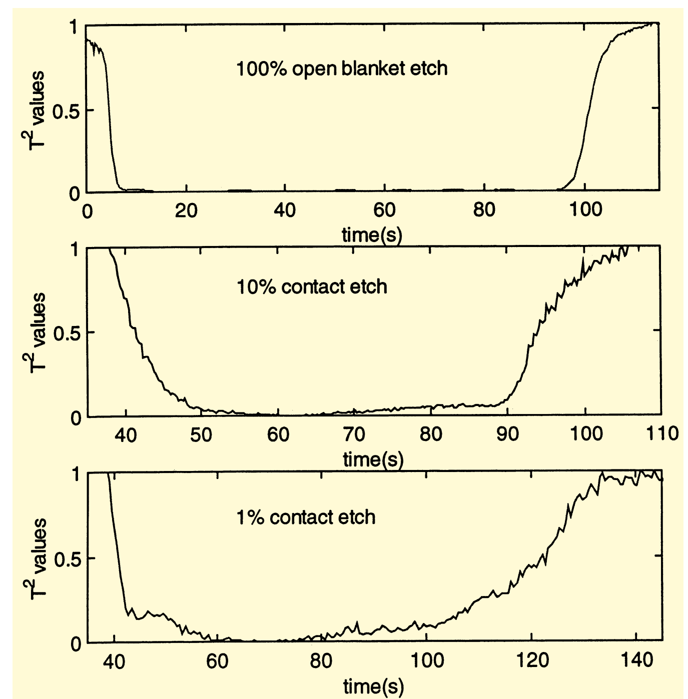


Fig. 3: Plot of T^2 values for three different open area etches. Endpoint detection is now possible for the very difficult 1% open area etch case (at bottom).

Distributed Design and Fabrication Architecture

Personnel

D. S. Boning, M. B. McIlrath, and D. E. Troxel

Sponsorship

DARPA, Stanford University

The design and fabrication of state-of-the-art semiconductor devices and integrated circuits requires an increasingly diverse and expensive set of resources, including manufacturing equipment, people, and computational tools. Advanced semiconductor research activities can be even more demanding, frequently requiring unique equipment and processing capabilities.

We are developing a flexible, distributed system architecture capable of supporting collaborative design, fabrication, and analysis of semiconductor devices and integrated circuits. Such capabilities are of particular importance in the development of new technologies, where both equipment and expertise are limited. Distributed fabrication enables direct, remote, physical experimentation in the development of leading edge technology, where the necessary manufacturing resources are new, expensive, and scarce. Computational resources, software, processing equipment, and people may all be widely distributed; their effective integration is essential in order to achieve the realization of new technologies for specific product requirements. Our architecture defines software interfaces and infrastructure based on existing and emerging networking, CIM, and CAD standards. Process engineers and product designers access processing and simulation results through a common interface and collaborate across the distributed manufacturing environment.

Current efforts in this area focus on the application of this architecture to collaborative microfabrication research, distributed process control and process diagnosis, and remote inspection and analysis of MicroElectroMechanical system (MEMS) devices.

Exploring Semiconductor Device Parameter Space using Rapid Analytical Modeling

Personnel

B. Lee and M. B. McIlrath (D. S. Boning, D. E. Troxel, and A. P. Chandrakasan)

Sponsorship

DARPA

One of the most important decisions a circuit designer must make is the selection of a specific device structure which is to be used within a given circuit design. To find desirable device characteristics, a designer must often revert to potentially time consuming techniques and calculations (e.g., numerical device simulators such as MEDICI). In this project, a software tool has been developed and implemented in Java which allows a designer rapidly to explore the device parameter space for a given technology, as well as across different technologies. The technique of exploring parameter space utilizes a method of rapid analytical modeling to allow for faster, but less accurate, evaluations than one might get through established methods of numerical simulation tools such as MEDICI or PISCES, offering an alternative to such simulators for circuit designers who wish to have rough estimates of parameter variation information, or device structure feasibility.

In general, any semiconductor device can be defined as a device model. Device models are sets of equations which serve to define the current-voltage characteristics of a particular device as a function of several parameters, some of which may represent environmental effects on a device (such as temperature), some of which may represent physical properties of the device (such as channel width), and some of which may represent fitting parameters (such as the channel length modulation parameter). These parameters and the sets of their feasible values form a parameter space which can be thought of as the set of all possible combinations of semiconductor device parameter values.

The idea of semiconductor device parameter space exploration is to examine the subset, or space, of semiconductor parameters under defined electrical constraints, and to determine a method of describing and utilizing the subsets to provide useful information. Specifically, the object of the tool is to determine the feasible parameter space of a specific device model given user-defined electrical and parameter constraints.

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Given a device model which defines a current-voltage relationship as a function of a vector of semiconductor device parameters and a voltage vector (in general, this vector can be thought of as a set of voltages applied to the terminals of a device), there exists a parameter space of all physical parameters of a device. The goal of exploring parameter space is to find a region within the space of all physical parameters where the parameter values of every point within the region meet some specific electrical criteria.

Labnet Software

Personnel

T. Lohman (D. S. Boning, M. McIlrath, and D. Troxel)

Sponsorship

DARPA

University microfabrication laboratories are facing many new challenges and opportunities: facilities are becoming more expensive and difficult to manage; resources and expertise need be shared and made available to a wider community; education and research are becoming more dependent on multi-institutional collaboration. Given the above challenges, there is a growing need for a new distributed information infrastructure to enable remote collaboration, access to remote sites' data and sharing of end-user software applications, in the face of differences between remote sites in computer platforms, operating systems, and technical resources. Past research has been done within this application domain but most working systems are too tightly coupled to their local facilities, suffer from portability problems and have never addressed the issue of data distribution and remote site interaction.

The Labnet Software Project was initiated in recognition of a need for universities to share the development and support effort required to develop and maintain new distributed laboratory information systems. With leadership by Stanford University, three schools — MIT, UC Berkeley, and Stanford — are working to specify and implement the new web-based Labnet Software information system. Key elements of the joint development effort are:

- Standard distributed computing interfaces, including the Object Management Group's (OMG) Common Object Request Broker Architecture (CORBA), OMG's Interface Definition Language (IDL), Sun Microsystem's Java language, and modern relational and object databases.

- Laboratory support software modules that run via a web interface, enabling distributed and remote access to laboratory information.

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- Focused development of critical support functions: equipment reservation, equipment operation and management, and accounting data collection modules are the initial focus.

Deployment of key modules is expected to take place in 1999 within the Stanford, MIT, and UC Berkeley microfabrication laboratories. The Labnet Software will also be made available to other laboratories in order to help support the university community's need for portable, distributed, and collaborative laboratory information system support.

Semiconductor Process Repository

Personnel

M. D. Verminski, W. P. Moyne and M. B. McIlrath
(D. E. Troxel)

Sponsorship

NIST Advanced Technology Program with
On-Line Technologies

We have developed the core of a software system to facilitate distributed process research and design. This core capability allows users to retrieve and examine process flows from multiple process libraries across the network.

A distributed process repository interface has been developed. The repository Application Programming Interface (API) is encapsulated by an OMG CORBA distributed object model and defined by an Interface Description Language (IDL) specification. The process object model used to encapsulate the process repository API is based on the Semiconductor Process Representation (SPR) Information Model. The IDL specification is programming language-neutral; application clients and repository services may be implemented in any language supported by a CORBA-compliant Object Request Broker (ORB) and interoperate across a local or wide-area network. Process repositories may be distributed; process objects and services may be located at various sites transparently to application clients. Applications and services may interoperate using entirely distinct ORB implementations if a common protocol such as the Internet InterORB Protocol (IIOP) or appropriate bridges are available.

The present SPR IDL development includes the base information model. This standard process representation interface provides a common facility to communicate fabrication processes. The fabrication process information organizes processes into smaller subprocesses. At each level, the process can be described from different views. These include the effect of a process on the wafer, the environment around the wafer during the process, and the equipment settings during the process. Each view contains parameters that describe some aspect of the wafer, environment, or equipment during some interval of time. Dynamic attributes (property lists) are also supported for maximum extensibility. The base SPR IDL has been extended to include specific effects and parameters with statistical information.

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A distributed software architecture for semiconductor process design has been defined and implemented in Java with the OrbixWeb Object Request Broker (ORB). The implementation communicates with any ORB adhering to the Internet Inter-ORB Protocol (IIOP). A persistent storage mechanism has been implemented using the Object Design Objectstore Persistent Storage Engine (PSE) for Java.

Other services to manage, query and find distributed objects are being developed. Their interfaces are based upon the Object Management Group's (OMG) CORBA services specifications. A Life Cycle service for creating, deleting, copying, and moving distributed objects has been developed. A Query service and a Trader service have also been implemented. Together, the services provide essential capabilities for the development of distributed and shared applications for semiconductor process research and design.

Statistical Metrology - Quantifying, Modeling, and Assessing the Impact of Spatial Variation in Semiconductor Manufacturing

Personnel

T. Gan, B. Lee, V. Mehrotra, C. Oji, D. Ouma, T. Park, S. Sam, T. Smith and T. Tugbawa
(D. S. Boning and J. Chung)

Sponsorship

DARPA, SEMATECH, PDF Solutions, MARCO

As device and interconnect dimensions continue to scale below quarter-micron dimensions, maintaining process and structure uniformity at each processing step is increasing in importance and difficulty. Yield loss due to systematic sources of variation will begin to supersede loss due to particle defects and random sources of variation. Circuit performance will also become increasingly limited by device and interconnect variation.

Statistical metrology is a new methodology we are developing to quantify, model, and understand the impact of spatial variation in semiconductor processes and device/interconnect structures. Key elements of the methodology include test structures, experimental designs, and measurement methods to gather the large volumes of data needed for statistical analysis; the development of algorithms and tools to decompose and identify variation sources; modeling methods to capture the systematic elements of device or interconnect variation (particularly as a function of layout parameters); and CAD tools and methods to understand the impact of such variation on circuit performance and yield.

The application of these methods have been in two primary areas: pattern dependencies in chemical-mechanical polishing (CMP), and variation in polysilicon and metal linewidths. The following abstracts summarize work on methods for rapid characterization and modeling of CMP in several processes, including interlevel dielectric (oxide) polishing, shallow trench isolation (STI), and in copper damascene polishing. Finally, development and application of CAD tools which utilize variation models (such as those generated in the above experiments) to study the impact of variation on circuit performance is summarized. These studies are collaborative with partners at Applied Materials, Texas Instruments, Sandia National Laboratories, Hewlett-Packard, PDF Solutions, Lucent Technologies, Conexant, and SEMATECH.

Dielectric CMP Characterization Mask

Personnel

D. Ouma, B. Lee and T. Park (D. S. Boning and J. Chung)

Sponsorship

DARPA

In order to enable the characterization and modeling of pattern dependencies in dielectric CMP, a number of specialized test masks have been developed. Our earlier four mask set, developed with HP and Sandia National Laboraties, has been widely used by the CMP community to develop and optimize CMP processes, and to study CMP consumable and tool issues.

In more recent work, we have developed a new unified dielectric CMP Characterization Mask, as shown in Figure 4. In this case a single die can be used to simultaneously extract key model parameters (planarization length) related to density effects, as well study both up area and down area polishing. The die includes step density structures as well as gradual density regions, so that measurements along a scan line can be used to extract planarization length. A pitch region (at constant 50% density) enables study of down area width dependencies which are particularly important for shallow trench isolation polishing. Additional structures facilitate measurement of effective density arising from different deposition processes (e.g. conformal deposition versus high density plasma deposited oxides). The mask is coupled to a spreadsheet program (PLEX) for planarization length extraction based on measurements from the test mask.

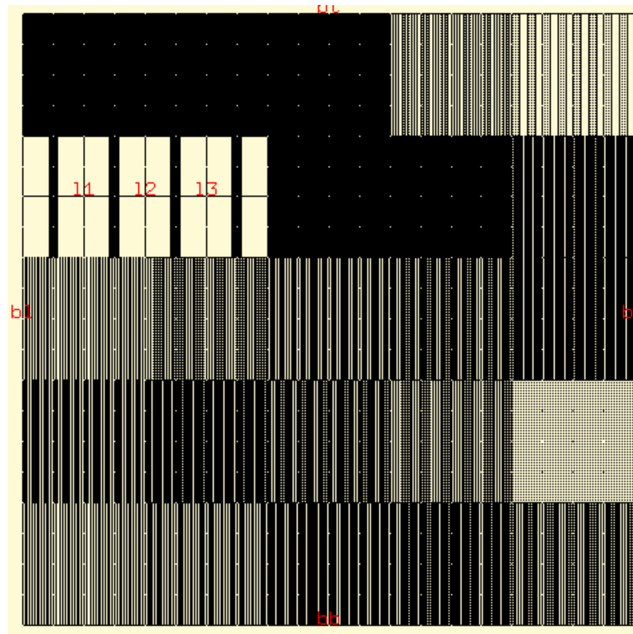

Fig. 4: The Dielectric CMP Characterization Mask

An Integrated Characterization and Modeling Methodology for CMP Dielectric Planarization

Personnel

D. Ouma, B. Lee, T. Smith, and C. Oji (D. S. Boning and J. Chung)

Sponsorship

DARPA, Texas Instruments

Efficient chip-level CMP models are required to predict dielectric planarization performance for arbitrary layouts prior to CMP. We are developing an integrated calibration and modeling methodology for oxide planarization which extends previous work in several important ways. First, we have developed improved characterization methods for model calibration, including new short flow test masks and simplified planarization model parameter extraction. Second, we have developed an efficient physically motivated density calculation and integration with a planarization model for prediction of oxide thickness above and between metal structures across the entire die. Predictions based on the model show excellent agreement when applied to layouts not used in model calibration.

In previous work, we have developed an analytic model for oxide CMP based on an effective layout density calculation. The critical parameter in this model is the "planarization length" or length scale over which the layout is averaged to determine the effective pattern density. Using wafers patterned with the dielectric CMP characterization mask or related patterns, we are able to extract the planarization length from characterization data, and use this to predict the effective density and the local polish rates as a function of position for new layouts, as illustrated in Figure 5.

In recent work, we have integrated this MIT density dependent model with an IMEC model capturing step height evolution over time. The integrated model does an excellent job in predicting not only the "up" area polishing (oxide over metal lines), but also "down" area polishing (the oxide between metal lines).

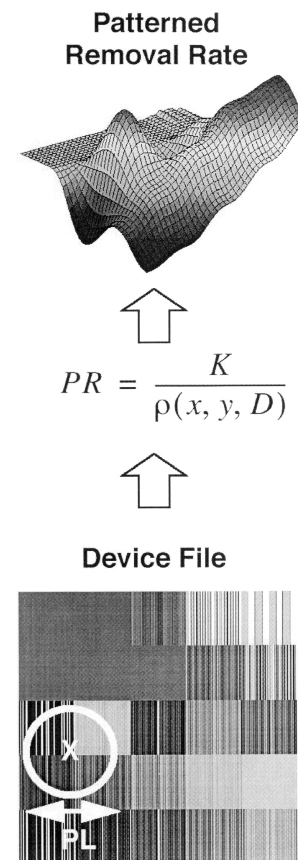

Fig. 5: Model for pattern dependent CMP polish rate, as a function of the effective density calculated across a patterned die.