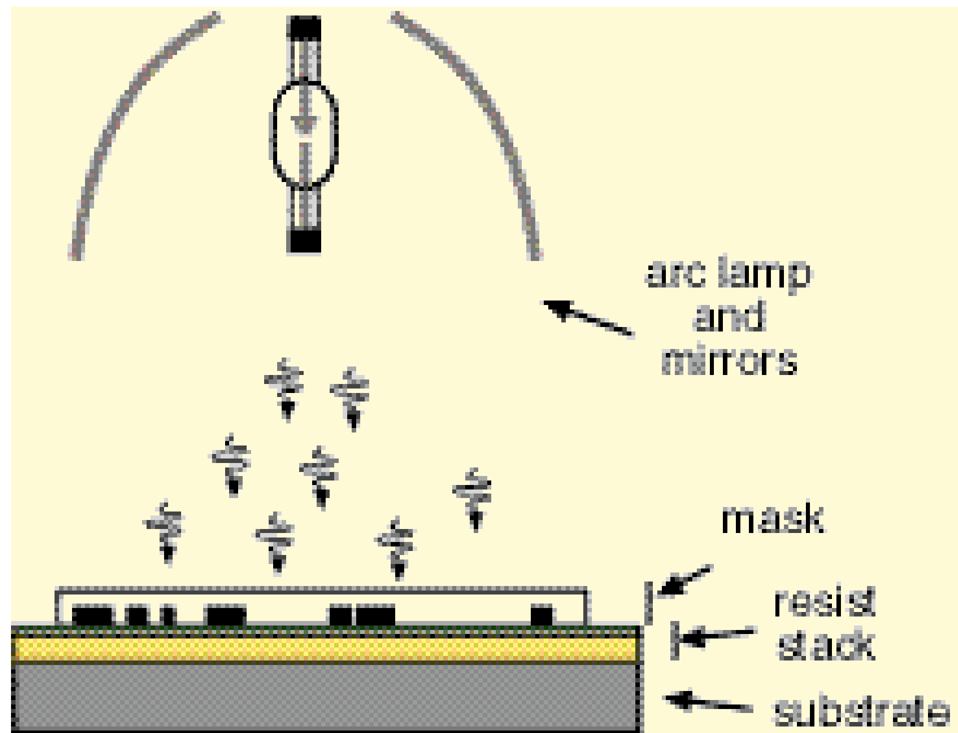
Fabrication Technology



Deep-ultraviolet contact photolithography is a simple exposure process in which the mask, with patterned absorber, and resist-coated substrate are brought into intimate contact. In our experiments, the wavelength of the exposing radiation is as short as 220 nm and comes from a Hg(Xe) arc lamp. (Courtesy of H. I. Smith)

Fabrication Technology

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Sub-100 nm Metrology Using Interferometrically Produced Fiducial Grids

Personnel

C. O. Chen, J. Ferrera, P. Konkola, M. L. Schattenburg
(H. I. Smith)

Sponsorship

DARPA/ARO

The ability to see and measure the results of a process is critical to advancing fabrication technology. Historically, the development of improved microscopy techniques led to rapid progress in microfabrication. Thus, the scanning-electron microscope was essential to the microelectronics revolution. Similarly, the scanning-tunnelling microscope is creating a revolution in the study of interfaces and nanostructures.

In the past, metrology of microstructures and the measurement of workpiece distortion (e.g., a photolithographic reticle or an x-ray mask) has been based on point-by-point measurement through an optical microscope using an X-Y table monitored by a laser interferometer. Although this approach enables relative distances in a plane to be measured with 1 nm-level detectivity, it is expensive, tedious, and subject to a number of shortcomings, including the necessity of placing rather perturbative marks on a workpiece. We have initiated a new approach to metrology for the sub-100 nm domain that is based on large-area fiducial grids produced by interferometric lithography. This new approach is complementary to the point-by-point approach in much the same way that aerial photogrammetry is complementary to ground-based land surveying for the mapping of terrain.

A key element in this new initiative is the holographic phase shifting interferometer (HPSI) interferometer, illustrated in Figure 1. This system, once it is fully developed, will enable us to measure in a global manner the in-plane distortion of a workpiece, provided one of its surfaces contains a shallow fiducial grid. Ideally, the grid on the workpiece will be created by interferometric lithography or a derivative thereof, such as near-field holography.

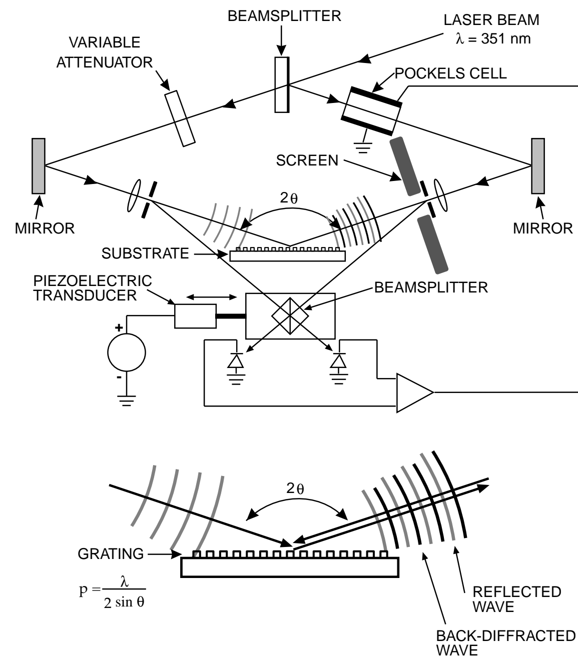

Fig. 1: Schematic of the holographic phase-shifting interferometer (HPSI). A spherical wave back-diffracted from a shallow substrate grid, and a second wave specularly reflected, interfere on a fluorescent screen at the spatial filter. The fringes are imaged onto a CCD. By shifting the beam splitter with a piezo, a computer generates an X-Y map of phase error.

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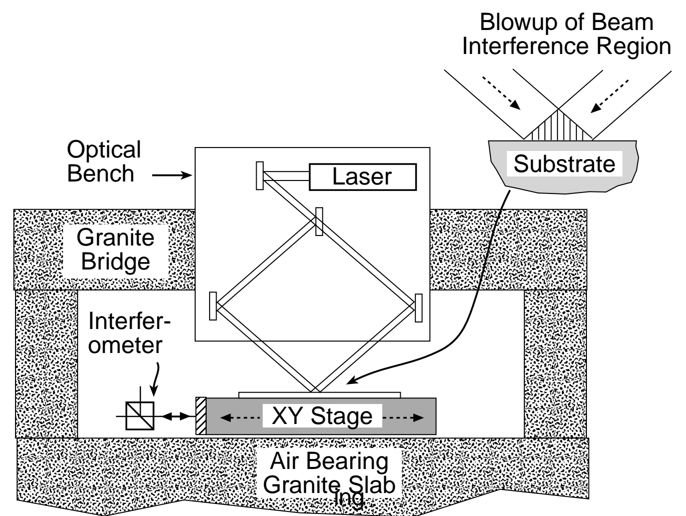
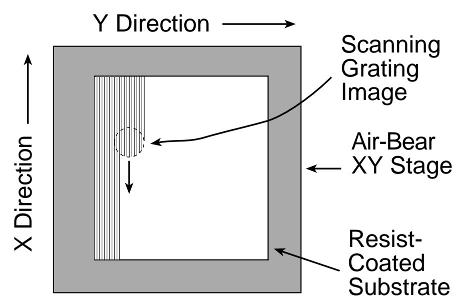
As part of this new initiative in sub-100 nm metrology, we are pursuing a variety of approaches to eliminating the distortion in interferometrically produced grids, decreasing the coefficient of the hyperbolic phase progression (a consequence of creating a grid by interfering spherical wavefronts), and increasing the useful area of fiducial grids. One such approach is scanning beam interferometric lithography (SBIL), depicted schematically in Figure 2. The concept here is to combine the sub-1nm displacement measuring capability of laser interferometry with the interference of narrow coherent beams to produce coherent, large-area, linear gratings and grids. Our ultimate goal is to produce such gratings over areas many tens of centimeter in diameter.



a) Scanning beam interferometer.



b) Grating scanning method.

Fig. 2: Schematic of the scanning beam interference lithography (SBIL) system. A pair of narrow, distortion-free beams overlap and interfere at the substrate, producing a small grating patch. The substrate is moved under the beams, writing a large area grating. Sophisticated electro-optical components (not shown) ensure phase locking of the grating during writing.

Nanometer-Level Feedback-Stabilized Alignment and X-Ray Exposure System

Personnel

Dr. P. N. Everett, E. E. Moon
(H. I. Smith)

Sponsorship

DARPA, SRC through U. C. Berkeley, Suss Advanced Lithography

An experimental high-precision, x-ray exposure and alignment system has been constructed that employs "Interferometric Broad-Band Imaging" (IBBI) for alignment. (Figure 3a). The objective of this system is to achieve ~1nm overlay. The IBBI scheme employs grating and checkerboard type alignment marks on mask and substrate, respectively, which are viewed through the mask from outside the x-ray beam at a Littrow angle of 15 degrees with f/10 optics and a 110 mm working distance. Each mark consists of two gratings (or checkerboards) of slightly different periods, p_1 and p_2, arranged so that p_1 is superimposed over p_2, and p_2 over p_1 during alignment. Alignment is measured from two identical sets of moiré fringes, projected onto a CCD, that move in opposite directions as the mask is moved relative to the substrate. The relative spatial phase of the two fringe sets signifies alignment. Experiments depicted schematically in Figure 3b demonstrated that the displacement scale observed by IBBI is consistent with the scale of a calibrated capacitive sensor associated with a closed-loop piezoelectric drive. Figure 4 shows alignment data read simultaneously from two microscopes, during times when the piezos were alternately scanning and stationary. The difference between the average IBBI reading and the piezo displacement was found to be within 1.5%.

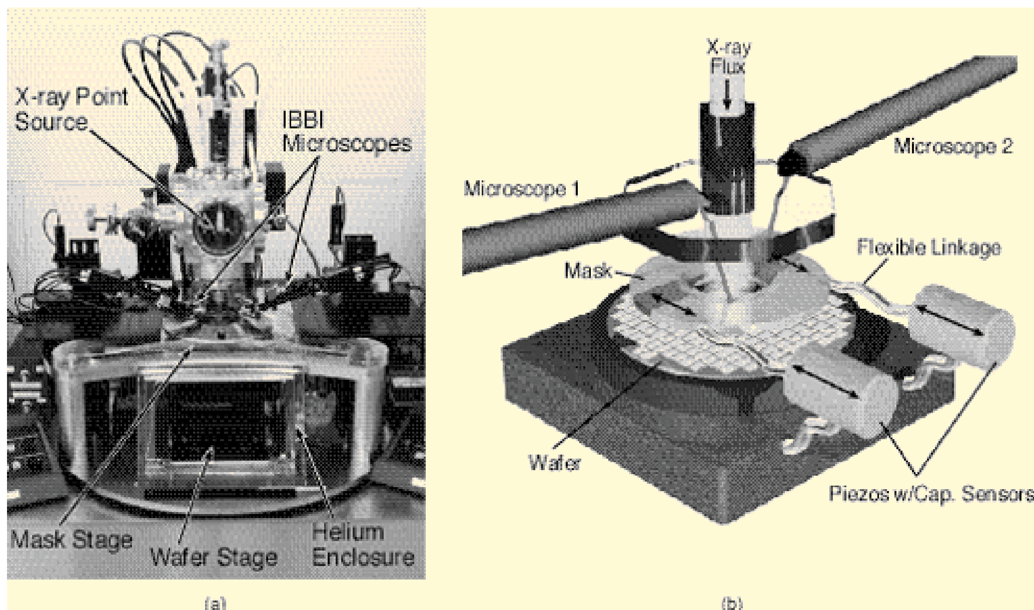


Fig. 3: (a) X-ray exposure and alignment system. Mask and wafer are located in a helium ambient and exposed to x-rays. IBBI microscopes observe alignment through a viewport before and during exposure. (b) Schematic of displacement experiments monitored by IBBI. Alignment is observed at two marks simultaneously by two microscopes. The relative mask-wafer position is controlled by piezos with integral capacitive sensors.

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Experiments showed that IBBI is self-consistent when viewed by two independent optical systems. Two microscopes observed the same mark, as shown in Figure 5, while taking readings alternately. The independent readings had a mean difference of 0.01 nm and a standard deviation of 0.66 nm.

The ability of IBBI to observe nanometer-level alignment during x-ray exposures implies that disturbances can be corrected during the course of an exposure. Figure 6a shows drift and vibration of the exposure/alignment system over a period of several hours, with the system running open loop. Feeding back a correction signal to the piezos (Figure 6b) results in alignment that is stabilized to a mean of 0.0 nm and a standard deviation of 1.4 nm.

The unique capabilities of IBBI alignment are being employed in the fabrication of a variety of electronic and optical devices, including 25 nm effective-channel-length n-MOS transistors.

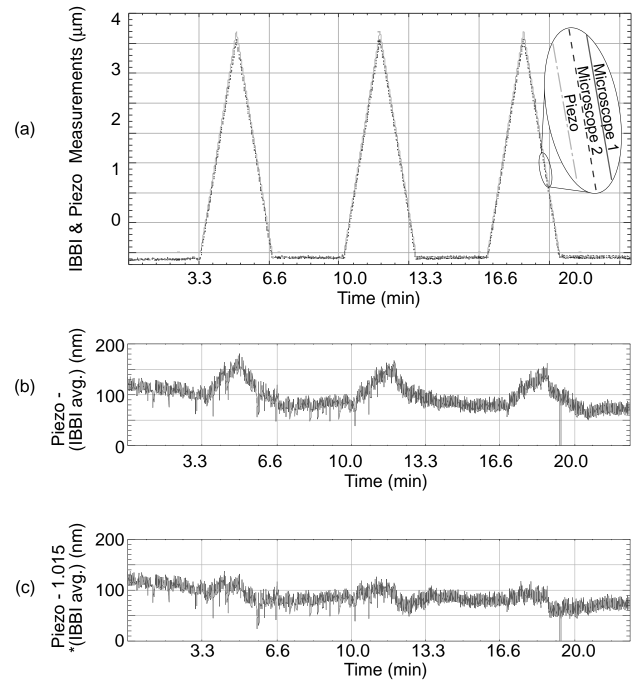

Fig. 4: Agreement between two simultaneous IBBI measurements and piezo/capacitor drives during 3.7 µm back-and-forth scan of mask. (a) IBBI measurements and piezo displacements throughout three scan/rest cycles. (b) Difference of piezo and average IBBI displacement readings, showing residual scale error. (c) Best-fit found with scale increase of 1.5%. The residual scale error is attributed to flexing of the 10 cm of metal separating mask and piezos, and possible pattern magnification during E-beam mask writing.

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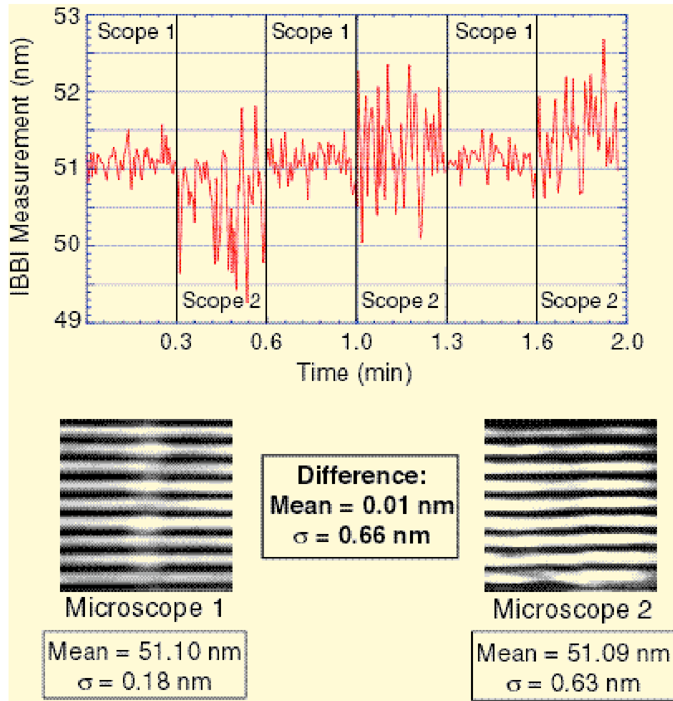

Fig. 5: Two IBBI microscopes alternately observe the same alignment mark from opposite directions, with the mask locked to the wafer at a 3 μm gap. Measurements agree to within σ = 0.66 nm.

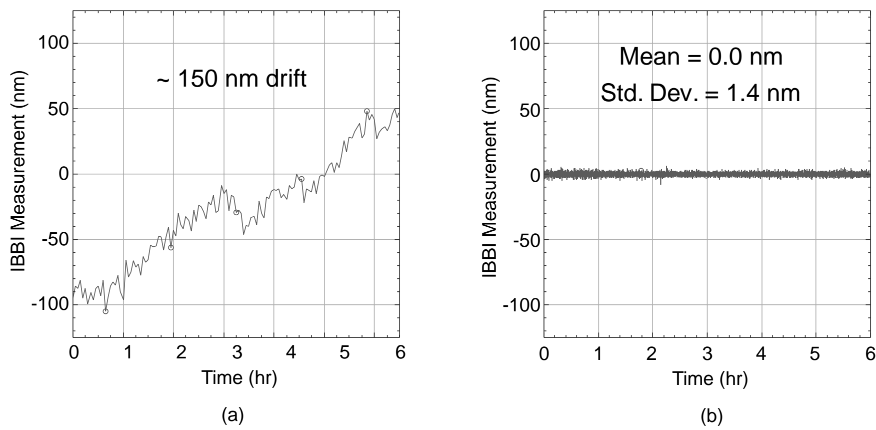

Fig. 6: Six-hour alignment data. (a) Open-loop operation. (b) Closed-loop operation.

Deep-Ultraviolet Contact Photolithography

Personnel

J. M. Daley, M. K. Mondol, Dr. J. G. Goodberlet (H. I. Smith)

Sponsorship

DARPA

A research program in deep-ultraviolet contact photolithography was begun this year. The goal of this project is to demonstrate a lithography process capable of patterning sub-100-nm features at high rates ($> 3\ cm^2/sec$) on spherical surfaces (radius of curvature as low as 8 cm). The lithography scheme must also be amenable to precise multilevel alignment, i.e. subsequently patterned levels must be aligned to previous levels to within a small fraction of the minimum feature size. A successful lithography scheme which meets these criteria will be used to fabricate a smart, wide-field-of-view camera. This camera will have detectors and high-speed signal-processing hardware on its curved focal plane. We believe that contact photolithography best fulfills these requirements.

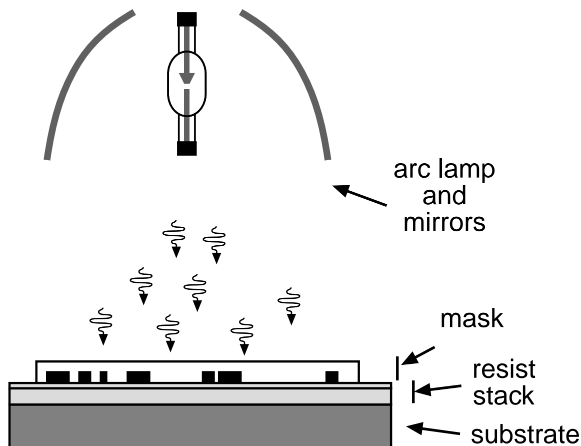

Fig. 7: Deep-ultraviolet contact photolithography is a simple exposure process in which the mask, with patterned absorber, and resist-coated substrate are brought into intimate contact. In our experiments, the wavelength of the exposing radiation is as short as 220 nm and comes from a Hg(Xe) arc lamp.

The basic approach of contact photolithography is depicted in Figure 7. An optically-transparent mask with a patterned absorber is brought into contact with a resist-coated substrate and then exposed with radiation. After exposure, the resist is developed to provide the desired relief pattern. This method was developed earlier for patterning electrodes on surface-acoustic wave devices, which typically had expensive and unconventional substrates. Our initial tasks are to extend the resolution of contact photolithography down to the sub-100-nm regime and then pattern on doubly-curved surfaces. To pattern on the curved surface we plan to use very thin, i.e. 1 to 10 μm thick, conformable membrane masks.

The practical resolution limit of the contact photolithography scheme is determined by the mask design and wavelength of the exposing radiation. We have considered three mask designs: the amplitude mask (AM), the embedded amplitude mask (EAM), and the embedded attenuating phase-shift mask (EAPSM). These designs are depicted in Figure 8. The amplitude mask is the easiest to fabricate, and we have done preliminary exposures with this type. The EAM and the EAPSM are designs which improve the resolution of the lithography by taking advantage of the high refractive index of the mask substrate. This is because the optical mode which traverses the region between absorbers can be confined more tightly in the high-refractive index material and propagate normally rather than decay evanescently. With these masks, the minimum printable feature size is approximately $\lambda/(2n)$, where n is the refractive index of the mask substrate. For the EAPSM, the absorber transmits about 18% of the incident radiation and imparts a pi phase shift to it. This design suppresses undesirable lateral-diffraction. Both the embedded mask designs may be covered with a thin protective layer which will facilitate mask cleaning and assist in minimizing any problems due to particles. Particles are highly problematic for contact photolithography be-

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cause our modeling indicates that for sub-100-nm features, gaps between mask and substrate greater than 20 nm cannot be tolerated. With an exposing wavelength of 220 nm and either the EAM or EAPSM, we expect to print ~70 nm features with broad process latitude.

To measure the resolution limit of deep-ultraviolet contact photolithography, we have conducted several preliminary experiments with 150-µm-thick quartz amplitude masks. In one set of experiments, radiation from a Hg lamp ($\lambda \sim 365$ nm) was used for exposures. In another experiment, a wavelength of 220 nm from a Hg(Xe) lamp was used. Figure 9 shows features patterned via contact photolithography. The first pattern consists of nested L's exposed in 60-nm-thick photoresist. The fidelity of the printed pattern is good and shows no line shortening or corner distortions. The linewidths of the L's are about 145 nm, and the exposure rate was 10 cm^2/sec. Isolated lines of 100 nm width were produced with the 220-nm exposure, but at a much slower rate because of the weak Hg(Xe) lamp and a slow-speed resist. (With the use of a commercial short-wavelength laser, the exposure rate could be increased to more than 3 cm^2/sec.) After development, gold was electroplated into the mold formed by the resist. These results give us high confidence that sub-100-nm features can be patterned with deep-ultraviolet contact photolithography using the EAM or EAPSM.

In subsequent experiments, we will compare the resolution-limit of the different mask designs and evaluate process latitude for each. We will also test multi-level alignment.

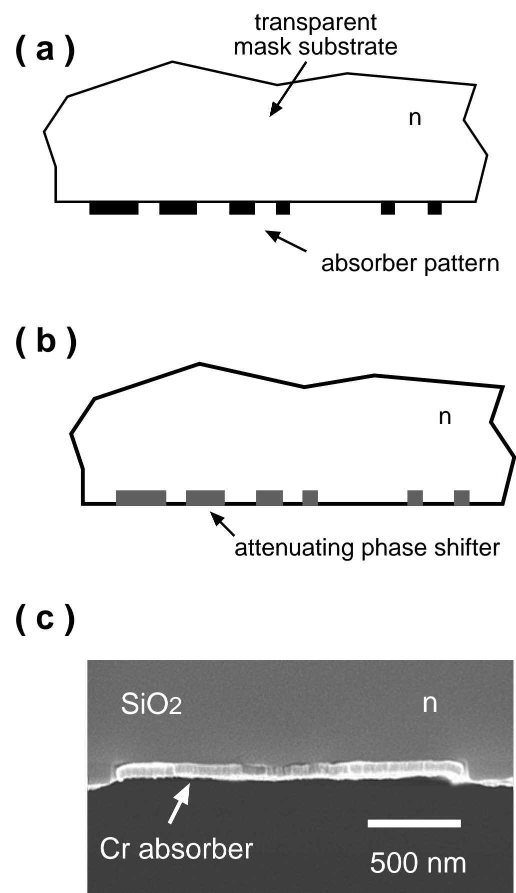

Fig. 8 Close-up views of three mask designs are shown. Details of the patterned region of the amplitude mask (AM) (a) and of the embedded attenuating phase-shift mask (EAPSM) (b) are illustrated. The EAPSM suppresses undesirable diffraction effects. A third mask design, called the embedded amplitude mask (EAM), has been fabricated as shown by the SEM image in (c), and is similar to the EAPSM. The EAPSM and EAM improve the resolution of the lithography scheme by taking advantage of the mask substrate's high refractive index, n.

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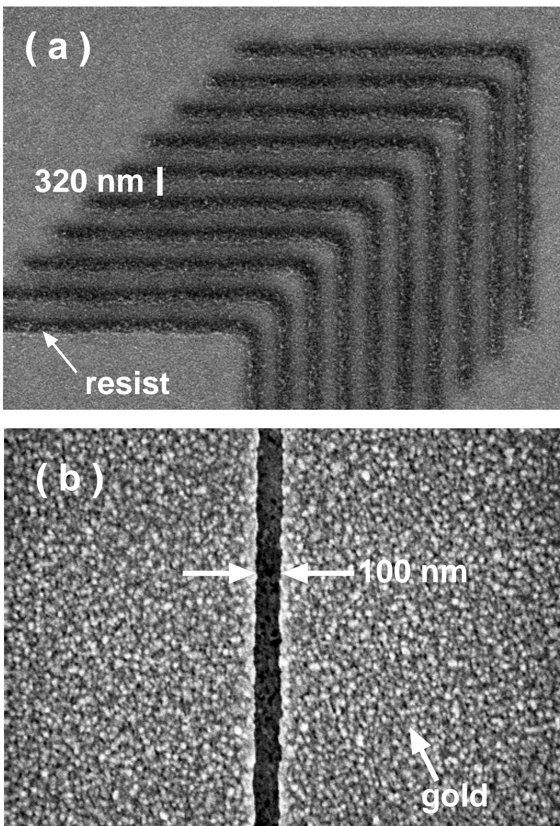

Fig. 9: These patterns were made with amplitude masks and contact photolithography. In (a), nested L's were patterned in 60-nm-thick photoresist with an exposing wavelength of 365 nm. In (b), 100-nm-wide isolated lines were patterned with an exposing wavelength of 220 nm, and after development, gold was electroplated into the mold formed by resist.

Environmentally Benign Process Chemistries and Chemical Recycling

Personnel

J. Chan, A. Reddy, and J. Michel (L. C. Kimerling) in collaboration with Millipore and Stanford U.

Sponsorship

NSF/SRC Ctr for Environmentally Benign Semiconductor Manufacturing and Wafer Engineering and Defect Science Consortium

In today's silicon electronics, control of the surface properties of the starting material, crystalline silicon, is essential for achieving a high process yield for devices with submicron dimensions. While wet cleaning cycles continue to be used widely in IC processing because of their excellent ability to remove particles and native oxides, environmental concerns will restrict the use of chemicals employed in these cleaning processes. It is, therefore, necessary to develop new cleaning processes by understanding the surface chemistries and, based on this knowledge, develop and evaluate alternative chemistries. We have developed a contactless monitoring tool based on the measurement of minority carrier lifetime which is capable of detecting very low levels (10^8 atoms/cm^2, or ppm surface states) of surface defects on high quality silicon wafers. This Radio-Frequency PhotoConductance Decay (RF-PCD) measurement detects any contaminants that generate mid-gap electronic states, including Si dangling bonds and metal adsorbates.

We have developed a new cleaning process using iodine dissolved in alcohol to replace dilute HF as a final cleaning step prior to gate oxidation or epilayer growth. In collaboration with a group in the Department of Chemistry at Stanford University, we have determined that iodine radicals catalyze bonding between surface silicon atoms and oxygen atoms of the alcohol. Further studies have shown the stability of this passivation in air to be superior to the stability of conventional dilute hydrofluoric acid (HF) passivation. We are currently investigating the impact iodine/alcohol passivation has on Gate Oxide Integrity (GOI).

We are studying the processes by which metals in solution contaminate the silicon surface. Using thermodynamic data for the formation of metal compounds, we have modeled the impact changes in solution chemistry have on metal removal capability. Our results show that reducing the acid content of a SC-2

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bath to 10% of the standard value reduces the Fe solubility by 10^3. The increase in metal solubility due to the presence of Cl^- has also been studied and is found to have the greatest impact for concentrated solutions. Both of these calculations demonstrate the trade-off between chemical consumption and cleaning efficiency.

For contamination from HF solutions, we have used RF-PCD to make *in-situ* observations of metal deposition. Our results show that dissolved gases strongly effect the rate of formation of metal-related surface defects. For solutions, which have been saturated with either Ar or O_2, the lifetime degradation due the presence of 1 ppb Cu is nearly an order of magnitude faster than for air-saturated solutions. We are currently performing Total X-Ray Fluorescence (TXRF) measurements at the Stanford Synchrotron Radiation Lab (SSRL) to correlate our lifetime observations with surface coverage data. We have extended our lifetime technique to measure metal contamination in cleaning baths. By measuring changes in the lifetime of monitor silicon wafer, we can quantify the metal concentration of the solution. The second generation of this monitor has demonstrated detection of two hundred parts-per-trillion (ppt) of Cu in a dilute HF solution. This monitor is part of point-of-use HF recycling system designed with our collaborators at Millipore Corp.

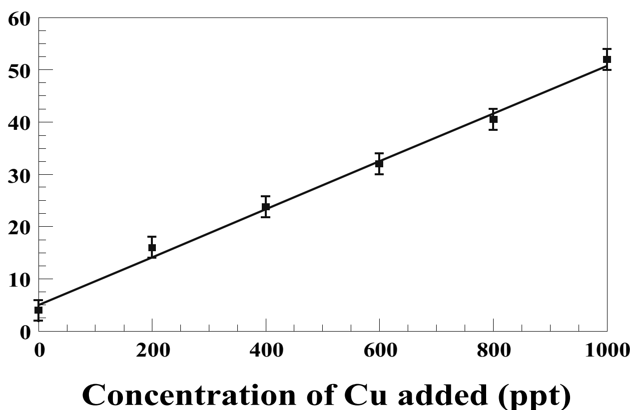

Fig. 10: Response of our bath contamination monitor to Cu spikes in the 200 ppt – 1 ppb range.

Alternative Chemistries for Wafer Patterning and PECVD Chamber Cleaning

Personnel

S. Karecki, L. Pruette, R. Chatterjee (R. Reif)in collaboration with L. Beu (Motorola APRDL) and B. Pogge (IBM)

Sponsorship

NSF/SRC Engineering Research Center for Environmentally Benign Semiconductor Manufacturing

The goal of this project is to identify possible alternatives for perfluorocompound chemistries for wafer patterning and PECVD (plasma enhanced chemical vapor deposition) chamber cleaning of silicon dioxide and silicon nitride films that do not pose long term environmental problems. The etch viability of a variety of alternatives is being determined, and the most promising candidates from the etch viability study are being further tested to define both an alternative chamber clean and an alternative wafer patterning process. The effluents of both processes are being identified with Fourier Transform Infrared Spectroscopy (FTIR) and Quadrupole Mass Spectrometry (QMS) to assess their potential ESH impact. Finally, beta testing of both alternative processes is being performed at the facilities of industrial collaborators.

Most of the experimental work for this phase of the project has taken place on a high density plasma etch tool at Motorola's Advanced Products Research and Development Laboratory (APRDL). The work for the overall project is intended to proceed in three stages for each candidate chemistry: a preliminary "etch viability" or chemical screening stage, to be followed by process-specific testing for both the wafer patterning and the PECVD chamber cleaning applications. An Applied Materials Precision 5000 etch tool housed at MIT's Integrated Circuits Laboratory is used for the screening stage, a high density plasma etcher at Motorola has been used for the wafer patterning process viability stage, and a Novellus Concept One PECVD tool at MIT is used for the chamber cleaning process viability experiments. Diagnostic tools include optical emission spectroscopy for plasma analysis and FTIR spectroscopy and QMS for effluent analysis.

An oxide via etch process has been developed using 2H-heptafluoropropane that offers equivalent (or better, in some aspects) etch process performance to a typical C_3F_8 process with lower emissions of global warming gases critical dimension, and etch rate lag were all factors in evaluating the process performance of 2H-heptafluoropropane as parameters such as source power, bias power, etch gas flow rate, and temperature were varied. The process developed offered an overall emissions reduction of 42% relative to the C_3F_8 reference process. The process developed operates in a standard regime for the HDP chamber, and can be considered as a drop-in replacement for C_3F_8 in this oxide via etch application. However, one hurdle presently blocking the implementation of 2H-heptafluoropropane as an etch gas in manufacturing is its absence from the Toxic Substances Control Act (TSCA) list. Without TSCA listing, most manufacturing facilities will not approve the use of 2H-heptafluoropropane for etch processing. Additionally, there is no current supplier for this compound in semiconductor-grade purity. It is made in bulk quantities at a lower purity for use as a fire-extinguishing agent.

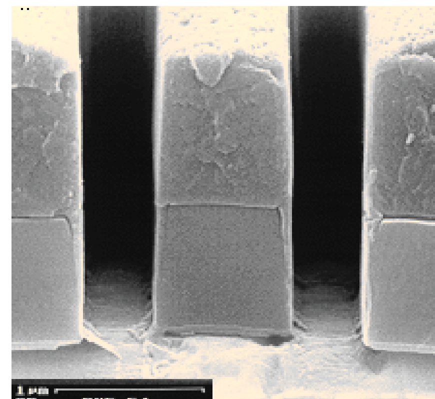

Fig. 11: 0.45 μm (nominal printed CD) via etched in TEOS layer with a 2H-heptafluoropropane process, stopping on metal.

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(Figure 11). Etch rate, photoresist selectivity, anisotropy, Although the etch process developed is both tool and chamber specific, it is likely that processes that demonstrate similarly good performance in combination with reduced emission of global warming gases can be developed using 2H-heptafluoropropane for oxide etch applications in a variety of high density plasma tools.

An effort has also been made to develop an iodofluorocarbon etch gas, 1 iodoheptafluoropropane, as a process gas for key dielectric etch applications in high density plasma etch tools, such as high aspect ratio via etch. Currently, the best 1-iodoheptafluoropropane process recorded offers very good TEOS etch rate (higher than the C_3F_8 reference process) and good sidewall profile. (Figure12) The best emissions reduction relative to the reference process that has been recorded in the present study is on the order of 70-80%. While noticeable gains have been made in improving both via profile and bulk resist selectivity, the latter parameter is still short of the target for this process. Bulk resist selectivity much greater than 3:1 tends to be accompanied by buildup of polymer inside the via and etch stopping.

A new phase of the work on this project will involve exploring the etch behavior of a different family of potential etch chemistries, specifically inorganic fluorine-containing molecules such as NF_3. Moving away from fluorocarbon-based etch chemistries offers the benefit of sharply reducing the possibility of the formation of high global warming potential PFCs as process byproducts. Although highly fluorinated inorganic molecules tend to etch oxide isotropically, sor suggested that the ion bombardment mechani plasma could control an NF_3-based etch to behave anisotropically. An alternative to this approach would be to begin with an inorganic molecule as the main fluorine source for the etch, and add a minimum amount of a polymerizing gas (such as a hydrocarbon or a hydrofluorocarbon) to aid in the polymer formation that is believed to be necessary for high aspect ratio etching. Experimental work on this stage of the project will begin during the spring semester of 1999.

Subsequent work is planned to involve more complete characterization of the effluent of the alternative chemistries, including obtaining a halogen mass balance, as well as further process tests, such as measurement of selectivity to various relevant stop layers and electrical tests to be carried out after metallization following the etch step.

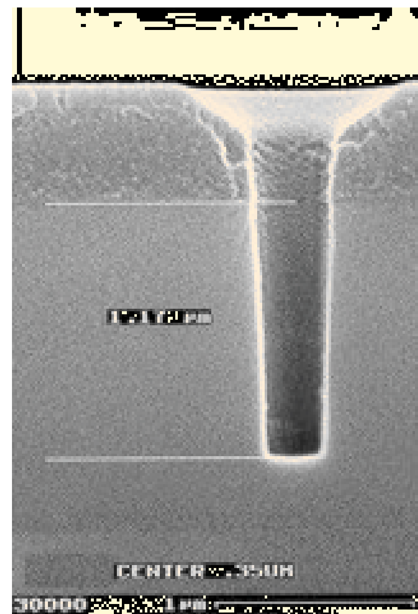

Fig. 12: 0.35 μm via etched in TEOS layer with a 1-iodoheptafluoropropane process.

Layout Pattern Dependencies in Copper Damascene CMP Processes

Personnel

T. Park, T. Tugbawa
(D. Boning)

Sponsorship

SEMATECH, Applied Materials, Conexant

Copper, due to its lower resistivity and higher electromigration immunity compared with aluminum, is rapidly being adopted for next generation VLSI interconnect. Copper damascene CMP processes are now under development in industry to resolve various issues such as process integration, reliability, defectivity, and yield. The goal of this project is to study pattern dependencies of density and pitch (or linewidth and line spacing) in copper damascene CMP processes. The pattern dependent issues include dishing of the copper and erosion of the oxide/copper films, as well as yield issues of line continuity and shorting. Experiments are being performed in conjunction with SEMATECH, Applied Materials, and Conexant.

There are two phases in this research. In the first phase, we are exploring the effect of pattern density and layout patterns on single-level metal polishing. The single layer electrical test mask has been designed for probing line thickness loss as a function of layout patterns. The mask contains pitch structures (with fixed local density) and density structures (with fixed local pitch) to characterize dishing and erosion, respectively. The mask contains electrical test structures (serpentine and comb) to measure line resistances and extract line thicknesses, as well as to study yield issues of line continuity and shorting. Experiments using these and earlier CMP characterization test masks are underway to support modeling of single-layer copper polish pattern dependencies.

In the second phase of this work, additional two and three-layer tests masks are being developed. In the new two-level masks (with SEMATECH), we are studying the impact of underlying topography on the patterning and polishing of second level copper structures. In the three-level masks (with Conexant), we are also interested in the impact of topography and pattern dependencies on via formation and reliability. Models and characterization methods to address these concerns are important for development of advanced multilevel interconnect technology.

Chemical Mechanical Polishing for Shallow Trench Isolation (STI)

Personnel

D. Ouma, C. Oji, and B. Lee
(D. Boning)

Sponsorship

DARPA, Applied Materials, Sandia National Laboratories

Shallow trench isolation (STI) is emerging as the isolation methodology of choice as the drive for device density intensifies. However, solution of layout pattern effects at the CMP planarization phase is critical to cost-effective single-mask STI processes. Pattern effects in STI are particularly severe and complex; it is first manifest at the overburden oxide polish phase resulting in a nonuniform time-to-reach the nitride capping layer across the die. This necessitates over polishing to completely remove the oxide and ensure complete nitride stripping. The over polishing together with higher oxide polish rate results in substantial dishing of the trench oxide in dense trench regions and rounding of silicon nitride around the trenches. In order to control and account for the pattern dependencies, understanding of the polish mechanism in both phases is needed.

In this project, we have characterized and modeled the pattern dependencies exhibited at the two polish stages. Using a dedicated mask to delineate the specific pattern dependencies, we have explored a range of polishing process conditions and consumables such as pads and slurries. Different oxide deposition techniques have also been examined; in particular, the oxide topography generated by HDP plasma versus TEOS deposition is important. We find that the conformal deposition profiles (TEOS) and "pyramidal" profiles (HDP) result in radically different effective densities profiles across the die which must be accounted for in CMP modeling. Based on such corrected effective densities, the oxide component of the polish can be well explained. We have used a simple selective nitride model with a similar density dependence to study the nitride erosion component of the polish. This STI CMP characterization and modeling methodology is helpful in defining process control windows and requirements for successful trench formation, and for exploration of process alternatives with decreased variation.

Ultrathin 600°C Wet Thermal Silicon Dioxide

Personnel

J. Appenzeller (J. A. del Alamo, in collaboration with R. Martel, K. Chan and P. Solomon, IBM)

Sponsorship

IBM, Deutsche Forschungsgemeinschaft

Present trends in ultra large-scale integration demand the development of ultrathin gate silicon dioxide of high quality. Often this requirement is coupled with a restricted thermal budget. Since in small devices dopant diffusion cannot be tolerated, it is important to develop new silicon oxidation processes at low temperatures. This is a challenge because the quality of an oxide depends strongly on its growth conditions.

The goal of this project is to extend conventional wet thermal oxidation to low temperatures. By establishing a temperature gradient in an oxidation furnace, we were able to grow oxide films at 600°C while keeping the temperature at the gas inlet at 750°C necessary for a safe and complete pyrogenic reaction between hydrogen and oxygen. The inset of figure shows a sketch of the temperature profile.

Using this approach we were able to grow very uniform silicon dioxide films in the range from 20Å to 60Å. The growth rate in the wet environment was found to be 5Å/h to 6 Å/h depending on substrate orientation. Figure 15 shows the leakage current through the oxide as a function of gate voltage for a 25Å, a 28.5Å and a 33Å oxide layer. The measured values of current density are in good agreement with theoretical predictions for high temperature gate oxide films indicating the high quality of our wet thermal oxide. In addition, we have investigated the breakdown voltage and interface trap density. Breakdown fields were found to be around 13 MV/cm and interface trap densities in the low 10^{11} $cm^{-2}eV^{-1}$ could be achieved by an adequate forming-gas treatment.

In summary, the performed electrical measurements indicate that wet thermal oxide grown under the conditions described above should be considered readily available to grow high quality gate oxide films.

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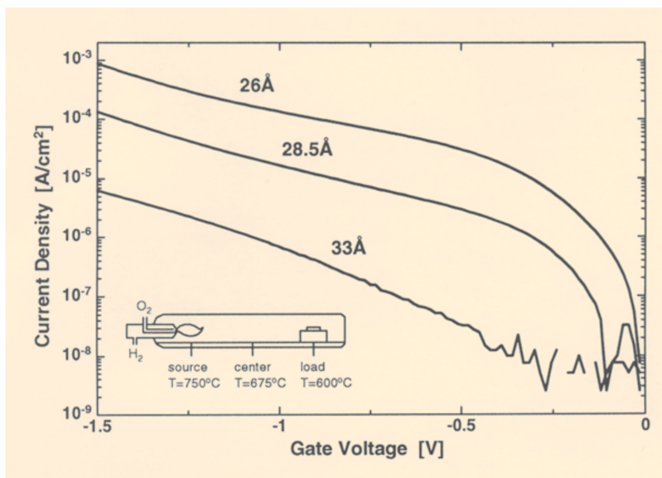

Fig. 15: Leakage current density for three different oxide thicknesses as a function of gate voltage. The inset shows a sketch of the temperature profile in the oxidation furnace.

Low Turn-on Voltage and High Uniformity n-type Silicon Field Emitter Array Fabrication and Characterization

Personnel

M. Ding (A. I. Akinwande)

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Si field emitter array technology is being explored for potential application in devices such as Field Emission Displays (FEDs), sensors, microwave amplifiers and switches. The technology is amendable to the integration of Si FEAs with MOSFETs to make smart field emitters. A typical Si field emitter is made up of a mircon-sized cone located within a gate aperture. An applied gate voltage establishes potential difference between the cone tip and the gate, resulting in high electric field at the cone tip. Electrons tunnel into the vacuum through the barrier at the tip and are accelerated to the anode which is biased at higher voltage than the gate.

The objective of the project is to fabricate high performance Si field emitter arrays using chemical-mechanical polishing (CMP) and correlate the current-voltage characteristics with the structural parameters (such as tip radius and aperture width) and materials parameters (such as work function). Our initial goal is to fabricate Si FEAs to explore the performance of the devices when the tip is coated with low workfunction materials such as diamond or AlN. Later, we plan to conduct simultaneous imaging of topology (tip radius) and surface potential (workfunction) using a UHV Scanning Maxwell Stress Microcope which is under construction.

We report a doped-poly-silicon gate Si Field Emitter Arrays (FEAs) fabricated with Chemical Mechanical Polishing (CMP) that have extremely low turn-on voltage and negligible gate current. Furthermore our devices show excellent uniformity for different sized arrays which are crucial for device reliability and mass production. We fabricated FEAs with 1-µm aperture on 4-inch (100) n-type silicon substrates with dopant concentration of about 10^{16} cm^{-3}. SEM analysis indicated that the radius of curvature of the tip is about 12.3 nm.

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An example of the device transfer characteristics for 10x10, 20x20, 30x30 and 60x60 FEAs on a single die is shown in Figure 18. The devices were characterized in UHV at an anode voltage of 1000 V. The figure shows the average currents per tip as a function of gate voltage. Devices turn on at about 25-30V, however we have observed turn-on voltage as low as 20V on some arrays. This is the lowest reported turn-on voltage for 1-µm aperture devices compared to typical 50-60V of metal FEAs before field forming and conditioning. We also observed the negligible gate leakage currents that are 3-4 orders of magnitude smaller than emitter current as shown in Figure 18. We attribute the low turn-on voltage to the extremely small radius of curvature of the Si tips. Figure 19 is the Fowler-Nodheim plot of the 4-µm 60x60 FEA. The emitted current obey Fowler-Nordheim theory. From the slope of the FN plot, b_{FN}, an effective field enhancement, $\beta(E=\beta V_G)$, where E is the electric field at the emitter tip) was calculated to be $7x10^5$ cm^{-1}. Using a simple electrostatic argument ($\beta=1/r$) we extracted an equivalent tip radius of about 14.3 nm which is in very close agreement with the SEM measurement of 12.3 nm.

Currently we are installing the Scanning Maxwell Stress Microscope system to image simultaneously the topology and the surface potential of the emitter. We are also fabricating FEAs with different emitter materials or coatings and will study how these processes affect the performance of the devices.

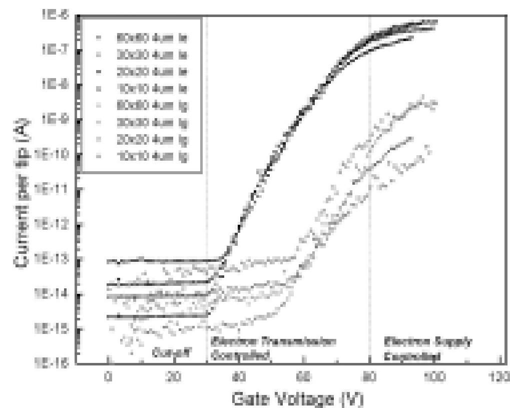

Fig. 18: Average Emitter and Gate Currents as a function of gate voltagefor 10x10, 20x20, 30x30 and 60 x 60 Si FEAs.

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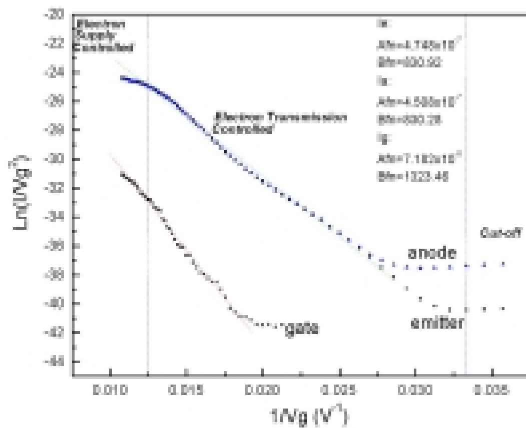

Fig. 19: Fowler-Nordheim Plot of the average emitter and gate currents for a 60x60 4-μm pitch FEA

Molybdenum Field Emitters with Integrated Focusing Electrode

Personnel

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Being an *emissive* display, the Field Emission Display (FED) outperforms today's dominant flat panel display technology, the liquid-crystal display, in the areas of brightness, viewing angle and luminous efficiency. A typical Field Emission Display consists of a base plate with a matrix of field emission arrays and a phosphor coated screen, separated from the base by insulating spacers. The breakdown field of these spacers limits the ratio of anode voltage to anode/cathode separation. Anode voltages of 5-10 kV are needed to use high voltage phosphors, whose brightness, luminous efficiency and lifetime characteristics are superior to those of low voltage phosphors. However, anode voltages of this magnitude require cathode/anode separation of 1-10 mm in order to avoid breakdown of the spacers. Since the emitted electron beam has an angular spread, electrons follow parabolic trajectories to the anode. Thus, higher cathode/anode separation leads to cross talk between neighboring pixels, which lowers display resolution. Keeping the cathode-anode separation small and thus preserving display resolution permits the use of only low-voltage phosphors, which have lower luminous efficiency, brightness and lifetime. Thus, in today's FEDs there exists a trade-off: luminous efficiency, brightness and screen lifetime *vs*. screen resolution.

A way to overcome this tradeoff is to collimate the emitted electron beam by focusing. The goal of our research effort is to simplify beam focusing by using micro-fabrication to integrate the focus electrode with the cathode. This approach, referred to as the Integrated Focus Electrode Field Emitter Arrays (IFE-FEAs), can be implemented in four different ways, and shown on Figure 20. Our choice of focusing scheme was based on our analytical model of the device. The modeling led to the following two important, easy to implement conclusions: (i) the most effective focusing is achieved when the focus electrode is positioned above (rather than outside) the gate

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electrode and there is one focus electrode per tip (rather than per pixel), i.e. the local, out-of-plane configuration (#2 in Figure 20). Since our stated objective was to optimize focusing, our design and fabrication efforts were concentrated on the out-of-plane, local IFE-FEA (ii) effective focusing calls for minimizing the thickness of the dielectric between the focus electrode and the gate electrode (i.e. the vertical separation between the focus and the tip). However, the dielectric strength of the oxide imposes the low limit of about 0.5 microns. In other words, effective focusing requires the focus electrode to be as close as possible to the tip, and this was implemented in our devices (see Figure 21). On the minus side, the present configuration also maximizes the reduction of the emission current by the focus electrode. We argue that this is overcome by operating at a higher gate voltage.

The IFE-FEAs that we fabricated have gate and focus electrodes made of doped polysilicon and separated from each and from the cathode by insulating layers of silicon dioxide. The emission tips were fabricated with a Spindt-type process, utilizing angular evaporation of aluminum parting layer, followed by vertical evaporation of molybdenum. After the cones are formed, the parting layer is lifted off removing unwanted molybdenum. The final device structure is shown in Figure 21.

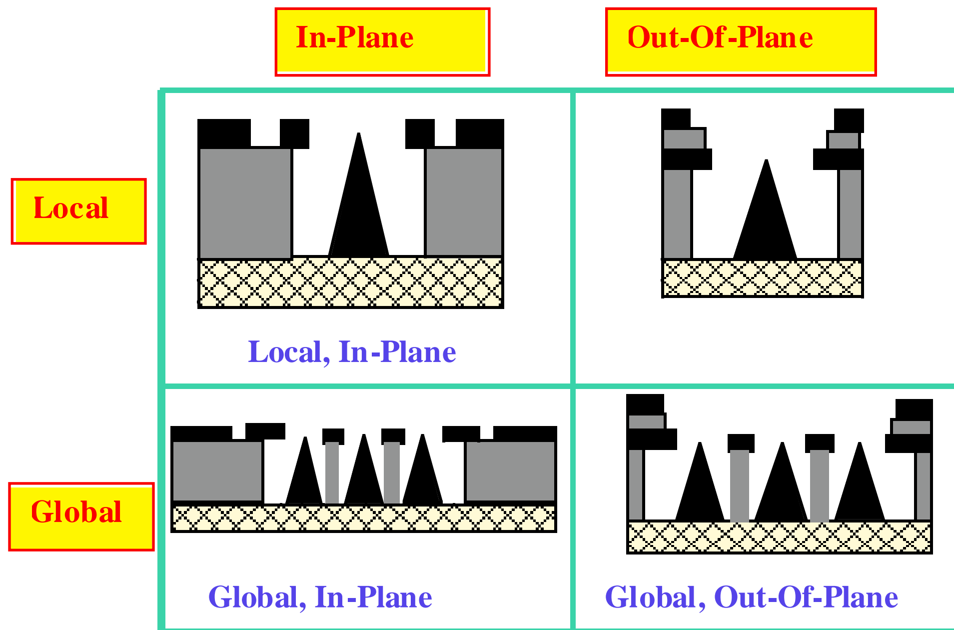

Fig. 20: Integrated focusing themes.

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Extensive electrical characterization of the devices was carried out. The first stage of this study involved taking 3-terminal IV characteristics of arrays of different sizes. In the 3-terminal measurements, the gate and focus voltages were kept equal to each other and were varied together. The Fowler-Nordheim plots of the 3-terminal IV data are linear, in agreement with theoretical expectations as shown in Figure 22. Next, we studied the gate and focus transfer characteristics of the devices; e.g., the variation of the emission current with focus voltage, gate voltage being kept constant. The focus transfer characteristic is a particularly important parameter because it gives an indication of how much the emission current will be reduced as a result of focusing the emission beam.

Finally, preliminary optical characterization did demonstrate the focusing effect that we aimed for. An instrumentation setup for quantitative spot size measurements is currently being developed. However, our devices were extremely susceptible to breakdown when operated in the focusing mode. The breakdown resulted from a large voltage differential between the gate and focus electrodes. We plan to overcome this problem by (i) lowering the operating voltage either through improving the current process or through making devices with silicon tips (ii) investigating the breakdown mechanisms and dielectric strength limitations of the insulating oxide.

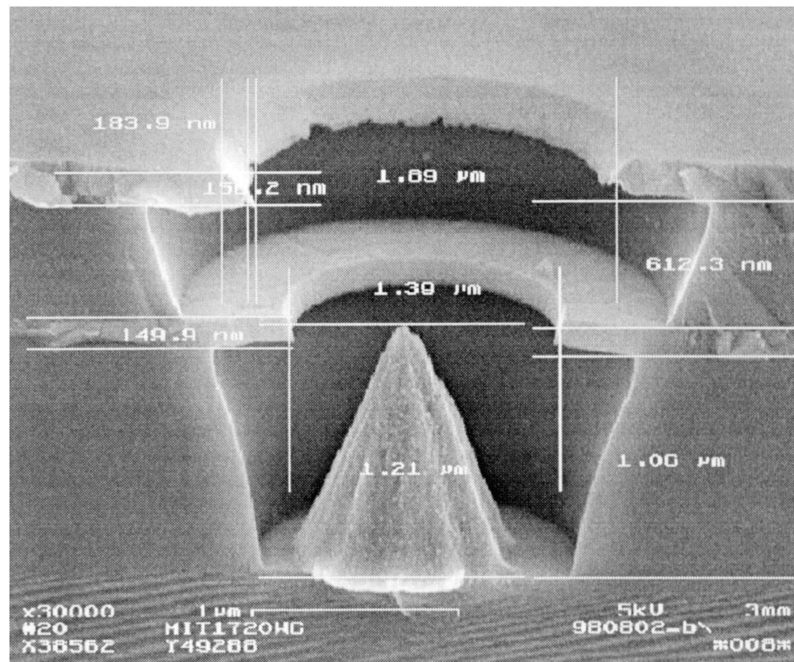

Fig. 21: An IFE FE cone with dimensions.

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Field Emitter Arrays with High Aspect Ratio

Personnel

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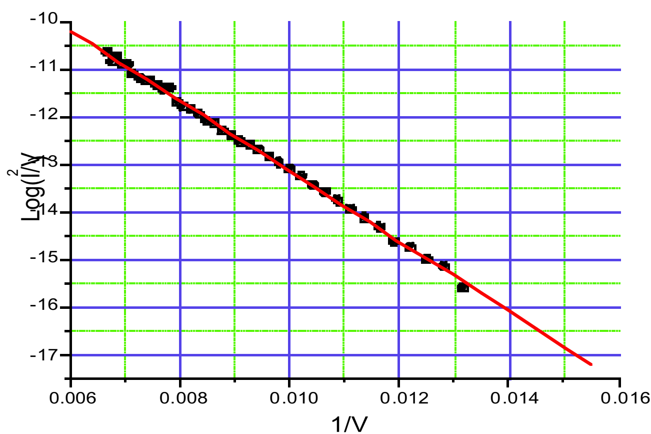

Fig. 22: FN plot of IV data from a single tip (A_{FN}=-11.56; B_{FN}=-803 $\beta \equiv E / V \cong 7.8 \times 10^5\ cm^{-1}$)

The goal of this project is to improve the performance of field emitter arrays (FEAs) by increasing the device aspect ratio (tip height/aperture width). The electrical performance of FEAs depends on its geometrical parameters such as radius of curvature, gate aperture and cone base angle. The ideal emitter is a tall vertical pillar with a very sharp top located within a narrow width gate aperture. This shape, high aspect ratio FEA, will yield low capacitance, low dynamic power dissipation, fast switching speed and low leakage currents.

Two areas of benefit of a high aspect ration FEA are (a) driver circuit power dissipation and (b) FEA reliability and lifetime. Typical FEAs have aspect ratios of about one1eading to high capacitance between the row and column electrodes in a typical display because of the thin insulator. Consequently, FED driver circuit power dissipation will be reduced as the aspect ratio of the FEA increases. Another benefit of high aspect ratio FEAs is that the increase in the insulator thickness reduces the average field across the insulator for the same gate operating voltage. This results in lower electron tunneling through the dielectric (gate current) and hence trapped charges in the insulator and damage of the insulator.

Numerical simulations of the cone deposition process indicate that several parameters in the fabrication process contribute to the final shape of the cone. The geometry of the initial structure (parting layer and initial gate opening radius), various process parameters (temperature, degree of flux collimation), and material parameters (diffusion coefficients, surface tension) affect the evolution of the cones with time. One important result of the simulations is that the shallower bevel angle of the gate opening results in higher aspect ratio cones. We fabricated FEAs cones with aspect ratios of about 3:1 as shown in Figure 23, using gate apertures and parting layers with shallow bevel angles.

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Scanned Laser Annealing of Patterned Films

Personnel

C. Hau (C.V. Thompson)

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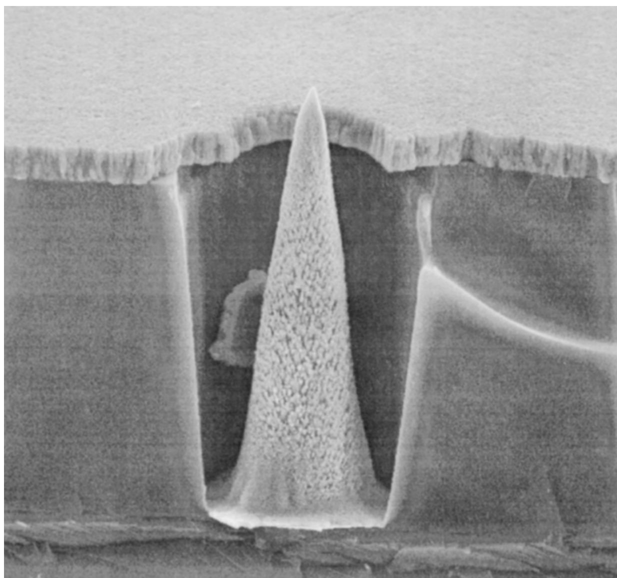

Fig. 23: Field Emitter Arrays with high aspect ratios.

Patterned polycrystalline films are used to interconnect devices and as device elements in electronic, magnetic, photonic and microelectromechanical devices and microsystems. When patterned feature sizes are comparable to the grain sizes of these structures, their properties and reliability can vary dramatically with minor variations in their grain structures. We have developed a process for scanned laser annealing of individual patterned structures in order to manipulate grain structures for basic studies of structure-property relationships, and to develop an engineering tool for reprocessing of patterned structures for performance optimization.

In our apparatus a Nd:YLF laser spot is scanned along a feature by translation of the wafer relative to the fixed laser beam (see figure24a). We have scanned polycrystalline films patterned into lines and shown that polycrystalline structures can be converted to large-grained 'bamboo' structures with grain boundaries normal to the line axes. These structures can be obtained in lines for which conventional uniform anneals would not yield bamboo structures. We have studied the mechanism for this structural conversion through simulation of the grain structure evolution process during scanned annealing. Both simulations and experiments demonstrate three regimes of structure evolution, agglomeration, uniform grain growth and evolution to bamboo structures, depending on the laser power, the scan speed, and the geometry of the line structure (see figures 24b and 24c). Simulations suggest that under appropriate conditions, near-single-crystal structures should be obtained. We are developing thermal models for input for simulations of structure evolution, and we are continuing experiments on patterned Al films as well as initiating experiments on patterned Cu.

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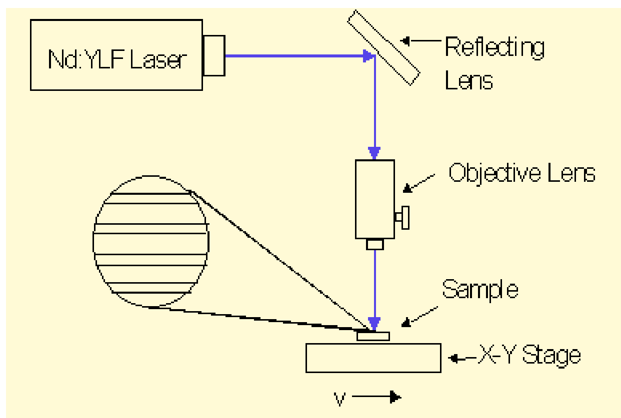

Fig. 24a

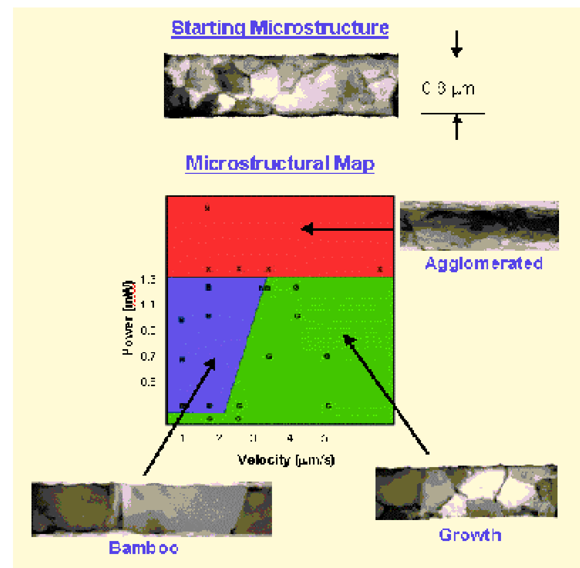

Fig. 24b

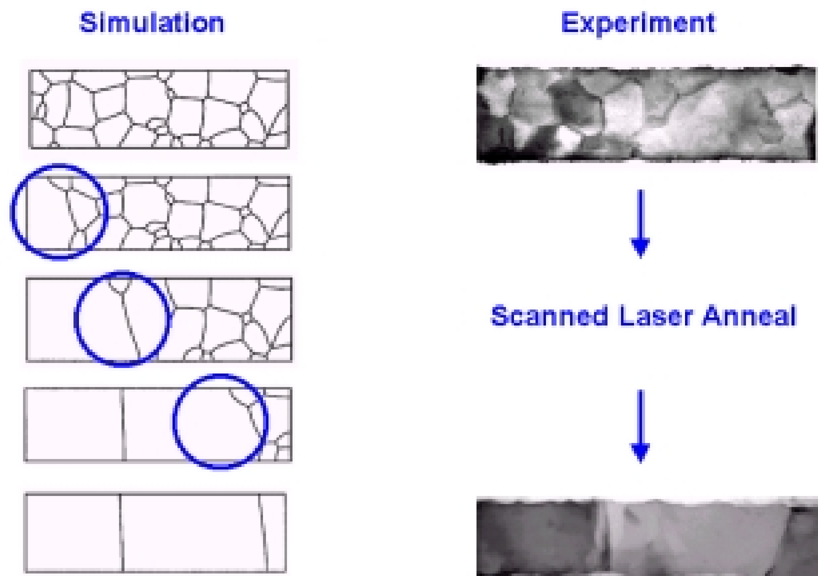

Fig. 24c