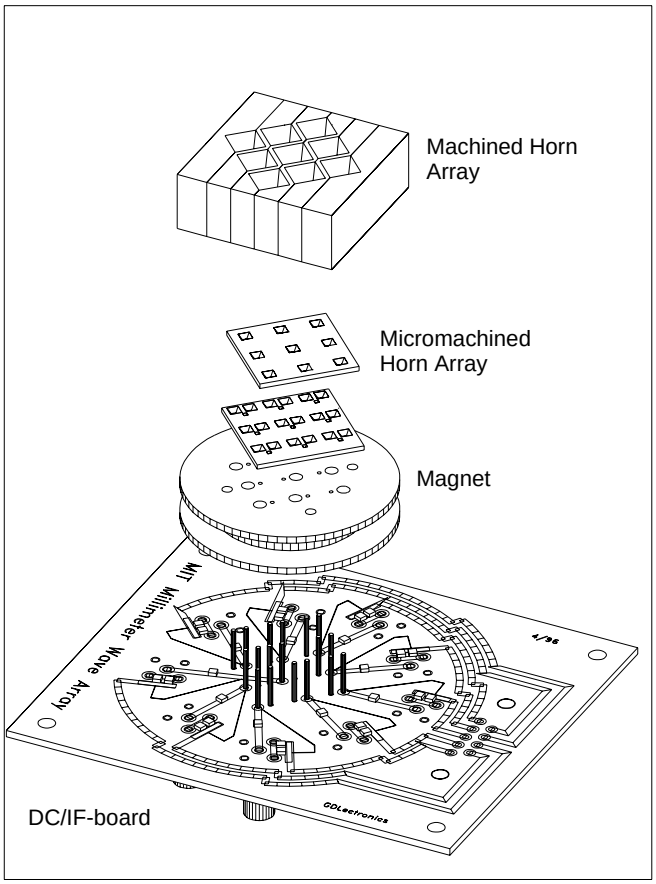

Schematic of an array structure including a micromachined and machined horn array, the device wafer, and the dc and IF connection board. (b) I-V curves of seven SIS junctions in the array. (Courtesy of Q. Hu)

Electronic Devices

- *CMOS Technology for 25 nm Channel Length*
- *Design and Fabrication of Single-Mask 50 nm MOSFETs*
- *Self-Aligned Double-Gate CMOS Technology for 3-D Integration*
- *Self-Aligned Dual-Gate Variable Threshold Voltage (VT)CMOS Technology*
- *Correlation of Silicon Microroughness on Electrical Parameters of SOIAS (Silicon-On-Insulator With Active Substrate)*
- *RF SOI LDMOS Power Devices*
- *High-density Silicon Substrate Via Technology*
- *Hydrogen-induced Piezoelectric Effects in InP HEMTs*
- *Drain Resistance Degradation in InAlAs/InGaAs Metamorphic HEMTs*
- *A Dynamic Model for the Kink Effect in InAlAs/InGaAs High-Electron Mobility Transistors*
- *Silicon field emitter arrays integrated with MOSFET devices*
- *Vertical MOSFET / Field Emitter Array Technology*
- *Low-Power Driver Circuit for Organic Light-Emitting Diode Displays*
- *Micromachined SIS millimeter-wave focal-plane arrays*
- *Fabrication of large area nanomagnet arrays for ultra high density magnetic data storage*

CMOS Technology for 25 nm Channel Length

Personnel

A. Lochtefeld and M. Meinhold (D. A. Antoniadis and H. I. Smith)

Sponsorship

DARPA and ONR

The scaling of CMOS transistors into the sub-100 nm region is extremely challenging because of short-channel effects. We are pursuing two distinct approaches that should permit scaling to 25 nm channel lengths. Both can be considered 3-dimensional-gate CMOS (3DG-CMOS) technologies. One is a planar double-gate configuration, with either joint or independent control of the two gates per MOSFET; the other features a gate that surrounds a pillar-like vertical channel.

Monte-Carlo modeling predicts that double-gated devices that are scaled to L_{eff} = 25 nm will have transconductances G_m in excess of 2000 mS/μm, while maintaining almost perfect sub-threshold slope. However, models also predict that the tolerance in aligning front and back gates has to be within Lg/4 in order to avoid performance deterioration due to overlap capacitance. The Lg/4 requirement translates into 6 nm alignment tolerance for a 25 nm channel. In order to meet this alignment challenge we will use the IBBI (Interferometric Broad-Band Imaging) alignment technique which achieves sub-nanometer misalignment detectivity. The planar double-gate devices will be fabricated starting with a SIMOX wafer. First the gate stack for the back-gate will be deposited and patterned by x-ray lithography. The structure will then be covered by a layer of CVD oxide, planarized, and bonded to a "handle wafer". The bulk of the SIMOX wafer will then be chemically etched using the back-oxide of the SIMOX wafer as the etch-stop. The fabrication will then follow a conventional SOI process, with front gate precisely aligned to back-gate layer using the IBBI alignment scheme. The final structure is depicted in Figure 1.

The second approach to 3DG-CMOS utilizes epitaxially grown vertical pillars of Si, potentially allowing optimization of dopant profiles beyond that achievable via implantation in planar MOS devices. Epitaxial definition of a vertical channel allows almost arbitrarily short L_{eff} with tighter control than possible with lithography. Previously demonstrated processes for epitaxially-defined vertical MOS structures generally start by etching a pillar from an epi wafer, and suffer from severe difficulties in the subsequent contact and isolation of gate and source/drain regions. These problems are avoided in our proposed vertical-MOS process, illustrated in Figure 2. The gate electrode material and isolation layers above and below are first deposited. A hole is etched to the underlying Si seed later, followed by LTO gate-oxide deposition and selective epitaxial growth of the channel. Critical lithographic alignments are avoided in this process.

The scalability of vertical surround-gate (VSG-) MOS versus planar double-gate (DG-) MOS has been addressed through numerical simulations. It is clear from analytical solutions that, for the case of equivalent VSG pillar diameter / DG film thickness, surround-gate allows more control over the channel. However, for a given lithography generation silicon film thickness can likely be much smaller than the diameter of vertical pillars. It is therefore more relevant to compare performance at a fixed lithography node, with process variation taken into account. Figure 3 shows the minimum acceptable L_{eff} for VSG and DG devices at the 50 nm lithography generation, assuming +/- 10 % process variation in lateral dimensions. Clearly DG devices with sufficiently thin silicon films can be scaled shorter than VSG while maintaining electrostatic integrity. However, VSG devices should enjoy a packing density advantage, resulting in respectable current drive despite longer channel length, as shown in Figure 4.

We have developed a key technology for our vertical MOS device, UHV-CVD selective epitaxy in deep submicron holes. Figure 5 shows perfect filling of 100 nm holes, with no defects at the growth interface or along oxide sidewalls. Defects are limited to the regions of lateral overgrowth, where the growth front merges with that from an adjacent hole. In-situ doping levels of

$5x10^{19}$ cm^{-3} (p-type) and $3x10^{19}$ cm^{-3} (n-type) have been demonstrated. We are currently investigating electrical characterization of devices (initially, pn-junction diodes) grown epitaxially in 100 nm holes.

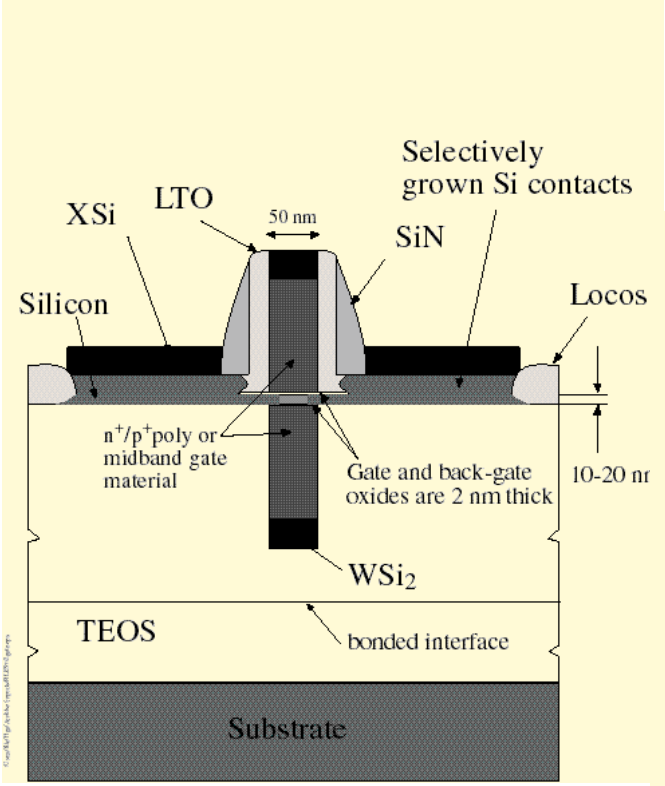

Fig. 1: Double-gate NMOS transistor with 25 nm effective channel length. Gate-to-gate alignment is via IBBI.

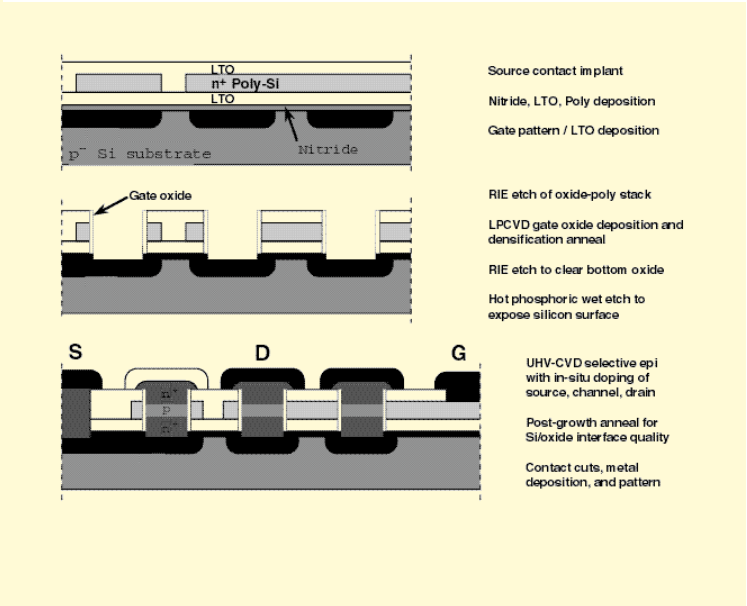

Fig. 2: Process for fabricating surround-gate vertical MOS devices.

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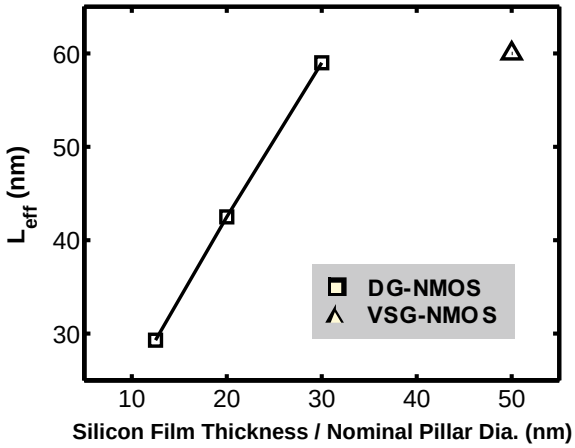

Fig. 3: Simulation results: Minimum acceptable L_{eff} (for $I_{off} = 1x10^{-8}$ A/mm) for DG- and VSG-MOS designs. $T_{ox} = 1.5$ nm, $V_{dd} = 1V$, $V_{th} \sim 400$ mV. Midgap gates.

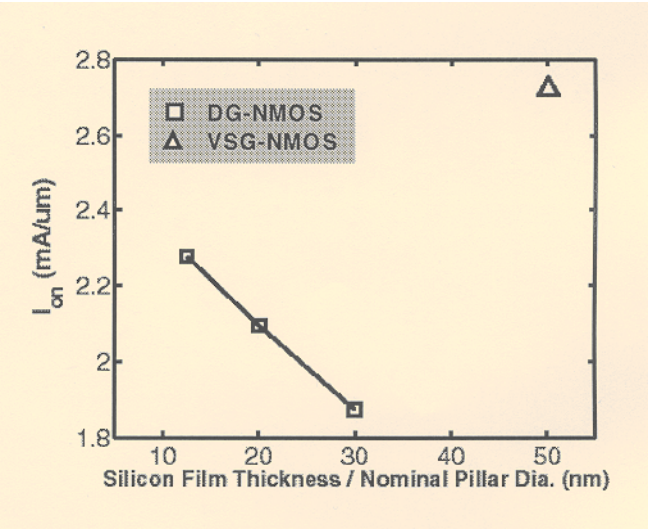

Fig. 4: Simulation results: Drive-current density for DG- and VSG-MOS designs. $T_{ox} = 1.5$ nm, $V_{dd} = 1V$, $V_{th} \sim 400$ mV. Midgap gates. Hydrodynamic models used.

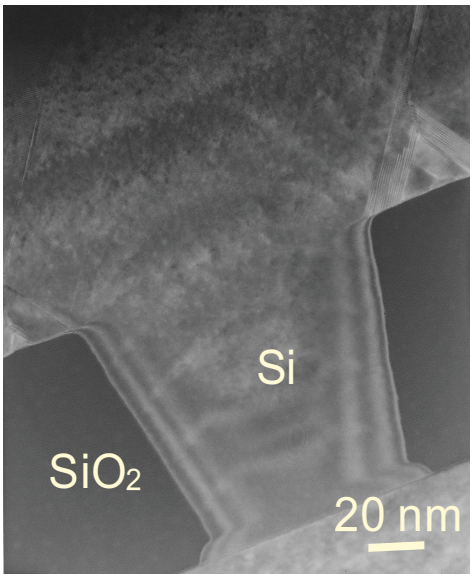

Fig. 5: TEM image of selective epitaxial filling of 100 nm holes in SiO_2

Design and Fabrication of Single-Mask 50 nm MOSFETs

Personnel

K. M. Jackson and Z. Lee (D. A. Antoniadis and H. I. Smith)

Sponsorship

DARPA

As MOSFET dimensions are scaled to lengths below 100 nm, significant challenges arise in controlling fabrication processes. Rapid turnaround between process changes and device results, and an ability to extract the exact structure and doping of the fabricated device are tools critical to the development. The first requires a short-flow process that focuses only on the fabrication steps that critically define device performance in a minimum number of steps. The second tool, known as inverse modeling, couples a device simulator with an optimizing routine that shifts the doping in the simulated device until the current-voltage and capacitance characteristics of the simulated device match those of the real device. This project focuses on creating a short-flow process for 50 nm channel-length MOSFETs, and coupling it with currently exisiting inverse modeling capabilities.

The short-flow process we have concieved will allow working MOSFETs to be fabricated in one mask step. It is shortened from a normal full-length MOSFET process by eliminating the need for oxide isolation around the devices and by eliminating the need for the passivation and metal layers at the end of the process. Two types of structures will allow operational MOSFETs to be fabricated without field-oxide isolation. The first is an annular device where the source is completely enclosed inside of a gate and the drain is outside of the annular gate. The second structure is a figure-eight configuration (Figure 6) where the parasitic out-of-channel (i.e. field region) source-to-drain current is less than 0.02 times the in-channel current under the gate in the center of the structure. By using a self-aligned cobalt-silicide process (salicide) the source and drain will be low enough in resitivity that they can be contacted directly by probes. Even though two significant steps of the conventional fabrication process are left out, the steps that define the device operation - the gate stack, implantation, and critical high temperature steps - are all contained in the short-flow process.

The gate-level lithography (the only lithography step) for the short-flow process will be done using X-ray lithography, easily allowing linewidths down to 50 nm. The mask will be fabricated with a mix of optical steps for the large features and e-beam writing for the fine gates. Using optically placed e-beam registration marks, the e-beam tool can match the in-plane scale and distortion of the optical projection tool to achieve good pattern placement.

The key elements in the fabrication of sub-100 nm devices are the placement of dopants and the use of very thin gate oxides. The accomplishments on the project this year have been in establishing process steps for these two key elements. NMOS and PMOS capacitors and long-channel MOSFETs with 20 Å gate oxides have been fabricated and show low defect densities. They have active gate dopings around $4x10^{19}$ cm^{-3} at the polysilicon/oxide interface with minimal Boron penetration in the PMOS. A combination of low energy implants (1 - 2 keV Boron for the PMOS) and short, well-controlled thermal cycles (5 sec. or less at 1000°C) have allowed us to achieve source and drain depths of less than 10 nm for both NMOS and PMOS. These junctions have near ideal forward bias chartacteristics, and have very low leakage in reverse bias. Having developed working processes for these device elements, the next set of devices will focus on optimizing the design of the ~ 30 nm deep source and drain extentions, and the placement of counter-doping, as halos or pockets around these junctions.

Once devices are fabricated using the short-flow process, their doping and structural components can be evaluated via inverse-modeling, using current-voltage and capacitance measurments. Understanding what doping profiles were achieved versus the original design then will allow us to go back and adjust the process and to see how changes affect the doping profiles in the device. This approach should facilitate the optimization of device fabrication for deep-sub-100nm MOSFETs.

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Self-Aligned Double-Gate CMOS Technology for 3-D Integration

Personnel

A. Ritenour and A. Wei
(D. A. Antoniadis)

Sponsorship

SRC

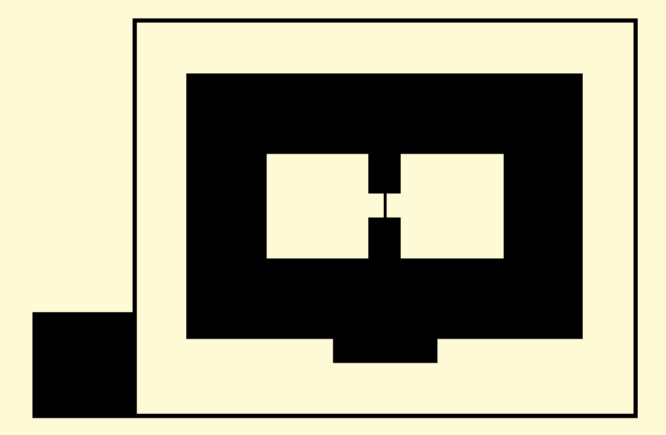

Fig. 6: Gate mask layout of a figure-eight geometry MOSFET. The inner two white square areas are the source and drain probe pads that will be salicided. The dark wide ring is the gate pad with the active gate being the fine line in the center. The outer ring is a guard ring.

Continued CMOS scaling into the sub-100 nm regime requires the use of fully-depleted double-gate MOSFET's to alleviate short channel effects and meet device performance requirements. Self-alignment of the bottom-gate to the top-gate is very important, so as not to introduce additional parasitic overlap capacitances. Double-gate devices also have the potential to offer double-sided operation. This will be critical for integration of CMOS technology into 3-D integration schemes.

Shown below in Figure 7 is a fabrication scheme which realizes a bottom-gate which is self-aligned to the top-gate. This fabrication involves formation of the top-gate stack on an SOI wafer. A chemically-modified layer is then formed through the top-gate, e.g. via implantation. This will serve as an etch mask to form the bottom-gate. The wafer is then flipped and bonded to a handle wafer, and the substrate of the SOI wafer is removed leaving the self-aligned chemically-modified layer as an etch mask for the bottom-gate.

With this fabrication scheme, double-gate devices can be fabricated with the top- and bottom-gates fully self-aligned. In addition, self-aligned double-sided double-gate devices can be fabricated if the top-gate device is fully processed up to interconnect before flip and bonding. The bottom-gate side can then also be fully processed up to interconnect and then bonded to other layers of devices similarly fabricated, resulting in full 3-D integration of CMOS devices.

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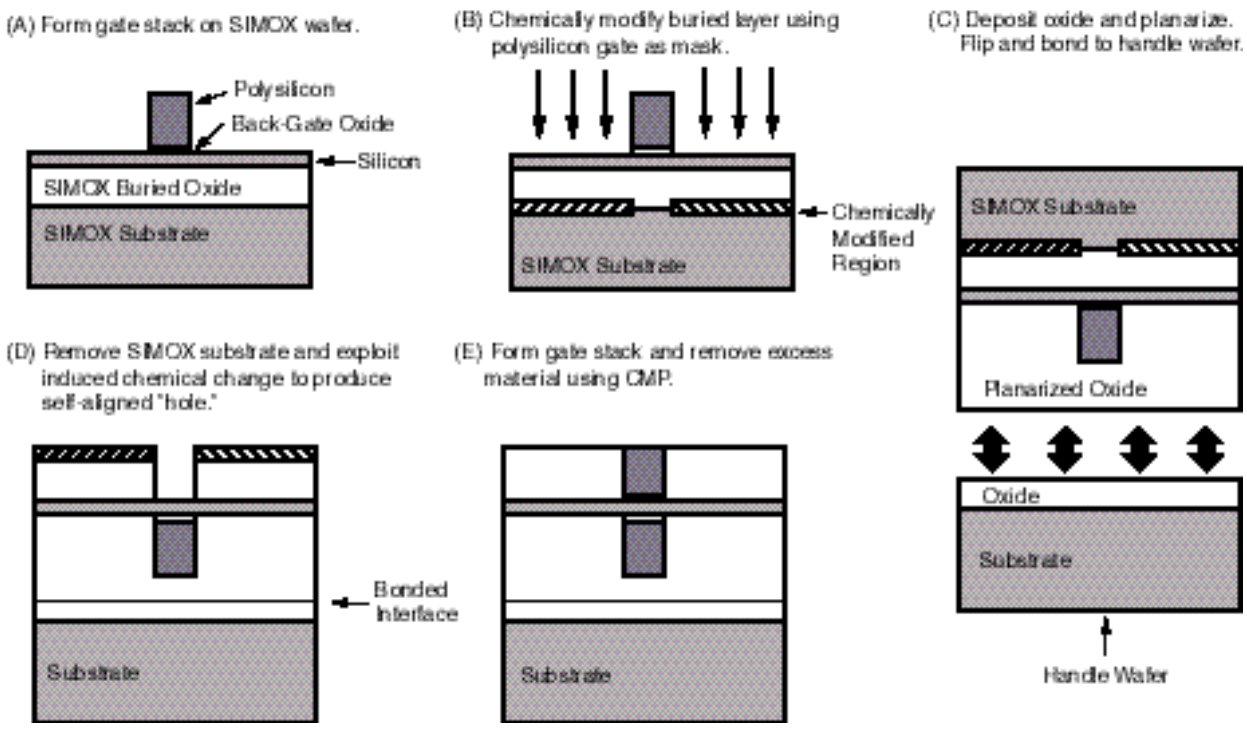


Fig. 7

Self-Aligned Dual-Gate Variable Threshold Voltage (VT)CMOS Technology

Personnel

A. Wei and A. Ritenour (D. A. Antoniadis)

Sponsorship

SRC

Continued power supply scaling in CMOS technology requires scaling of device threshold voltage to maintain circuit performance. However, reduced device threshold voltage leads to unacceptably high off-state leakage current, particularly as device dimensions are reduced. A variable threshold-voltage CMOS technology allows for reduced threshold voltage during periods of high circuit activity, and an increased threshold voltage when the circuit is idle for long periods of time.

A silicon-on-insulator with active substrate (SOIAS) has been demonstrated in which a buried back gate is used to modulate the front gate threshold voltage of a fully-depleted SOI MOSFET. Fully-depleted SOI MOSFET's are ideal for variable threshold voltage technology due to their inherently low threshold voltage, and the addition of the backgate facilitates fully-depleted SOI MOSFET scaling into extreme submicron regimes. Alignment of the front and back gates is difficult, however, and SOIAS technology used an oversized backgate, formed in buried unpatterned polysilicon. Oversize of the backgate leads to a large drain-to-backgate overlap capacitance resulting in degraded performance.

Shown below in Figure 8 is a representational cross section of a self-aligned dual-gate variable threshold voltage CMOS. The structure is a fully optimized version of SOIAS technology featuring self-alignment of front and back gates, silicided front and back gates, and silicided raised source/drain to minimize series resistance in the fully-depleted MOSFET. It is fabricated by forming the backgate stack on an SOI wafer. The backgate stack is silicided, patterned, filled with dielectric, chemical-mechanical-polished flat, flipped, and bonded to a handle wafer. The substrate of the SOI wafer, now on top, is removed in a chemical etch, and the buried oxide of the SOI wafer is removed leaving the SOI film on which to build devices. Devices are aligned to the prepatterned backgates. The prepatterned backgates are oversized relative to the front gate in order to meet alignment tolerances. Full self-alignment is achieved by counterdoping of the backgate through the frontgate in order to form regions with low doping. This should significantly reduce overlap capacitance. A raised source/drain is then formed by selective epitaxy and the top device is silicided and contacted.

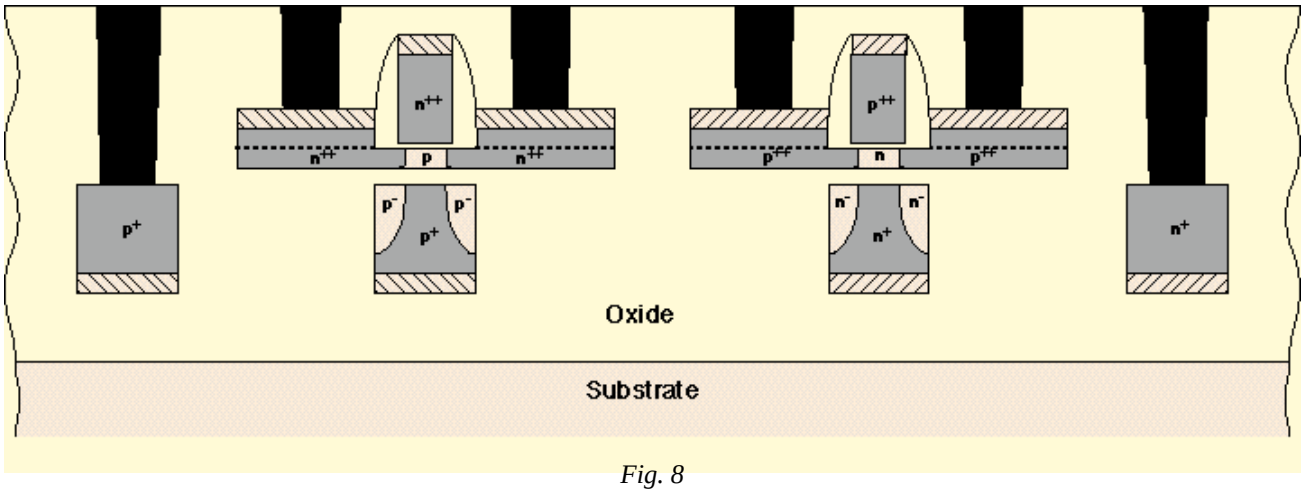


Fig. 8

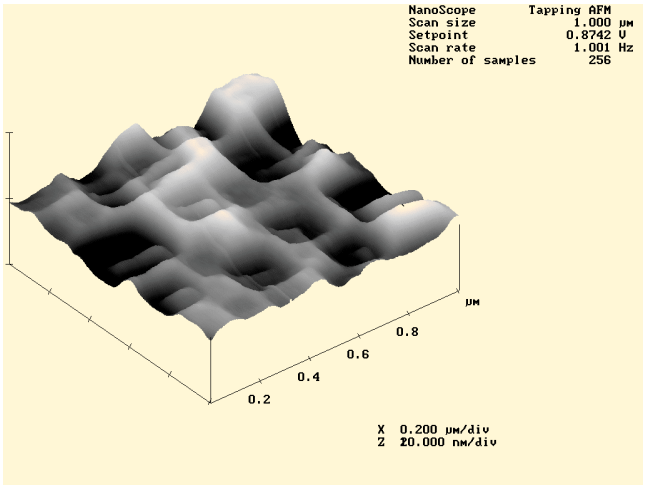
Correlation of Silicon Microroughness on Electrical Parameters of SOIAS (Silicon-On-Insulator With Active Substrate)

Personnel
H. Nayfeh (D.A. Antoniadis)

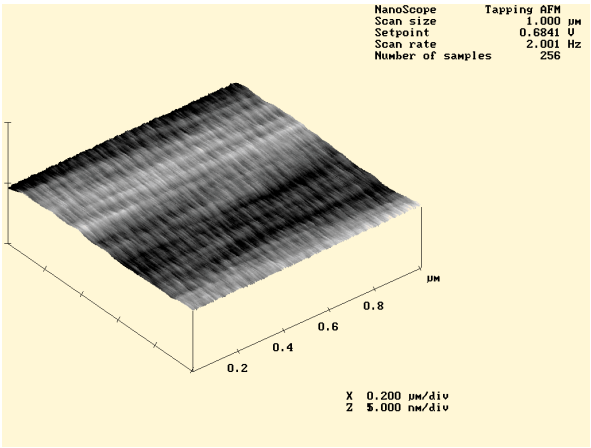
Sponsorship
DARPA

The technology of the formation of SOIAS (Silicon-on-Insulator With Active Substrate) requires us to utilize the lower quality back side surface of the silicon film of the original Separation by IMplantation of OXygen (SIMOX) wafer. Transistor action occurs within a distance of approximately ten nanometers from the top silicon surface. This calls for an investigation and optimization of the surface properties of SOIAS. Novel Chemical Mechanical Polishing (CMP) techniques were used to reduce the surface roughness values to bulk silicon value (1-3 Angstroms) as seen in Figures one and two. Electrical parameters were determined by measuring the interface state density (Dit) using charge pumping, and the dielectric breakdown using Time-Zero BreakDown (TZBD). The effective mobility (meff) has been measured as a function of vertical electric field. Surface characterization was performed using Atomic Force Microscopy (AFM). The relationship between surface roughness and these parameters has been determined by measuring the above electrical parameters on fabricated gated P-i-N diodes and NMOS transistors with different surface roughness.

This work has discovered that the electrical performance of SOIAS is slightly improved by polishing.The mobility has been shown to be capable of matching or exceeding bulk-Si devices. A SOIAS wafer with a 8% smaller roughness than its bulk counterpart has a 9% larger surface mobility at an effective electric field of 0.8 MV / cm. The trend of improving mobility is also found amongst SOIAS wafers themselves as it is found that a 97% reduction in surface roughness leads to a 16% increase in mobility. Moreover, comparing two SOIAS wafers, the roughest and the smoothest, we discover that reducing the roughness by a factor of 92% reduces the interface trap density by 22%. However, the interface trap density could not be reduced to values measured on bulk-Si for SOIAS wafers polished to comparable roughness. However, it was found that polished samples have less on-wafer variation of Dit.



(a)



(b)

Fig. 9a: SOIAS wafer before polish- 2.84 nm-rms.
Fig. 9b: SOIAS wafer after polish- .89 nm-rms.

RF SOI LDMOS Power Devices

Personnel
J. G. Fiorenza (J. A. del Alamo and D. A. Antoniadis)

Sponsorship
SRC

Future cellular and satellite communication networks will be pushed into higher frequency bands by the continually increasing demand for bandwidth. Silicon power amplifiers used in mobile wireless communication devices today cannot effectively operate above 2 GHz. We are studying RF (Radio Frequency) SOI (Silicon-on-Insulator) LDMOS (Laterally Diffused MOS) devices and their potential to push silicon power amplifiers to frequencies that are beyond the limits imposed by bulk silicon technology.

A cross-section of the RF SOI LDMOS device that we have designed is shown in the inset in the figure. The device is a MOSFET that features several enhancements to give it superior RF power performance. The body doping of the device is laterally graded which increases the device's gain at high frequency. The lightly doped n-type drift region, combined with a body contact under the source, increases the device's breakdown voltage and its power handling capability. The insulating buried oxide layer reduces the parasitic drain capacitance and improves its high frequency power gain as well as the isolation between different devices on the same substrate. The device fabrication process has been designed to avoid exotic processing techniques so that it will ultimately be possible to integrate the power device process into a standard digital SOI CMOS process.

Microwave and DC devices have been fabricated and their DC and AC performance was measured. Devices with a 1mm gate length had a current-gain cut-off frequency ft of up to 8 GHz and a off-state breakdown voltage of greater than 20 V. The under-source body contact design proved to be effective, as is demonstrated in the figure. The DC characteristics exhibita high on-state breakdown voltage and do not show any trace of the drain current kink that is characteristic of a floating body device.

Our present results are promising and future research will further improve the device performance. The device design will be thoroughly studied and optimized. The physics of the breakdown of RF SOI power devices will be explored, and a metal gate process will be developed to enhance the RF power performance. We believe that SOI LDMOS devices may have the potential to become a viable technology for future generations of high efficiency, high frequency power amplifiers.

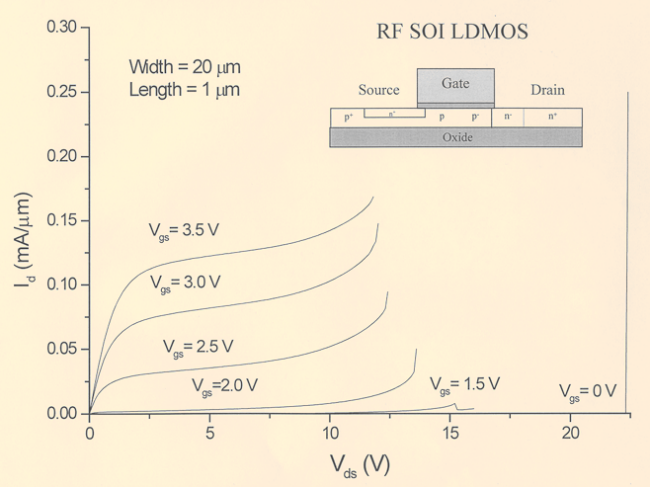


Fig. 10: Device output characteristics

High-density Silicon Substrate Via Technology

Personnel

J. H. Wu (J. A. del Alamo, A. A. Ayon in collaboration with D. A. Antoniadis and M. A. Schmidt)

Sponsorship

SRC

This project pursues the demonstration of a high-density substrate-via technology in silicon. Substrate vias are widely used in the GaAs world to provide low-impedance ground connections for high-power and low-noise devices. In silicon, such a technology could provide low-resistance and low-inductance routing of power and ground supplies for numerous applications such as RF systems, digital logic circuits, and microelectro-mechanical systems. Since IC chip thickness is continually decreasing, this via technology is becoming more feasible as time goes on. This research is motivated specifically by the need for a minimum-impedance ground interconnect for the source of RF power MOSFETs, since source inductance and resistance critically affect large-signal gain and power efficiency. Our broader goal is to explore silicon RF power devices to operate at frequencies of up to 10 GHz. Conventional frontside wiring techniques are problematic at these high frequencies.

In this project, we will develop a substrate via technology for silicon and study the tradeoffs between the performance gains and processing obstacles of these vias. Our target is substrate vias of aspect ratio of 40:1 on 100-mm thick substrates. We will subsequently characterize the resistance, inductance, and high-frequency performance of these vias. The high-aspect ratio vias are etched using a Deep Reactive Ion Etcher (DRIE), which achieves near vertical sidewalls for depths greater than 100 µm. The figure is a SEM photograph of an 84-µm deep, 5-µm wide via etched in silicon using this etcher. The next processing step involves electrodepositing the interconnect metal through the via. This poses the greatest challenge, especially in 100-µm deep vias. We are investigating copper and gold as candidates for the electroplated metal.

Future work on this project could incorporate a liner for the vias as a barrier for the electroplated metal and to enable multiple signals to use the backside for wiring.

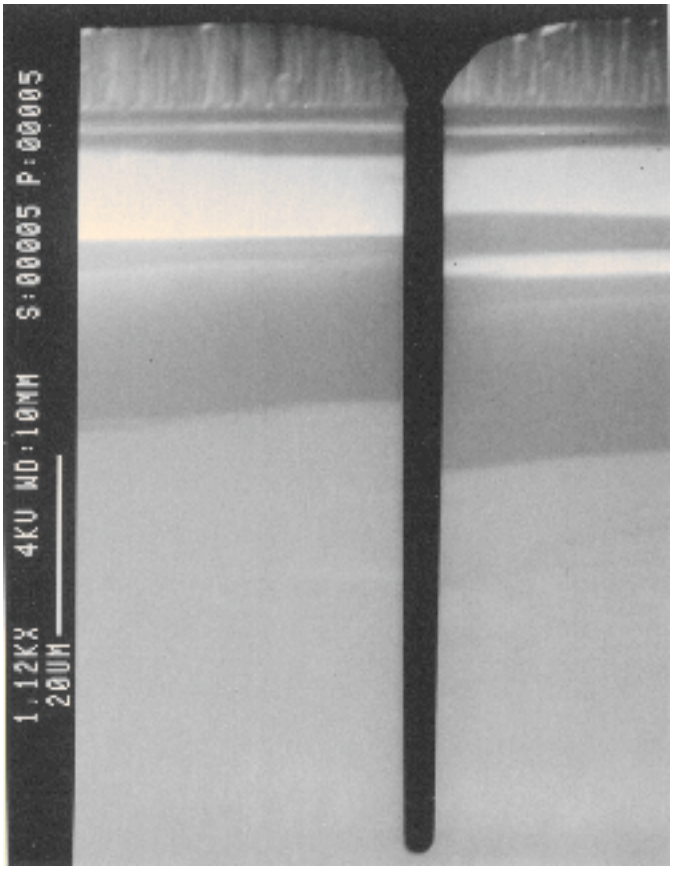


Fig. 11: 84-µm deep, 5-mm wide via etched in silicon using the Deep Reactive Ion Etcher (DRIE)

Hydrogen-induced Piezoelectric Effects in InP HEMTs

Personnel

R. R. Blanchard (J. A. del Alamo)

Sponsorship

Sanders Lockheed Martin, JSEP Fellowship

Hydrogen sensitivity of III-V FETs is a serious and well documented reliability concern. Using the InP High-Electron-Mobility Transistor (HEMT) as a test vehicle, in this work we have found that exposure to hydrogen leads to the formation of titanium hydride in the Ti/Pt/Au gate metallization. This produces compressive stress in the gate, and tensile stress in the underlying semiconductor. Since all compound semiconductors are piezoelectric, this stress induces a volume charge distribution in the transistor. This affects the threshold voltage, and in turn the device characteristics.

To examine the effects of hydrogen exposure, transistors of varying gate lengths and orientations were fabricated in MTL. The devices were exposed to hydrogen through forming-gas (5% H_2 in N_2) anneals performed in a temperature-controlled wafer probe station equipped with a sealed chamber. Room temperature characterizations were done before and after annealing at 200ºC for 3 hours. The change in device threshold voltage, ΔV_T, was used to monitor degradation.

The figure shows the results of this testing. The hydrogen-induced ΔV_T exhibits both gate length, L_G, and orientation dependencies, which are key signatures of the piezoelectric effect. Since all phases of TiH_x have a larger lattice constant than Ti, its formation produces compressive stress in the gate. This stress affects V_T by inducing a piezoelectric charge distribution in the semiconductor. The figure also shows the predicted ΔV_T due to a gate stress of -1.5×10^9 dyn/cm^2 (compressive). The L_G and orientation dependencies of ΔV_T agree well with calculations once we account for a rigid 8 mV offset which we believe arises from H^+ penetration into the semiconductor.

In support of this hypothesis, we have independently confirmed that TiH_x forms under our experimental conditions through Auger Electron Spectroscopy on Ti/Pt test films. In addition, radius-of-curvature measurements have independently confirmed that Ti/Pt films undergo a volume expansion, leading to compressive stress, after exposure to forming-gas. The physical understanding obtained in this work should be instrumental in identifying a device-level solution to this problem.

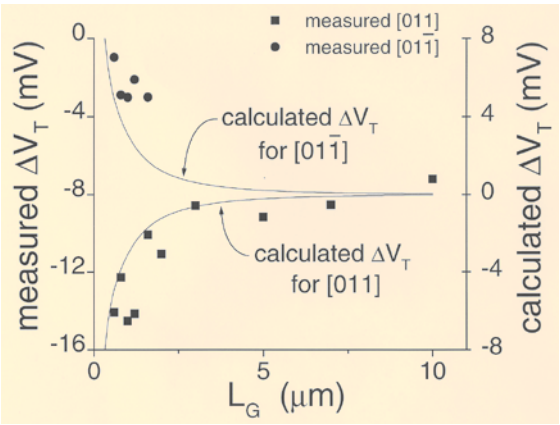


Fig. 12: The change in threshold voltage, ΔV_T, of InP HEMTs after exposure to forming-gas (5% H_2 in N_2) at 200ºC for 3 hours. The L_G and orientation dependencies are key signatures of the piezoelectric effect, and indicate that ΔV_T is in part due to mechanical stress. This stress arises from titanium hydride formation in the Ti/Pt/Au gate. Also shown is the predicted ΔV_T due to a piezoelectric-induced volume charge distribution.

Drain Resistance Degradation in InAlAs/InGaAs Metamorphic HEMTs

Personnel

S. D. Mertens (J.A. del Alamo in collaboration with L.Studebaker and D. D'Avanzo-HP)

Sponsorship

Hewlett Packard

InAlAs/InGaAs High Electron Mobility Transistors (HEMT) hold promise for power-millimeter wave applications. A major reliability concern in some of these devices is the degradation of the drain resistance that is observed when the device is electrically stressed for a long time at bias conditions necessary for power applications. The goal of this project is to find the physical origin of this reliability problem and to suggest solutions to it.

State-of-the-art InAlAs/InGaAs metamorphic HEMTS (mHMETs), provided by our sponsor, Hewlett Packard, were stressed under different bias schemes. It was found that most figures of merit of the device degrade under severe bias stress. In particular, the drain resistance, R_D, has been found to increase significantly. Experiments on mHEMTs have shown that the degradation of R_D is strongly correlated to the amount of impact-ionization during stress.

In order to understand the physical origin of R_D degradation, we have studied the degradation of simpler Transmission Line Model (TLM) structures. These are devices that have exactly the same material structure as the transistors, but no gate has been fabricated, as can be seen on the figure inset. We have found that the low-field resistance, R, of the TLMs degrades significantly at sufficiently high voltage. The figure shows the time evolution of the TLM resistance R, as the bias between the two contacts of the TLM is stepped up at regular time intervals. R is unaffected by bias stress, as long as the voltage is lower than 3.1 V. At this voltage, there is an initial period where degradation is very slow, after 100 minutes, the degradation rate suddenly increases. The degradation seems to saturate then, until the bias is stepped up to 3.4 V, at which bias the degradation rate suddenly increases again. If the bias is stepped up to 3.7 V the device becomes critically damaged.

This result suggests that there might be two different degradation mechanisms at play. One of the degradation mechanisms is likely to be recombination enhanced growth of some kind of defect. Impact-ionization generated holes recombine with electrons, releasing energy to the lattice and thereby aiding the growth of defects. These cause the resistance to increase, as these defects can act as traps and decrease the sheet carrier concentration in the channel. Additional experiments are being performed to narrow down the physical location of defect formation.

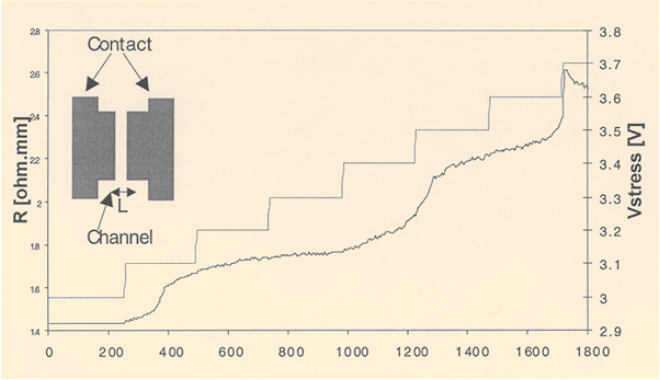


Fig.13: Time evolution of low-field resistance of a TLM with a 12 μm long channel. The TLM is stressed at a bias V_{stress} that is stepped up from 3 to 3.7 V in 0.1 V intervals.

A Dynamic Model for the Kink Effect in InAlAs/InGaAs High-Electron Mobility Transistors

Personnel

M. Somerville (J. A. del Alamo)

Sponsorship

JSEP, JSEP Fellowship, Lockheed Martin

InAlAs/InGaAs high-electron mobility transistors (HEMTs) are devices of great interest for millimeter-wave applications. The kink effect is a prominent anomaly in the output characteristics of these devices that results in reduced gain and excess noise at high frequencies. There is a great deal of interest in understanding the physics of the kink with the goal of eliminating it or, at least, with the goal of accurately modeling it so that circuit operation takes full account of it.

In the last few years, we have been carrying out a systematic experimental study of the kink-effect in InAlAs/InGaAs HEMTs that has involved detailed DC characterization, sidegate measurements, large-signal transient measurements with nanosecond resolution, and ligh-sensitivity measurements. This work has allowed us to develop the first physical model for the dynamics of the kink. This work has resulted in a complete equivalent circuit model that fully accounts for the dynamics of the kink down to the nanosecond range.

Our experimental work has revealed that the kink arises from the generation of holes by impact-ionization and their subsequent accumulation in the extrinsic source, the cap layer above the extrinsic source, and the buffer layer underneath the extrinsic source. This hole accumulation results in a reduction in source resistance and a shift in the threshold voltage of the device. This physical picture suggests that the dynamics of the kink are dominated by the transfer of holes from the extrinsic source to the cap layer and to the buffer layer. This understanding has allowed us to propose a simple phenomenological formulation for the kink effect that is ameanable to an equivalent circuit model representation.

This formulation does an excellent job of describing the dynamics of the kink. In pulsed measurements of InAlAs/InGaAs HEMTs fabricated at MIT, we found that the kink emerges a few nanoseconds after the device has been turned on. We also found that the kink appears first at high values of drain-to-source voltage. The model does a good job in describing the entire dynamic behavior of the kink down to the nanosecond range (see figure).

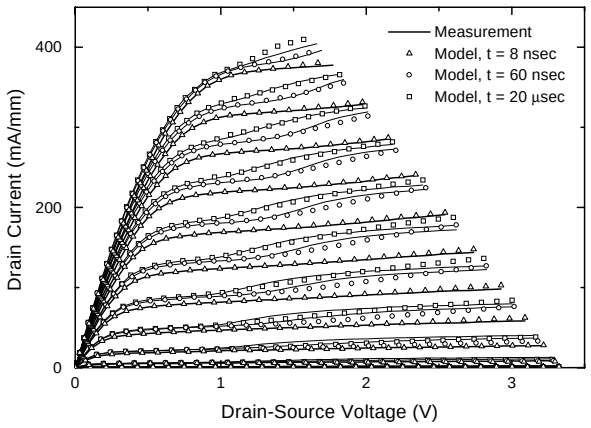


Fig. 14: Pulsed I-V characteristics of InAlAs/InGaAs HEMTs fabricated at MIT at three different times after the device is turned on. Also graphed are the predictions of a new equivalent circuit model of the kink.

Silicon Field Emitter Arrays Integrated With MOSFET Devices

Personnel

C-Y. Hong (A. I. Akinwande)

Sponsorship

DARPA

Si field emitter arrays are being investigated as electron sources for field emission displays; however, as with other field emitter arrays, they are susceptible to current instability and non-uniformity caused by structural and work function variations of the tip. The simplest way to improve uniformity is to introduce a highly resistive film between the emitter tips and the substrate to act as a negative feedback resistor. However, this approach leads to excessive power dissipation and lowered device transconductance.

Studies of the emission characteristics of p-type and p-n junction silicon FEAs suggest that the emission current is controlled by the current flow in the substrate and an inversion layer was formed under the extraction gate. This notion can be extended to the MOSFET/FEA in which the current emitted by the FEA is controlled by current flowing through the channel of the MOSFET. However, this FEAs requires high voltages while the MOSFET requires low voltages, leading to breakdown of the MOSFET. Using a LDMOSFET/FEA device structure can solve this problem. We are fabricating MOSFET/FEAs that have a relatively simple structure in which the n-Si FEA tip is also the drain of the n-MOSFET. This device eliminates the current non-uniformity and instability because the current is controlled by the MOSFET.

A seven masks set has been designed to fabricate the integrated Si FEA with MOSFET device. The MOSFET has light doping at the drain to improve its breakdown voltage because the MOSFET must be able to withstand the gate voltage of a field emitter. One optional mask is used to make the oxide thinner under the MOSFET gate but not all the FEA gate to meet the breakdown requirement. Different length/width ratio MOSFETs have been designed to connect with the different number of Si tips in series to reach the optimum performance. The device structure has been simulated using process and device simulation tools. The process adapts oxidation sharpening for making sharp Si tips, CMP for defining the poly-Si gate, etc. The MOSFET structure is fabricated with FEA simultaneously.

Vertical MOSFET / Field Emitter Array Technology

Personnel

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DARPA

As the pixel density of high-resolution electronic display increases, there is a corresponding increase in the I/O data transfer rate necessary to address the display. This ultimately reduces the row access time on the display for a fixed scanning refresh rate. To alleviate this problem, active matrix addressing is used in current display technologies. However, the I/O data transfer rate is still very high and leads to large power dissipation in the addressing circuits and system drivers.

A proposed solution to this issue is the use of intelligent pixel arrays whereby an actively addressed pixel retains on/off information within the pixel between frame scans. This reduces the necessary refresh rate if the actively on or off pixel state does not need to be modified on the subsequent picture frame. We are proposing to construct a field emitter array with an integrated transistor structure to form the basis of a pixel latch subsystem. Using an additional transistor to isolate the pixel latch element from the display row and column address lines, random addressing of each pixel latch element is possible. An additional benefit of an integrated transistor structure is stabilization of field emission current from the emitter arrays (FEA).

Using an integrated transistor structure, it is possible to modulate the field emission current density by adjusting the vertical MOSFET (VMOS) gate voltage. Because the VMOS is connected in series with the field emitter array the gate voltage of the FEA is divided between the drain to source voltage, V_{DS}, and the gate to emitter voltage, V_{GE}, of the FEA. This can be modeled as a voltage controlled current source with a floating drain voltage for the VMOS device. The floating drain voltage is then controlled such that the desired level of emission current is produced. A simplified VMOS/FEA schematic is shown in Figure 15.

Other approaches that have been proposed for MOSFET/FEA structures have used lateral MOSFET designs integrated with field emitter arrays. While this is a very good device structure, higher packing density and thereby greater display resolution can be achieved with a vertically integrated MOSFET/FEA device. A candidate device structure is a combined MOSFET and field emitter structure.

Initial investigation into VMOS simulation and fabrication has been completed and appears feasible. The initial process design will use vertically etched silicon pillars to create the VMOS structure for testing and analysis. Figure 16 and 17 show process simulation results and etched Si pillar arrays as the first process steps.

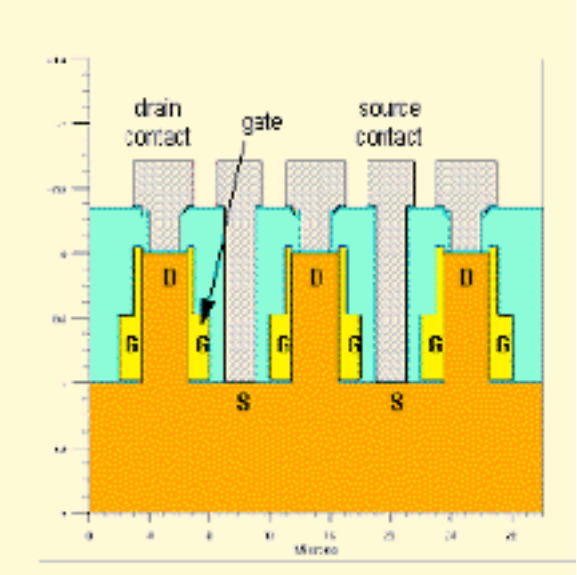

Fig. 16: VMOS Process simulation

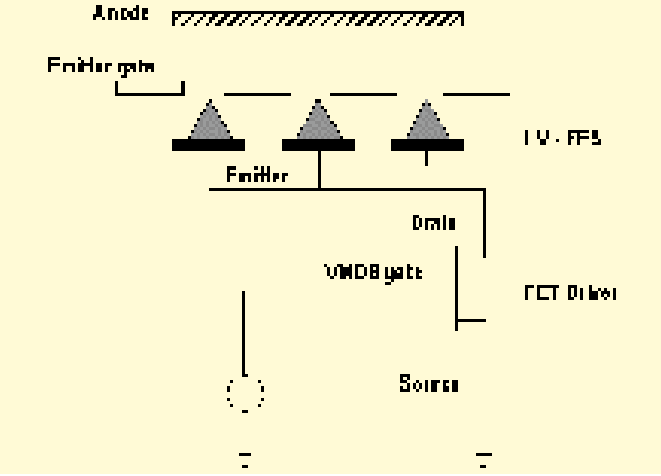

Fig. 15: MOSFET/FEA Schematic

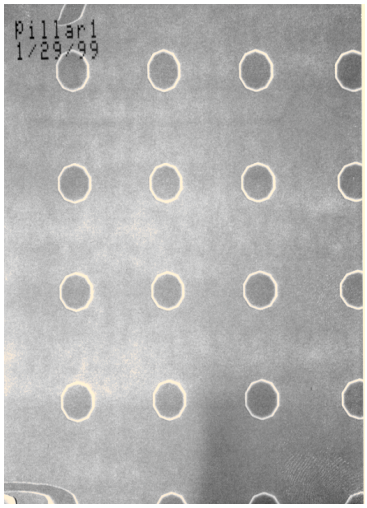

Fig. 17: Vertically etched Si pillar arrays (top view)

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Low-Power Driver Circuit for Organic Light-Emitting Diode Displays

Personnel

V. M. Joyner (A. I. Akinwande)

Sponsorship

DARPA

Organic Light-Emitting Diode (OLED) devices offer a very promising alternative to existing flat panel display technologies, such as Liquid Crystal Displays (LCD) that currently dominate the market. OLED displays offer very attractive characteristics, including higher luminous, larger viewing angle, and low-power consumption, over the established LCD technology. The current burst of technological advances as the result of world-wide research endeavors to increase the performance of these devices has created a myriad of exciting new opportunities for OLEDs in the flat-panel display market.

One major concern associated with implementing OLED displays is establishing the most power efficient means of addressing the display. OLED displays are emissive in nature and the luminance of OLED is controlled by the flow of current through an organic material. The display consists of a matrix of pixels, similar to most displays, addressed by driver and control circuitry. For most existing flat panel technologies, pixel addressing and controlling the flow of data from the external system to the display panel can consume up to one third of the overall power consumed by the display. Therefore, there are considerable savings if the power consumed by the addressing electronics is reduced.

There are several factors that must be considered in order to design low-power driver circuitry for OLED displays, that provide high luminance and gray scale capabilities. For miniature devices, displaying images that are nearly static, incorporating a mechanism for storing data at each pixel can reduce the power consumption considerably and increase brightness.

The primary goal of this research project is to implement a low-power display driver circuit for an OLED display. The implementation will be chosen based on the outcome of a feasibility study aimed at investigating the various options available for addressing the display and the design requirements imposed by the operation of the OLED. There are four primary design options to be considered: (a) passive matrix addressing with sequentially addressed rows/columns, (b) active matrix addressing with sequentially addressed rows/columns and dynamic storage at each pixel, (c) active matrix addressing with sequentially addressed rows/columns and static storage at each pixel, and (d) active matrix addressing with randomly addressed rows/columns and static storage at each pixel. Each implementation is compared in terms of the overall power consumed in driving the high capacitance row and column lines in the display matrix and reduction of I/O data rate.

The fourth implementation was chosen for several reasons. In this approach the display data is stored at each pixel using a static RAM latch and the array is addressed in a manner similar to a conventional memory circuit. In most existing flat panel technologies, each pixel is addressed every frame. However, in this implementation each pixel is only addressed when its data has changed, and therefore, unnecessary driving of the high capacitance row and column lines is eliminated. Each pixel is divided into 3 subpixels, one for each of the three primary colors: Red, Green, and Blue.

Micromachined SIS Millimeter-Wave Focal-Plane Arrays

Personnel

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Sponsorship

NSF, NASA

SIS (superconductor-insulator-superconductor) heterodyne receivers have been demonstrated to be the most sensitive receivers throughout 30-840 GHz frequency range. The challenge now in the SIS receiver technology is to develop focal-plane arrays to improve the efficiency of data acquisition. In order to achieve these goals, we are currently developing a novel scheme to couple the millimeter-wave and infrared signals to the
Following our recent success in developing single-superconducting devices by using a micromachined horn antenna and a planar antenna supported by a thin (~1 micron) membrane, as shown in Fig. 18(a). As stated in the introduction, this novel micromachined antenna structure can be produced with a high precision using photolithography, and it can be utilized in focal-plane arrays, as shown in Fig. 18(b).

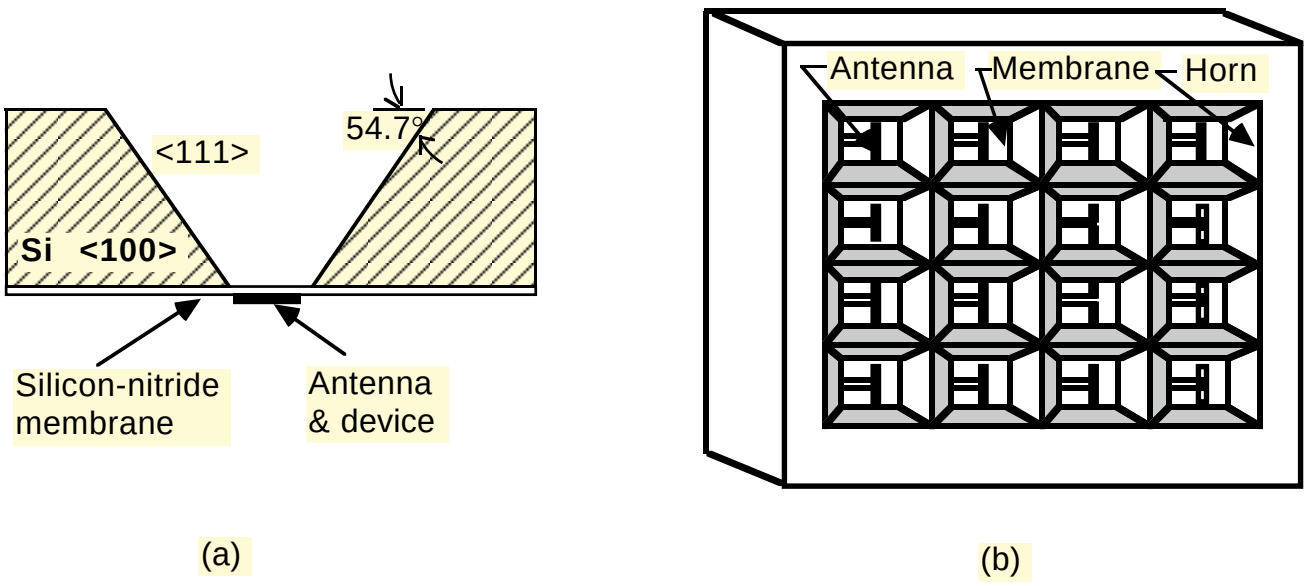

Fig. 18: (a) Example of a micromachined horn antenna structure that is made by anisotropically etching a <100> silicon wafer. (b) Schematic of a focal-plane array on a single wafer made using micromachining.

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Following our recent success in developing single-element micromachined SIS receivers (see our previous publication in Appl. Phys. Lett. 68, 1862 (1996)), we have designed and constructed a 3x3 focal-plane array with the center frequency around 200 GHz. The schematic of the structure is shown in Fig. 19, which includes a micromachined and mechanically machined horn array, the device wafer, and the dc and IF connection board. Measurements of the dc I-V characteristics showed good uniformity across the entire array. A heterodyne measurement on the central element yielded the best result. The minimum uncorrected receiver noise temperature is 52 K DSB, measured at a bath temperature of 2.7 K. This noise temperature is comparable to the best results obtained in (tunable) waveguide mixers.

The measured noise temperatures as functions of the LO frequency for all the 9 elements of another array are shown in Fig. 20. In this array the minimum noise temperature of the central element is 62 K (illustrated in the inset). The measured noise temperature of the different elements is fairly uniform, with minimum noise temperatures for all the nine elements ranging from 62 to 101 K. The 3-dB noise bandwidth of all the 9 elements has a uniform value of 30 GHz across the array. We attribute the slight difference in the noise temperatures to the effect of the limited size of our dewar window and the thick lens inside the dewar. Measurements of several arrays always showed the lowest noise temperature for the central element. The DSB noise temperatures of the current state-of-the-art waveguide receivers for the 230 GHz astronomy band are in the range of 35-50 K. With a further optimization of the junction device characteristics and a reduction of the junction area, the micromachined SIS mixer arrays could yield comparable noise temperature for each array element. Furthermore, the scalability of the machined and micromachined sections could extend the operating frequencies of the micromachined focal-plane imaging arrays up to 1 THz.

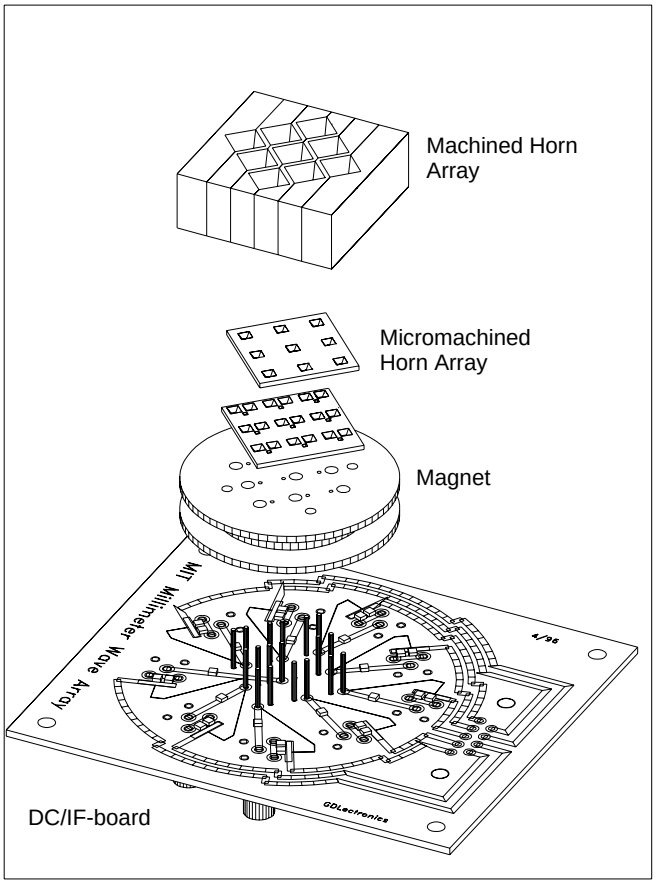

Fig. 19: (a) Schematic of an array structure including a micromachined and machined horn array, the device wafer, and the dc and IF connection board. (b) I-V curves of seven SIS junctions in the array.

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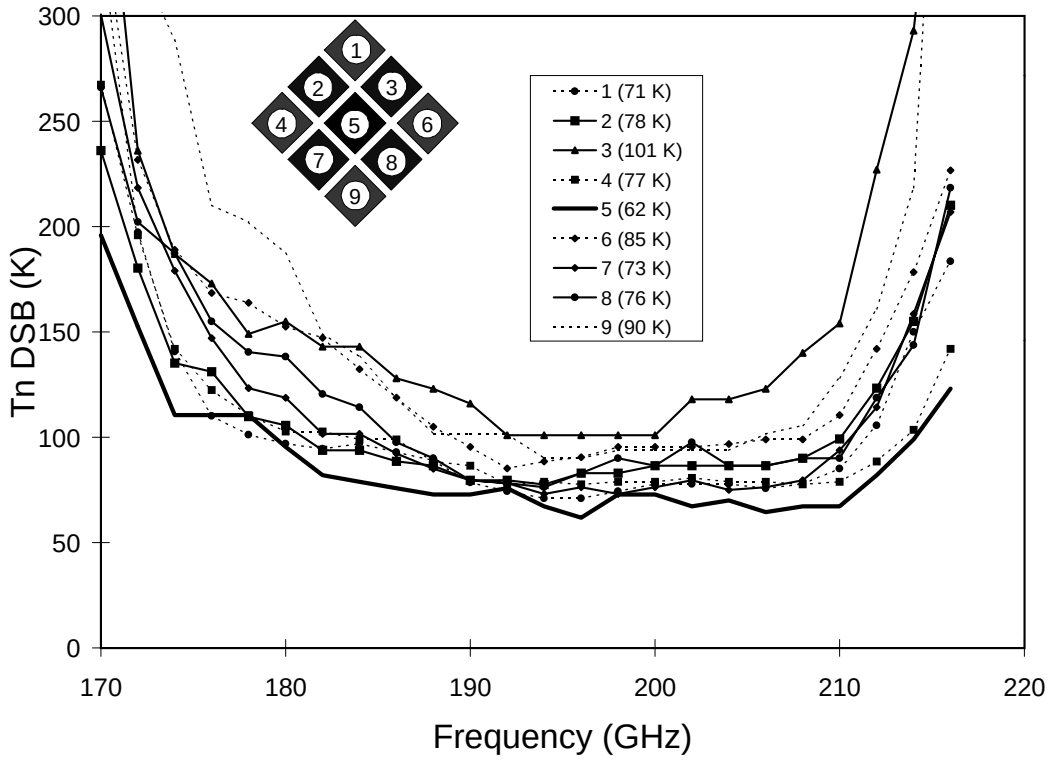

Fig. 20: Measured DSB noise temperatures of all the nine elements in the array. The inset shows the minimum noise temperature for each individual element.

Fabrication of Large Area Nanomagnet Arrays for Ultra High Density Magnetic Data Storage

Personnel

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Sponsorship

NSF, DARPA

The magnetic information storage density of hard drives has increased at the amazing rate of 60% per year for the last 8 years. This growth is being achieved through evolutionary means involving scaling and improvement in all components of a hard drive: the head design, the signal processing, the media, etc. However, as the bits in the conventional thin film medium continue to decrease in size, thermal energy threatens to switch the individual grains that make up the bit, resulting in a loss of signal. There is wide agreement that a storage medium based on discrete, single-domain particles with uniform magnetization (Figure 21) may be scaled two orders-of-magnitude beyond the physical limits of conventional media.

We have initiated a program to develop fabrication techniques to generate high-density arrays of magnetic nano-particles, and investigate their applicability to data storage. Our goal is to explore the effects of particle size, shape, inter-particle spacing, and material composition on magnetization reversal, thermal stability, and particle interactions; and to realize the necessary densities via fabrication techniques that are compatible with low-cost manufacturing. To the latter end, we take advantage of the high resolution capabilities of our interferometric lithography systems to define the 2-dimensional pattern for such particles. To determine the effect of physical parameters such as particle size, shape, and material composition, we have developed process sequences for the fabrication of particles that fit into three general categories (Figure 23a) particles formed by electrodepostion, b) particles formed by evaporation, and c) particles formed by etching. Electrodeposition involves forming a pattern of holes in a photoresist and transferring this pattern into an antireflection coating (ARC) polymer plating template. This method allows us to form high-aspect-ratio structures and thus to study the effect of shape anisotropy on magnetic behavior. Figure 22a is a scanning electron micrograph of 100 nm-period, electrodeposited Ni pillars. The magnetization curves obtained by vibrating-sample magnetometry (Figure 22b) suggest that the pillars favor out-of-plane magnetization. Magnetic force microscopy performed on these pillars (Figure 24b) confirms perpendicular magnetization as illustrated in Figure 21. With a switching field of 700 Oe, these particles may be well suited for data storage. The second process sequence (Figure 23b) entails the evaporation of pyramids of ferromagnet into holes in a polymer, followed by liftoff of the template. Evaporated Ni pyramids of 100 nm-period (Figure 25a) are small enough to exhibit unstable magnetization at room temperature. However, at 10 K, they too favor out-of-plane magnetization (Figure 25b). The third process (Figure 23c) allows us to pattern thin films that have properties desirable for data storage. Using ARC posts as an etch mask, and ion milling as an etching technique, one can pattern a thin film into islands of magnetic material, as shown in Figure 26.

In addition to patterned media, structures such as Figure 26 also have applications in MRAM (magnetic random access memory) devices. In an MRAM, data are stored into, and read from small magnetic particles using the magnetoresistive effect, in which the resistance of the magnetic particle depends on its magnetization state. We are etching 'spin valve' multilayer magnetic stacks into dots to evaluate their magnetoresistive properties.

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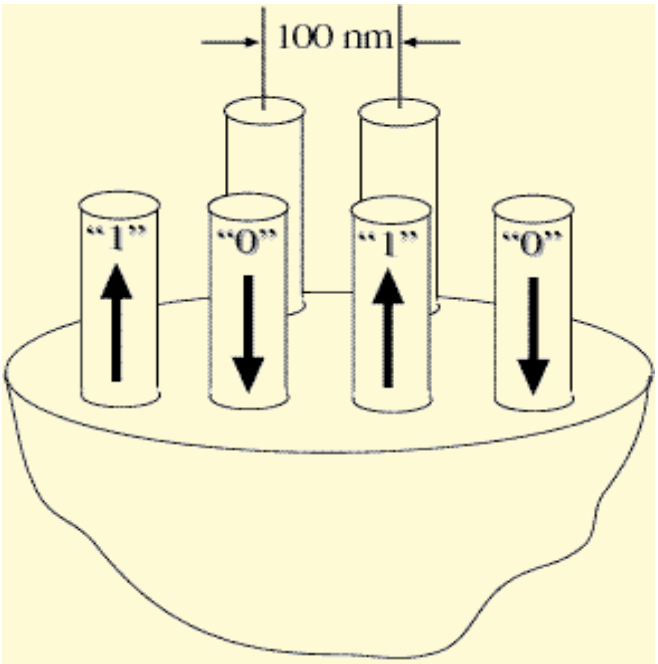

Fig. 21: Schematic of high density magnetic information storage based on sub-100 nm sized magnetic particles.

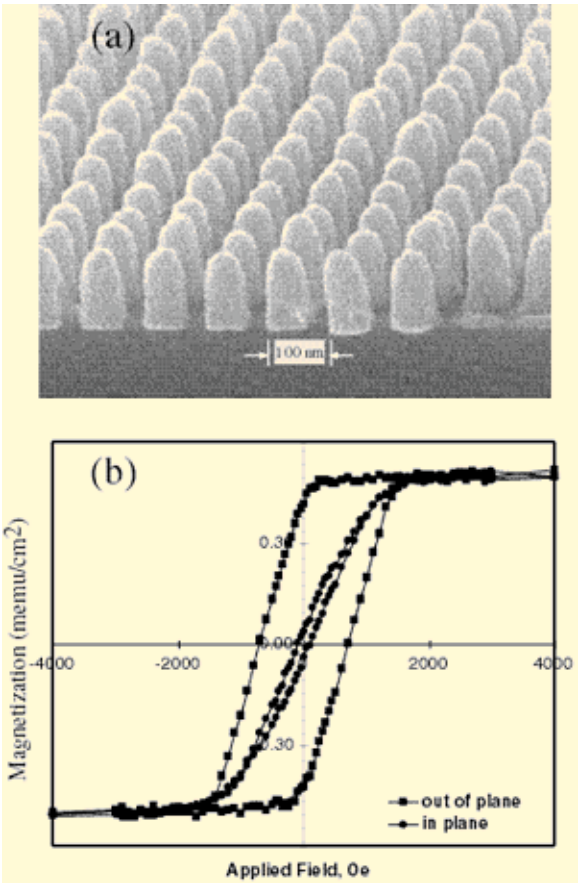

Fig. 22a: An electron micrograph of 100 nm-period Ni pillars after the removal of the ARC plating template. Figure 22b is a plot of the magnetization of the pillars vs. a magnetic field applied in-plane (dots) and out-of-plane (squares). The large magnetization at remanence (applied field = 0) for the out-of-plane compared to the in-plane applied field indicates that out-of-plane magnetization is favored.

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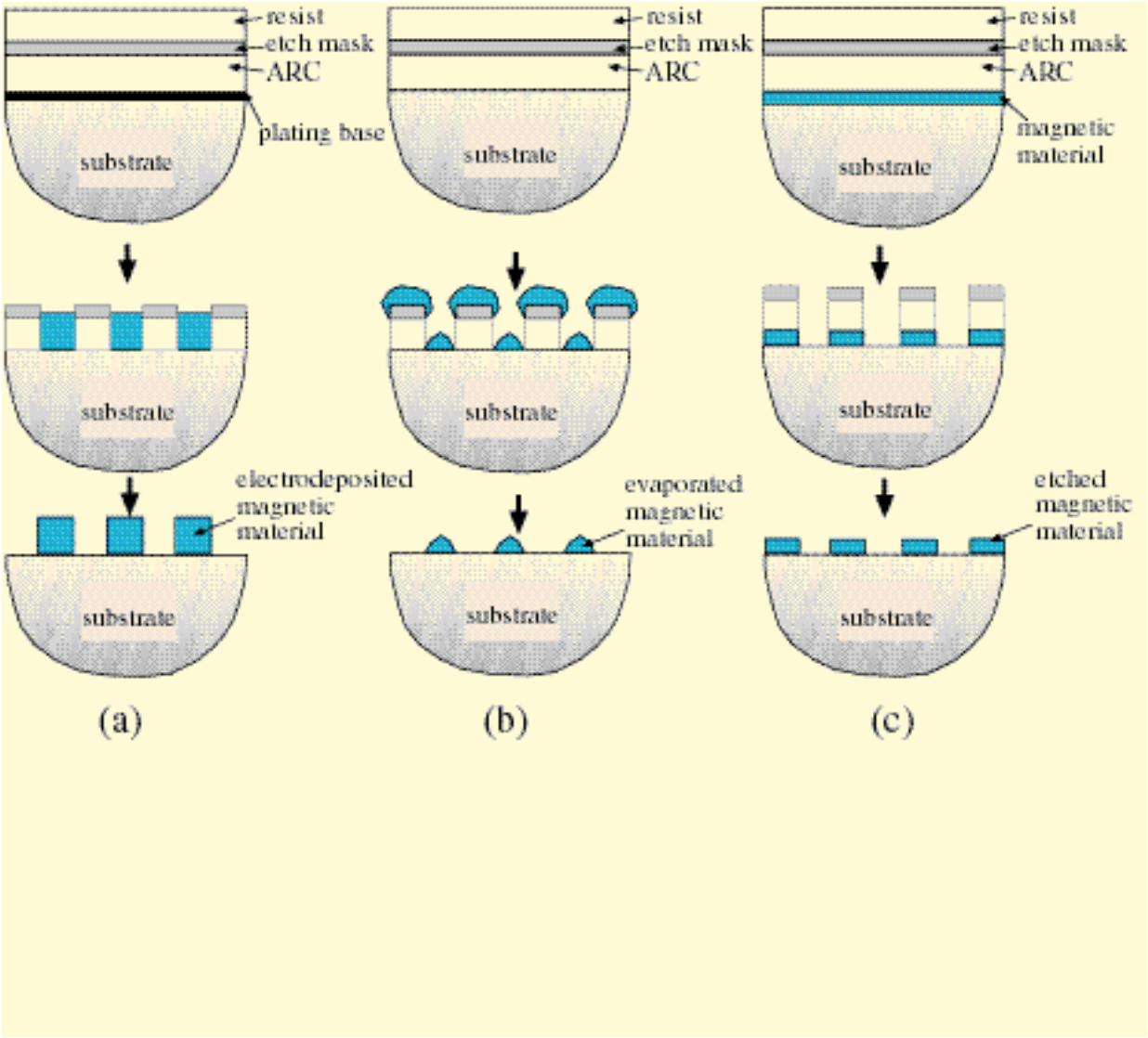

Fig. 23: Schematic of three process sequences developed for the investigation of magnetic nano-particles with a variety of physical parameters. Lithographic exposure is by interferometric lithography or achromatic interferometric lithography. The antireflection coating (ARC) prevents backreflections from the substrate from interfering with the lithography. Sequence (a) illustrates the process of fabricating high aspect ratio magnetic pillars via electroplating. Sequence (b) involves the deposition of magnetic pyramids via evaporation and lift-off. Sequence (c) is appropriate for patterning magnetic islands in predeposited thin films.

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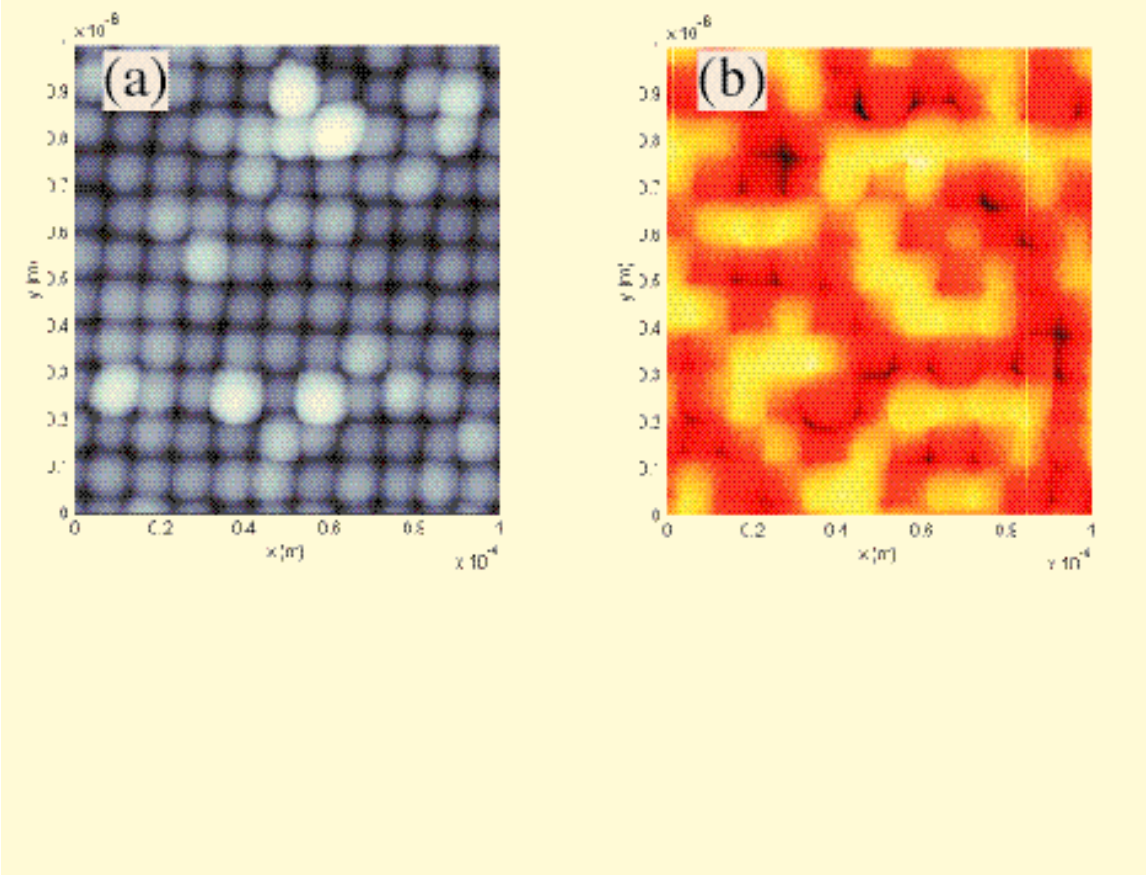
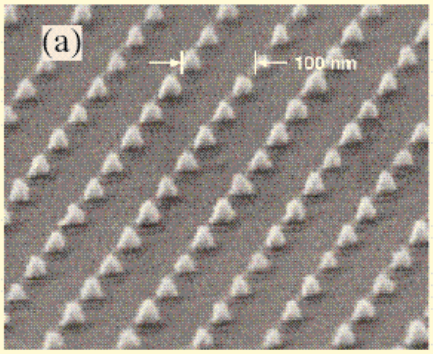


Fig. 24a: Topography plot of the electroplated Ni pillars obtained by scanning the pillars with the tip of a magnetic force microscope and recording tip deflections. Figure 24b is the corresponding magnetic-force plot where the light regions indicate "up" magnetization and the dark regions indicate "down" magnetization.



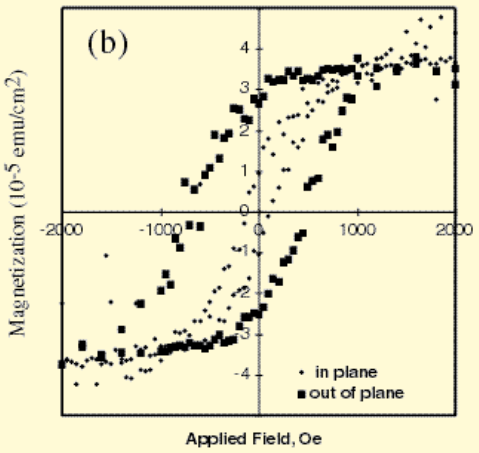


Fig. 25a: Evaporated NiCr pyramids after lift-off. (b) In-plane (dots) and out-of-plane (squares) magnetization curves obtained by Superconducting Quantum Interference Device (SQUID) magnetometery at 10 K of a similar Ni sample. Such pyramids, whose magnetization is unstable at room temperature, also favor out-of plane magnetization at 10 K.

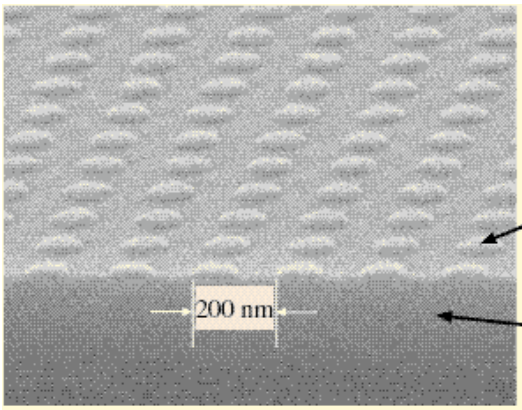


Fig. 26: 200 nm-period islands of Cu/Co multilayers, patterned by interferometric lithography and ion milling, are suitable for magnetic random access memory (MRAM) applications.