Efficient 3-D Interconnect Analysis

Personnel

I. Balk, M. Chou, M. Kamon, Y. Massoud, V. Nadkarni, J. Phillips, and J. Tausch
(J. White)

Sponsorship

ARPA, SRC, IBM, and Harris Semiconductor

We have developed multipole-accelerated algorithms for computing capacitances and inductances of complicated 3-D geometries, and have implemented these algorithms in the programs FASTCAP and FASTHENRY. The methods are accelerations of the boundary-element or method-of-moments techniques for solving the integral equations associated with the multiconductor capacitance or inductance extraction problem. Boundary-element methods become slow when a large number of elements are used because they lead to dense matrix problems which are typically solved with some form of Gaussian elimination. This implies that the computation grows as n^3, where n is the number of panels or tiles needed to accurately discretize the conductor surface charges. Our new algorithms, which use Krylov subspace iterative algorithms with a multipole approximation to compute the iterates, reduces the complexity so that accurate multiconductor capacitance and inductance calculations grow nearly as n m where m is the number of conductors. For practical problems which require as many as 10,000 panels or filaments, FASTCAP and FASTHENRY are more than two orders of magnitude faster than standard boundary-element based programs. Manuals and source code for FASTCAP and FASTHENRY are available directly from MIT.

In more recent work, we have been developing an alternative to the fast-multipole approach to potential calculation. The new approach uses an approximate representation of charge density by point charges lying on a uniform grid instead of by multipole expansions. For engineering accuracies, the grid-charge representation has been shown to be a more efficient charge representation than the multipole expansions. Numerical experiments on a variety of engineering examples arising indicate that algorithms based on the resulting "precorrected-FFT" method are comparable in computational efficiency to multipole-accelerated iterative schemes, and superior in terms of memory utilization. The precorrected-FFT method has another significant advantage over the multipole-based schemes, in that it can be easily generalized to some other common kernels. Preliminary results indicate that the precorrected-FFT method can easily incorporate kernels arising from the problem of capacitance extraction in layered media. More importantly, problems with a Helmholtz equation kernel have be solved at moderate frequencies with only a modest increase in computational resources over the zero-frequency case. An algorithm based on the precorrected-FFT method which efficiently solves the Helmholtz equation could form the basis for a rapid yet accurate full-wave electromagnetic analysis tool.

Our latest work has been on extending the applicability of precorrected-FFT and fast multipole schemes. We have combined these fast techniques with new numerically stable integral formulations for problems in electroquasistatics (distributed RC) and for problems with high dielectric permitivity ratios. In addition, we have extended the algorithms in FASTHENRY to include finite substrate conductivity and used it to analyze on-chip inductance. We have also developed parallel versions of the precorrected-FFT algorithm, as well as preconditioners which improve the convergence of the iterative solver used in FASTHENRY.

Reduced-order modeling techniques are now commonly used to efficiently simulate circuits combined with interconnect. Generating reduced-order models from realistic 3-D structures, however has received less attention. Recently we have been studying an accurate approach to using the iterative method in the 3-D magnetoquasistatic analysis program FASTHENRY to compute reduced-order models of frequency-dependent inductance matrices associated with complicated 3-D structures. This method, based on a Krylov-subspace technique, namely the Arnoldi iteration, reformulates the system of linear ODE's resulting from the FASTHENRY

continued

equation into a state-space form and directly produces a reduced-order model in state-space form. The key advantage of this method is that it is no more expensive than computing the inductance matrix at a single frequency. The method compares well with the standard Pade approaches and may present some advantages because in the Arnoldi-based algorithm, each set of iterations produces an entire column of the inductance matrix rather than a single entry, and if matrix-vector product costs dominate then the Arnoldi-based algorithm produces a better approximation for a given amount of work. Finally, we have shown that the Arnoldi method generates guaranteed stable reduced order models, even for RLC problems.

Our recent work has focused on fast techniques of model reduction which automatically generate low order models of the interconnect directly from the discretized Maxwell's equations under the quasistatic assumption. When combined with fast potential solvers, the overall algorithm efficiently generates accurate models suitable for coupled circuit-interconnect simulation.

The design of single chip mixed-signal systems which combine both analog and digital functional blocks on a common substrate is now an active area of research, driven by the relentless quest for high-level integration and cost reduction. A major challenge for mixed-signal design tools is the accurate modeling of the parasitic noise coupling through the common substrate between the high-speed digital and high-precision analog components. We are working on a sparsification method based on eigendecomposition which handles edge effects more accurately than previously applied multipole expansion techniques, and then combine the sparsification approach with a multigrid iterative method which converges more rapidly than previously applied Krylov-subspace methods. Results on realistic examples demonstrate that the combined approach is up to an order of magnitude faster than the sparsification plus a Krylov-subspace method, and orders of magnitude faster than not using sparsification at all. ❑

Simulation of Electromigration-Induced Failure of IC Interconnects

Personnel

V. Andleigh, W. Fayad, S. Riege, and Y.-J. Park
(C. V. Thompson)

Sponsorship

SRC and DARPA

We have developed a tool for simulation of post-patterning grain structure evolution in polycrystalline metallic interconnects, GGSim. We have used this tool to predict the statistical characteristics of the grain structures which affect the reliability of interconnects as a function of the interconnect dimensions, and as a function of the thermal history of the interconnects. We find that the polygranular and bamboo clusters in near-bamboo interconnects have length distributions which are well fit by Weibull distribution functions, for a broad range of line widths and thermal histories. The average polygranular cluster length decreases and the average bamboo cluster length increases with decreasing line width and with increasing thermally induced post-patterning grain structure evolution. The results of these simulations are embodied in a tool called Cluster, which is available at http://web.mit.edu/cthomp/www. We have also modified GGSim to allow simulation of post-patterning grain structure evolution in interconnects with arbitrary shapes. This modified tool can be used in conjunction with layout tools to predict the intrinsic variability of grain structures in specific interconnect layouts, both for as-patterned interconnects and as a function of specific thermal histories of the interconnect structures.

We have also developed a software tool for structure-sensitive simulation of electromigration and electromigration-induced failure of interconnects. A web-based version of this tool, MIT/EmSim, can be accessed at http://nirvana.mit.edu/emsim. The tool generates grain structures with appropriate statistical variations as a function of median grain size and line width, and predicts failure statistics as a function of the failure criteria, of the current density and of the temperature. MIT/EmSim allows the user to study failures based on void nucleation, void growth, and compressive failures. The effects of wide-to-narrow transitions, junctions, and thermal history have also been included in the internal version of MIT/EmSim (not available on the web), and are now being tested through comparisons with experiments. The current version of MIT/EmSim has been developed for use in analysis of the process-sensitivity of the reliability of Al and Al-Cu interconnects, as well as for use in making more accurate extrapolation of test data for calculation of in-service reliabilities than can be made using conventional methods. We are currently modifying MIT/EmSim for process and structure-sensitive simulations of electromigration in pure Cu. ❑

Modeling of Advanced Device Structures

Personnel

Z. K. Lee and K. Jackson
(D. A. Antoniadis and M. B. McIlrath)

Sponsorship

DARPA

As MOSFET dimensions are reduced to the submicron level, the electrical performance is critically dependent on the two-dimensional (2D) distribution of dopant concentrations in the semiconductor. In order to accurately characterize, predict, and control the diffusion characteristics of dopants, and therefore the device electrical characteristics, it is essential that the 2D doping profile be accurately known. Moreover, knowledge of an accurate 2D doping profile enables one to calibrate mobility models for the inversion channel of MOSFETs, making accurate simulations of device performance possible.

However, the lack of a mature 2D doping profiling technique has been an obstacle in achieving such goals. Here, we have demonstrated a new, comprehensive technique for the extraction of 2D doping profiles in submicron MOSFETs by inverse modeling using subthreshold I-V characteristics. The main advantages of this technique include: (1) ability to extract 2D doping profile (including channel length) of very small devices (down to sub-100 nm) due to the technique's immunity to parasitic capacitance, resistance, and noise; (2) no special test structures needed since only subthreshold I-V data are used; (3) non-destructive; (4) low sensitivity to gate electrode area variations; (5) low dependence on mobility and mobility models; and (6) simplicity of data collection and preparation, as well as general ease of use.

We have demonstrated the application of the technique using the Super-Steep Retrograde (SSR) devices fabricated at MIT. The extracted profile of a 0.1 μm effective channel length device is shown in Figure 1. We have also demonstrated the accurate device performance prediction capability that is possible with this technique, once appropriate mobility models have been calibrated using the extracted 2D profiles. Figure 2 shows a comparison between the measured and predicted I-V characteristics of a 0.15 μm channel length device having a "step" channel doping profile. The potential of the technique is clearly demonstrated. ❑

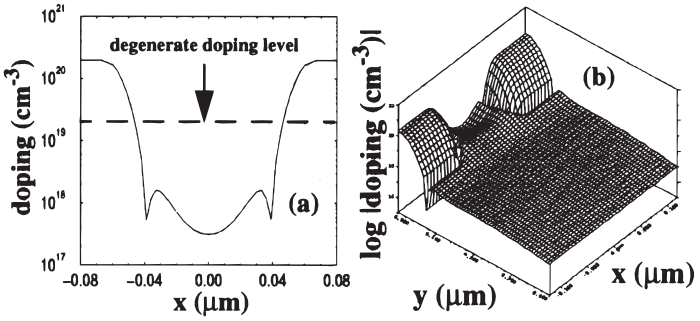

Fig. 1: Extracted (a) lateral and (b) 2D doping profile of a SSR device having source/drain halo dopings. The device has L_{gate} = 0.1 μm, T_{ox}= 50 A, and W = 10 μm.

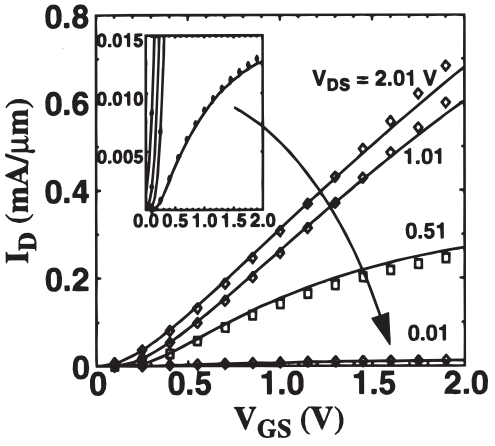

Fig. 2: Comparison between measured and predicted I-V characteristics using calibrated mobility models. The device has a "step" channel doping profile with L_{gate} = 0.15 μm, T_{ox} = 50 A, and W = 10 μm. Simulated data are denoted by symbols.

A Low Temperature Perspective on MOSFET Scaling

Personnel

K. M. Jackson
(J. Chung, and D. Antoniadis)

Sponsorship

DARPA (NSF Fellowship)

Lower temperature operation of devices has long been viewed as a way to extract the ultimate performance out of a given gate length device. Lowering the temperature increases the low-field mobility and saturation velocity, which significantly increase the drive current of the device. This project, however, views temperature as another knob to be turned in the overall optimization of a MOSFET design. The work so far on the project has focused on using a physically based analytical model for a uniformly doped MOSFET that allows one to explore the design space of a deep submicron MOSFET. The results of this modeling suggest that lower temperature operation is one way to realize the full performance gains promised by the continued scaling of the MOSFET.

Scaling a MOSFET requires reducing its channel length, which results in faster switching speeds from increased drive currents and/or reduced capacitance. Scaling the channel length requires the gate oxide thickness (t_{ox}) to decrease and channel doping to increase to meet the constraints of being able to turn the device off to a set leakage level. The electric field across the gate oxide is limited by reliability concerns, thus the power supply voltage (V_{dd}) has to scale at a similar rate as t_{ox}. From a device performance perspective, the V_{dd}/V_{th} ratio should remain the same (or increase) as L is scaled. However, because the rate at which the device turns off (the inverse subthreshold slope) does not scale, at an 80° C operating temperature (normal for a microprocessor) V_{th} is constrained to above about 0.4 V for an off current leakage (current with 0 V on the gate) of 1×10^{-9}A/um.

Lowering temperature steepens the inverse subthreshold slope ($\propto$ T) thus allowing a lower threshold voltage (V_{th}) for a fixed off current (I_{off}). However, the device still has to be designed to have a lower V_{th}. Taking the simple case of a uniformly doped device, the doping cannot be lowered because this reduces gate control of the device and lowering t_{ox} even further is very difficult from a manufacturability perspective. However, if one forward biases the substrate with respect to the source, then the V_{th} is lowered and the gate control of the device actually improves. Because the operating temperature has been lowered, the forward bias current through the source and drain to substrate p-n junctions ($\propto e^{kT}$) is still negligible.

Using the model to optimize for device switching speed (I/CV metric), design parameters were found versus channel length that agree with the 1997 SIA roadmap. The solid line in Figure 3 shows the threshold voltage that meets the I_{off} criteria, which at an 80° C operating temperature is around 0.4 V. However, if the operating

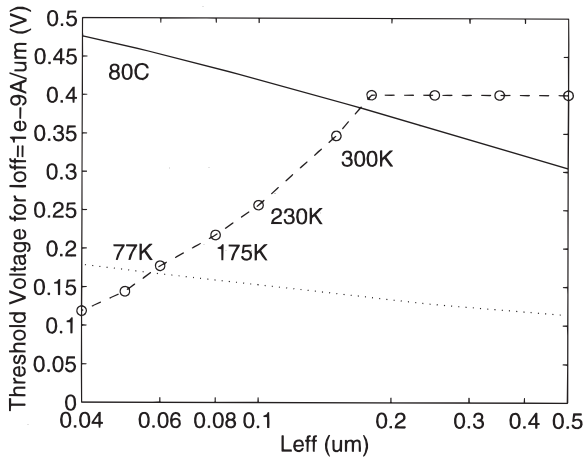

Fig. 3: Optimal threshold voltage versus L_{eff} at different temperatures for a fixed I_{off} of 1×10^{-9} A/um.

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continued

temperature is allowed to drop, then the V_{th} can be scaled at the same rate as V_{dd} (V_{dd}/V_{th} constant) as shown by the dashed line. The temperatures next to each point represent the approximate operating temperature needed. This scaling of V_{th} results in significant performance increases as can be seen in Figure 4 where the scaled temperature case (dashed line) rises well above the 80° C case (solid line). Although cooling to 77K gives the highest performance at a given L (dotted line), this approach seems unlikely given the current difficulties of cooling a processor consuming 10s of watts of power to such a temperature. The approach suggested here views scaling as the driver for a gradual lowering of temperature. Taking -50° C as a lower limit for gaseous coolants, the model projects that a V_{th} of 0.25 V would be achievable, which would result in a gain of about 1.7x in performance over not scaling temperature at all.

Continuing work is focusing on correlating the model with 2-D numerical simulations and actual device data to explore the model's predictions with real devices. ❑

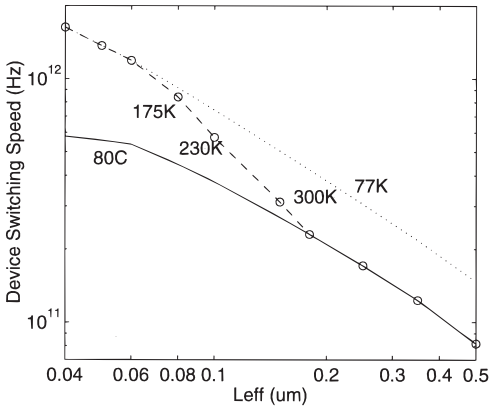

Fig. 4: Optimal device switching speed versus L_{eff} at different temperatures.

Role of FDSOI in Low Power High-Performance sub-0.1 μm CMOS

Personnel

S. Narendra
(D. A. Antoniadis, A. Chandrakasan and V. De - Intel)

Sponsorship

Unsponsored

In order to achieve both high performance and low power dissipation in scaled feature sizes, there is a need for both V_{dd} and V_t scaling. So as technology approaches sub-0.1 μm channel lengths, we need devices that can have low V_t along with reasonable short channel effects, sub-threshold slope, process variations, etc.

The goal of this work is to evaluate the role of using Fully Depleted SOI (FDSOI) instead of bulk for achieving this goal. Insulated channel in FDSOI should make it easier to achieve low threshold voltages while maintaining reasonable aspect ratio or short channel effect, compared to bulk.

These comparisons between bulk and FDSOI will be done at device and circuit levels through measurement and simulations. Lincoln Lab's 0.25 μm FDSOI technology will be used to calibrate the device and circuit simulators for extrapolation to sub-0.1 μm technology. ❑

Simulation Algorithms for RF Circuits

Personnel
O. Nastov
(J. White)

Sponsorship
Cadence Design Systems, Motorola Semiconductor, Harris Semiconductor, and MAFET Consortium

RF integrated circuit designers make extensive use of simulation tools which perform nonlinear periodic steady-state analysis and its extensions. However, the computational costs of these simulation tools have restricted users from examining the detailed behavior of complete RF subsystems. Recent algorithmic developments, based on matrix-implicit iterative methods, is rapidly changing this situation and providing new faster tools which can easily analyze circuits with hundreds of devices. We have investigated how these new methods by describing how they can be used to accelerate finite-difference, shooting-Newton, and harmonic-balance based algorithms for periodic steady-state analysis.

When simulating RF circuits, it is important to include parasitics associated with a layout. However, most layout extraction tools generate an enormous number of resistors, capacitors and inductors for a given layout, and this makes subsequent simulation expensive. There are a number of heuristic algorithms for reducing lines of resistors, capacitors and inductors, but we have recently derived an approach with a formal, but odd, optimality property. The approach is based on recasting the problem in to a problem in determining the distribution, with respect to resistance, of the capacitance and inductance. Then, one which can be solve the reduction problem directly using optimal Gaussian-quadrature. ❑

Software Tools for Process-Sensitive Reliability Assessments of IC Designs

Personnel
Y. Chery, S. Riege, and W. Fayad
(D. Troxel and C. V. Thompson)

Sponsorship
DARPA and SRC

Integrated circuits are currently designed using simple and conservative 'design rules' to ensure that the resulting circuits will meet reliability goals. This simplicity and conservatism leads to reduced performance for a given circuit and metallization technology. There have been recent significant advances in the understanding of the dependence of IC interconnect reliability on interconnect geometries, as affected by the circuit layout, and grain structures, as affected by the process history, and of how these affect the mechanisms of failure and the scaling of test results from accelerated testing conditions to service conditions. In addition, interconnect trees immune to electromigration failure can be recognized and filtered. This allows much more accurate process- and design-specific reliability assessments. We are developing a TCAD tool, ERNI, which will allow analysis of full and partial IC layouts, to extract interconnect features and calculate stress conditions for accurate running and final reliability assessments. ❑

Simulation Tools for Micromachined Device Design

Personnel

N. Aluru, A. Beskok, M. Schmidt, S. Senturia, D. Ramaswamy, F. Wang, and J. White

Sponsorship

DARPA

Micromachining technology has enabled the fabrication of several novel microsensors and microactuators. Because of the specialized processing involved, the cost of prototyping even simple microsensors, microvalves, and microactuators is enormous. In order to reduce the number of prototype failures, designers of these devices need to make frequent use of simulation tools. To efficiently predict the performance of micro-electro-mechanical systems these simulation tools need to account for the interaction between electrical, mechanical, and fluidic forces. Simulating this coupled problem is made more difficulty by the fact that most MEMS devices are innately three-dimensional and geometrically complicated. It is possible to simulate efficiently these devices using domain-specific solvers, provided the coupling between domains can be handled effectively. In this work we have developed several new approaches and tools for efficient computer aided design and analysis of MEMS.

Our most recent work in this area has been to particular, we have developed a matrix-free multi-level Newton method for coupled domain simulation. The approach has much more robust convergence properties than just iterating between domain-specific analysis programs, but still allows one to treat the programs as black boxes.

Our second effort is on finding fast approaches to computing geometric sensitivities of electrostatic forces, for use in fast coupled-domain simulation and structural optimization. Our new approach, based on the precorrected-FFT accelerated algorithm, is hundreds of times faster than direct computation for structures with as few as two thousand discretization unknowns.

Our third effort is in accelerating coupled-domain simulation by allowing physical simplifications where appropriate. We refer to this as mixed regime simulation. For example, self-consistent coupled electromechanical simulation of MEMS devices face a bottleneck in the finite element based nonlinear elastostatic solver. Replacing a stiff structural element by a rigid body approximation which has only 6 variables, all variables associated with the internal and surface nodes of the element are eliminated which are now a function of the rigid body parameters. The rigid/elastic interface forces obtained from the finite element stiffness matrix contribute to the equilibrium of the rigid body and by an application of the chain rule the elastic [rigid] variables contribution to the rigid [elastic] body part of the jacobian is determined. The rigid/elastic formulation is then coupled with the electrostatic solver in a multi-level newton method. With this approximation an entire comb drive accelerometer can be solved in less than 15 minutes compared to approximately 135 min for a just an elastic analysis. ❑

Dynamical Macro-Models for Nonlinear MEMS Devices

Personnel

M. Varghese and B. Romanowicz
(S. D. Senturia in collaboration with the research groups of J. K. White of MIT, J. Gilbert at Microcosm Technologies, and M. Allen of Georgia Tech.)

Sponsorship

DARPA

The MIT MEMCAD System has emphasized quasi-static 3-D numerical simulations of meshed structures as the basis for device modeling. However, designers typically prefer to work with dynamical analytical models with only a few degrees of freedom; we refer to these as "macro-models."

There has already been extensive work on automatic generation of macro-models for electrostatically actuated deformable elastic structures (see "CAD for Microelectromechanical Systems (MEMCAD)"). These devices have only linear constitutive properties, although they can exhibit geometric nonlinearities and positional hysteresis. We are now extending these concepts to devices that incorporate additional nonlinearities, either in their constitutive properties, or in their damping behavior.

Varghese, in collaboration with a research team at the David Sarnoff Research Laboratories, has studied the dynamic damping of motions in capacitive position sensors that must operate in vacuum, hence, without air damping. The specific approach, suggested by the Sarnoff team, is to use a suitably biased resistor to damp the mechanical vibrations of the structure that are set up by the applied voltages used to measure capacitance. Varghese has determined that this damping is highly nonlinear, because damping only occurs on half of the oscillatory cycle. But the method can be very effective when the proper choice of resistor value is made. The results of this work were reported at Transducers '97 in June 1997.

In a new DARPA-sponsored program, we are now examining a set of magnetically actuated devices of increasing complexity: Lorentz-force devices (no permeable materials), devices with linear permeable materials, devices with saturable permeable materials, and devices with hysteric magnetic materials. The goal is to develop macro-modeling methods, analogous to what has already been achieved for electrostatically actuated devices, for this class of magnetic devices. This program involves close collaboration with Prof. J. White at MIT and the Microcosm group for the development of boundary-element simulation tools for Lorentz-force and linear-permeable cases, and with Prof. M. Allen of Georgia Tech whose group will be fabricating and characterizing a new class of test structures designed by our group. ❑

Quasi-Static Modeling of Electrostatic Actuators

Personnel

E. Hung
(S. D. Senturia)

Sponsorship

DARPA

Electrostatic actuation is very attractive for microelectromechanical systems because of good scaling properties to small dimensions, high energy densities and relative ease of fabrication. A particular class of electrostatic actuators, in which parallel-plate capacitors are used, can suffer from an instability known as pull-in. The pull-in effect can severely limit the usable range of positions that can be controlled in a continuous fashion. For a simple parallel plate capacitor with gap g having a single moveable plate suspended by a linear spring, the pull-in instability limits the usable travel to g/3. This creates severe difficulties for actuator design.

We have been investigating methods for achieving electrostatic actuation using parallel-plate principles in ways that overcome this g/3 limitation. One method is the development of a concept called "leveraged bending." This is described separately in the report on the Polychromator. A second method is the zipper-actuator concept, originally proposed by Gilbert, and recently studied in our group using polysilicon devices fabricated at the MCNC Micromachining Foundry (called the MUMPs process). The specific device is an electromechanical varactor with a C-V characteristic that can be varied by changing the shape of the actuation electrodes (see Figure 5). The first public report of this work will be at the Hilton Head Solid-State Sensor and Actuator Workshop in June 1998. ❑

Fig. 5

Simulation of Squeeze-Film Damping in MEMS Devices

Personnel

J. Young and E. S. Hung
(S. D. Senturia in collaboration with M. Grétillat-IMT, Neuchâtel)

Sponsorship
SRC and DARPA

Many dynamical MEMS devices are designed to operate in a gaseous ambient, either because of a device requirement (such as a pressure sensor or microphone), or because it is desirable to use the air damping to control device dynamics. We have been working on methods for the efficient simulation of both small-amplitude (linearized) and large-amplitude (nonlinear) compressible squeeze-film damping of MEMS devices, using the well-known Reynolds equation from lubrication theory as the starting point. Air behaves like a viscoelastic medium, producing viscous damping when motions are slow, and acting like an air spring when motions are rapid. Analytical solutions in simple geometries of the linearized Reynolds equation demonstrate these effects, including an air-spring induced shift of the fundamental resonance mode.

Several results reported at major conferences during the past year include correct simulation of the ambient pressure dependence of the quality factor and resonance frequency of silicon microbeam resonators, and the development of basis-function methods for more rapid simulation of damping dynamics.

An important application is the damping of structures with perforations, since many MEMS devices have perforations through the moving parts either to speed up the release etch during fabrication, or to reduce air damping. When the perforations are small compared to the thickness of the dynamic part, then flow resistance through the perforations has a large impact on damping. By adding suitably sized flow resistors to the finite-difference simulator for the Reynolds equation, we have been able to account for this effect (see Figure 6). Agreement of the damping constant for a capacitive accelerometer between simulation and experiment is greatly improved with this enhancement. This project is now considered completed. ❑

Fig. 6

Co-Evolution of Stress and Structure in Polycrystalline Thin Films

Personnel
S. Seel, M. Kobrinsky, A. Blanchet, P. Muellner, T. Wagner, and E. Arzt
(C. V. Thompson)

Sponsorship
NSF

Structure evolution during formation of a polycrystalline film affects the stress state and other mechanical properties of the film. Nucleation, growth, and coalescence processes affect the initial grain size and stress state of a growing film. Grain boundary motion in the bulk and/or at the surface of a thickening film affects the grain size, as well as the grain shapes and the distribution of grain orientations in the final film. We are using transmission electron microscopy to characterize the early stages of film formation in systems with mobile grain boundaries. We will also characterize stress evolution during deposition in a variety of systems using in situ stress measurements. We are developing analytic models and simulations for the early stages of polycrystalline film formation. We are also adapting 2D simulations for modeling of grain structure evolution during thickening of deposited films.

The evolution of grain sizes and orientations in polycrystalline films which are heated after deposition can be driven in part by the strain energy resulting from deformation. However, to accurately calculate the strain energy, a better understanding of the film thickness, grain size, and crystallographic texture dependencies of deformation mechanisms in thin films must be developed. We are carrying out experiments to characterize stress and structure evolution during post-deposition annealing of films. These experiments include stress measurements made on metallic films deposited on coated Si wafers which are subsequently subjected to various thermal histories, including deposition and post-deposition at temperatures above and below room temperature. Experiments also include heating of films on membrane substrates in both conventional and high energy transmission electron microscopes, allowing simultaneous observation of deformation-induced dislocation dynamics as well as grain and twin structure evolution. Results from these experiments are being used as the bases for development of modeling and simulation capabilities for engineering optimization of film stresses and structures. ❑

Electric-Field Simulation for Field-Emission Devices

Personnel
J. Young and V. Rabinovich
(S. D. Senturia in collaboration with A. Akinwande and T. Korsmeyer)

Sponsorship
DARPA

The goal of this project is to develop a CAD tool for trajectory prediction in field-emission flat-panel display pixels. The basic structure being studied is shown in Figure 7. It consists of an emission tip with a 10 nm radius of curvature, a 0.2 μm thick gate with a 1 μm aperture, and a 0.5 μm thick focusing electrode located 0.5 μm above the gate. Not shown is the anode, which is far above the structure using the scale of the figure (1 mm away).

This project raises two challenges: the very different dimensional scales surrounding the tip and gate region compared to the far-field regions between the emission pixel and the anode, and the need to adapt boundary-element-based Laplace solvers for a mixture of Dirichlet and Neumann boundary conditions around the boundary of the solution space. The procedure now being used, developed in collaboration with T. Korsmeyer, is to use a Green's theorem kernel to calculate the potential gradient on surfaces with Dirichlet conditions, and potentials on faces with Neumann conditions. Then, using a source formulation, an equivalent pseudo-charge distribution on all the surfaces is determined from which electric fields can be found at any point of interest along an electron trajectory. These trajectories are obtained by integrating the electron equations of motion from various points on the emission tip to the anode. ❑

Fig. 7

Simulation of Cone Deposition Process for Field Emitter Displays

Personnel
Z. Sbiaa
(A. I. Akinwande)

Sponsorship
DARPA

One concept of a "Flat CRT's" is based on the use of an addressable matrix of Field Emission Arrays. Each addressable location of the matrix corresponds to a display pixel that is in close proximity to the phosphor screen. This display will have the image quality and brightness of a CRT in a thin, lightweight package.

The emitter cone structure as shown in Figure 8 is made up of a conducting cone (cathode) on a conducting substrate. The tip of the cone is located in an opening gate electrode which is a conducting layer separated from the cathode by an insulator. When a large enough potential difference is applied between the gate and the emitter, electrons will tunnel out of the tip. Due to symmetry, the electrons do not collide with the gate, but instead are accelerated to the anode which is biased positively with respect to the emitter and the cathode. The electrons strike the phosphors, causing them to luminesce.

Fig. 8: Cross section of a field emitter.

The electrical performances of the emitter depend on its geometrical parameters such as radius of curvature (r), the gate aperture (a) and the cone base angle (theta) as shown in Figure 8. The optimum shape for an emitter is a tall and thin vertical pillar with a sharp top. This shape will yield a low capacitance and therefore low leakage current, low dynamic power dissipation, and fast switching speed. Many parameters contribute to the final shape of the cone. The geometry of the initial structure (parting layer and initial gate opening radius), various process parameters (temperature, degree of flux collimation), and material parameters (diffusion coefficients, surface tension) affect the evolution of the cones with time. For this reason, we are developing a program which can simulate the cone deposition of the FED including all the geometrical, process and material parameters. The simulation results will be compared to actual fabricated devices.

One of the principle steps of the fabrication of the Field Emission Arrays is the metal deposition. The angular evaporation of a metal used as the parting layer and the vertical evaporation used in the formation of the emitter as a cone must be understood in order to produce cones of desired geometries.

There have been several approaches to simulate thin film growth which have varying levels of details. At one extreme are the atomic-level models such as molecular dynamics and atomistic Monte Carlo models which account for the positions and interactions of every individual atom. At the other end of the spectrum are the continuum and string algorithm models which only account for the position and development of the gross film surface. Somewhere in between are the ballistic deposition models which use abstractions of the film material which are larger than atomic size, but provide greater detail than string algorithms. Our approach is based on the ballistic deposition model because it's easy to implement and makes the execution time and memory requirements reasonable.

The numerical simulation program assumes an initial gate aperture that closed linearly with time. The cone is formed by vapor flux landing in the open area of the trench and solid condensation occurs during the impinging of particles onto the substrate. Our initial model do

continued

not take into account the surface diffusion due to the curvature gradients. A more detailed model including the surface diffusion and the temperature of the wafer is under investigation.

In our models we assume that the evaporated metal is coming from a point source. The program starts by generating metal vapor from this point source (Cosine law), and all the exposed region of the trench receives the vapor flux with the angular distribution. The exposed region is initially the radius of the trench, but it shrinks at a constant rate. The thickness of the metal deposited is calculated on both the parting layer and the base of the trench. The process is repeated until the simulation time has expired. Some simulation results are shown in Figures 9 and 10 have been obtained for different beveled parting layer. Figure 11 shows an array of emitters with high aspect ratio. They were fabricated using shallow bevel angles for the parting layer and high vertical deposition rate for the Mo cone. ❑

Fig. 9: Cone deposition onto 1 micron gate aperture with a 45 degree parting layer bevel.

Fig. 10: Cone deposition onto 1 micron gate aperture with a 90 degree parting layer bevel.

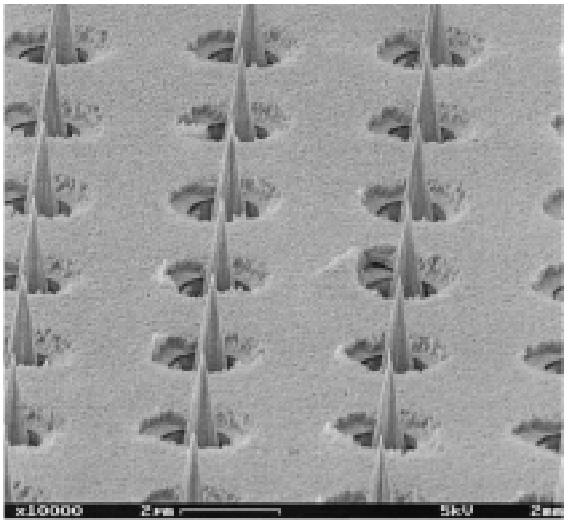

Fig. 11: High aspect ratio of field emitter.

Quantum Device Simulations

Personnel

C. B. Whan
(T. P. Orlando)

Sponsorship

NSF and AFOSR Grant

We carried out numerical simulations of single-electron transport through a quantum dot with superconducting leads, based on an experimental system. We introduce a general phenomenological model of transport through a quantum dot. In this model, we assume that the quantum dot is weakly coupled to the two leads by tunnel barriers. When an appropriate bias voltage V is applied to the leads, an electron can tunnel across one barrier into the dot and subsequently tunnel out through the second barrier. According to general tunneling theory, the tunneling rate across a barrier from side "a" to side "b", can be evaluated using the Fermi's Golden Rule, where T_{ab} is the phenomenological tunneling matrix element, and $f(x) = 1/[1 + \exp(x/k_BT)]$ is the Fermi function. N_a and N_b are the density of states, and μm_a and μm_b are the chemical potentials, on their corresponding sides. For our system, to compute the tunneling rate from one of the leads to the dot, we take the BCS quasiparticle density of states in the lead and assume that the dot itself has an evenly spaced (with spacing εe) discrete level spectrum.

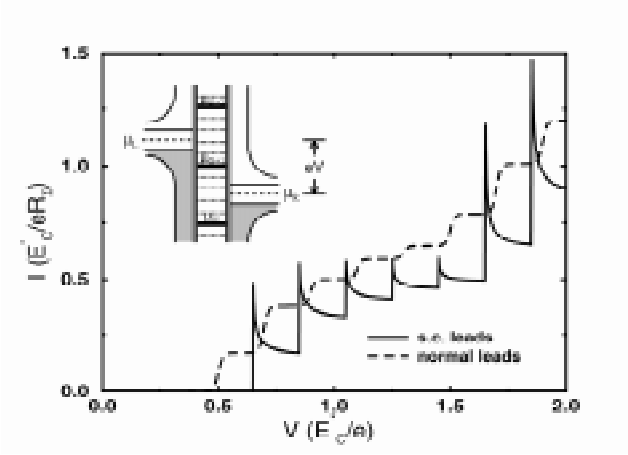

Fig. 12: Low temperature I-V characteristics of a quantum dot with superconducting leads (solid curve) and normal metal leads (dashed curve). The temperature is $k_BT = 0.02E^*_C$, and the superconducting energy gap in the leads is $2\Delta D = 0.3\ E^*_C$. The quantum level spacing is, $\varepsilon e = 0.2\ E^*_C$. The inset is a sketch of the energy spectra in the leads and the dot. Note the quantum dot energy spectrum includes the excitation spectrum (with spacing εe), and addition spectrum (with spacing $E^*_C = e^2/C + \varepsilon e$).

In Figure 12, we show a typical low temperature current-voltage (I-V) characteristic of the system. Here the temperature $k_BT = 0.02E^*_C$ ($E^*_C \equiv \int E_C + \varepsilon e$ is the spacing between chemical potential levels, and $E_C \equiv \int e^2/C\Sigma_S$ is the charging energy), the superconducting energy gap $2\Delta D = 0.3\ E^*_C$ and the quantum energy level spacing in the dot. When the leads are superconducting (solid curve), the I-V curve consists of a series of sharp peaks spaced εe apart. This is in contrast with the I-V curve of the same dot with normal metal leads (dashed curve), which has only gentle steps with the same spacing εe. Figure 12 is in good qualitative agreement with experiment.

In addition to the low temperature transport, our analysis shows that at higher temperatures thermal excitation of quasiparticles in the leads and thermal population of the excited quantum levels within the quantum dot should lead to interesting changes in the I-V curves. We also predict that when RF radiation is coupled to the system, the photon-assisted tunneling phenomena should manifest itself by producing extra periodic structures in the I-V curves, which might be useful in the millimeter wave detector/mixer applications. Due to the presence of many different characteristic energy scales, the rich dynamical properties of this system demand more exploration. ❑

Design and Analysis of VCSEL-Based Resonant Cavity Enhanced Photodetectors

Personnel

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(C. G. Fonstad, Jr.)

Sponsorship

University of Ulm and NSF

It is extremely desirable for monolithic optoelectronic integration to have emitters and detectors operating at the same wavelength, which can be fabricated from the same basic heterostructure. To this end we have modeled and studied (theoretically at this stage) the design of Resonant Cavity Enhanced Photodetectors (RCEPs) using heterostructure designed primarily for Vertical Cavity Surface Emitting Lasers (VCSELs).

A transmission matrix model was developed to compute the optical electric field and power in a complex, multi-layered heterostructure. The input to the program is the composition profile of the structure, and the program calculates the spectral response of the detector after first calculating the appropriate refractive indices, absorption coefficients, etc. The program can accommodate graded interfaces and doping profiles, as well as variations in temperature and in incident angle.

Simulation indicates that the most important parameter for the device designer is the top mirror reflectivity. As expected, there is a direct competition between the peak quantum efficiency of an RCEP and its spectral bandwidth. It is clear from the analysis that the narrow spectral bandwidth inherent in achieving a useful peak quantum efficiency from a single-resonant-cavity RCE fabricated from a modified VCSEL structure, and the significant shift of the resonance to longer wavelength seen with increasing temperature, that the usefulness of simple RCEP/VCSEL combinations is very limited. Consequently, we have also studied VCSEL-based RCEPs with broadened response spectra created by depositing additional, multiple-resonance mirror stacks on the top surface, after first modifying the original VCSEL top mirror stack. Initial indications from these studies, which are still in progress, indicate that this approach is very attractive.

A simple model allowing one to make a first order approximation to estimate the high speed behavior of RCEPs was also developed. The indication is that RCEPs can be twice as fast as PIN detectors with comparable quantum efficiencies.

This research was conducted by Thomas Knoedl during a six-month stay in our laboratories at MIT and was presented as his minor thesis (Studienarbeit) to the University of Ulm in January 1998. It is planned that Mr. Knoedl will return to MIT in the Summer of 1998 to continue with an experimental investigation of resonant cavity enhanced photodetectors fabricated from VCSEL heterostructures. ❑

Modeling of Grain Growth in Thin Films

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Sponsorship
NSF, SRC, and DARPA

We have developed computer simulations of normal and abnormal grain growth in thin films, occurring during deposition and subsequent heat treatments. We have included the effects of grain boundary drag due to surface grooving and due to the presence of solutes. The former leads to stagnation of normal grain growth at a point where the grain sizes are lognormally distributed and the average grain diameter is about three times the film thickness. This simulation result closely matches experimental results in a wide variety of systems. We also include the effects of surface and interface energy anisotropy, as well as strain energy anisotropy, to investigate the evolution of texture, on the average grain size and on the distribution of grain sizes in polycrystalline thin films. These simulations have demonstrated conditions which lead to experimentally observed abnormal grain growth or secondary grain growth. Predictive simulations of the evolution of the distribution of grain sizes and orientations can be made as a function of materials selection, film thickness, and processing conditions, in both continuous and patterned films. ❑

Numerical Techniques for Integral Equations

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Sponsorship
SRC, DARPA, and Multiuniversity Research Initiative

Finding computationally efficient numerical techniques for simulation of three dimensional structures has been an important research topic in almost every engineering domain. Surprisingly, the most numerically intractable problem across these various disciplines can be reduced to the problem of solving a three-dimensional potential problem with a problem-specific Greens function. Application examples include electrostatic analysis of sensors and actuators; electro- and magneto- quasistatic analysis of integrated circuit interconnect and packaging; and potential flow based analysis of wave-ocean structure interaction.

Although the boundary element method is a popular tool to solve the integral formulation of many three-dimensional potential problems, the method become slow when a large number of elements are used. This is because boundary-element methods lead to dense matrix problems which are typically solved with some form of Gaussian elimination. This implies that the computation grows as cubically with the number of unknowns tiles needed to accurately discretize the problem. Over the last decade, algorithms with grow linearly with problem size have been developed by combining iterative methods with multipole approximations. Our more recent work in this area has been to develop precorrected-FFT techniques which can work for general Greens functions. This approach uses an approximate representation of charge density by point charges lying on a uniform grid. An extension of this work showed that using dual grid (cube vertex) multipole expansions is more efficient for a given required accuracy than either point-charge or standard (cube center) multipole expansions. As is not surprising, the gain in efficiency can be as much as a factor of eight.

After a decade of research on fast numerical schemes for potential problems, a somewhat unsatisfying picture has emerged: On one side are methods which exploit the fact that interactions can be approximated by low order

continued

expansions if their sources are sufficiently separated in space. Algorithms that are based on that principle only give a partial solution to deal with complicated problems, in that they allow potential calculations in nearly linear time. However, it still remains unclear how to precondition these algorithms efficiently. On the other side are wavelets, which allow nearly sparse representations of integral operators. Furthermore, the multilevel setting of wavelets allows the construction of efficient preconditioners. Since wavelets are usually constructed in a parameter space of the boundary surface, they are inefficient when the geometry is represented by a large number of parameter patches.

Rather than using vanishing moments in the parameter space, we have constructed a wavelet-like basis with vanishing multipole expansion coefficients, thus avoiding the need of a surface parameterization. We have obtained numerical results which show that integral operators are nearly sparse in this basis, even for complex, multiply connected geometries. Furthermore, the preconditioned system converges in a number of iterations that is independent of the geometry as well as the discretization fineness. We have also investigated improving the condition number by developing second-kind formulations. ❑