
UHV-CVD Growth of Erbium Doped Si/Si_{1-x}Ge_x Emitters and SiGe Photodetectors

Personnel

K. Chen, L. Giovane, A. Luan, M. Morse, and J. Michel (L. C. Kimerling)

Sponsorship

AFOSR, DARPA, Rome Laboratory - Hanscom AFB, and SRC - MPC Administered

Erbium-doping of silicon-based materials has been achieved using Ultra-High Vacuum MetalOrganic CVD (UHV-MOCVD). By using growth temperatures as low as 530 °C, we have produced highly metastable erbium concentrations, greater than two orders of magnitude above the solubility. Photoluminescence has been used to compare these samples with erbium-implanted silicon. At cryogenic temperatures, the light output from the two processes is comparable, but the decrease in intensity at room temperature is much less severe for the CVD grown samples. The first silicon-based double heterostructures (Si/SiGe) doped with erbium have also been grown in order to take advantage of electrical and optical confinement for more efficient power output. Further improvements from structure optimization and lower growth temperatures are underway.

We are studying SiGe heterostructures in collaboration with Professor Fitzgerald (MSE). SiGe alloys can be used to push the long wavelength detection limit of silicon-based photodetectors to 1.5 μm. We are developing a pin photodetector structure that consists of a strain-balanced Ge_(x+d)Si_{(1-(x+d))}/Ge_(x-d)Si_{(1-(x-d))} superlattice intrinsic region grown on a Ge_xSi_(1-x) relaxed buffer. The relaxed buffer is grown at 900 °C using a composition-graded layer of 10%Ge/μm. The thickness of the alternating layers is limited by the lattice misfit critical thickness, but there is no limit to the number of layers in the superlattice, because the layers are strain balanced. This structure permits the incorporation of high germanium fraction, compressively strained layers. We have measured very strong absorption ($\alpha = 6 \times 10^3 \text{ cm}^{-1}$) at 1.3 μm, which is sufficient for high efficiency photodetectors. Currently the integration of these detectors with polycrystalline Si waveguides is being studied. □

III-V/GeSi/Si Heterointegration

Personnel

M. Bulsara, S. Ting, M. Groenert, M. Currie, T. Langdo, V. Yang, L. McGill, and G. Taraschi (E. A. Fitzgerald)

Sponsorship

NSF/MRSEC and ARO

Recent advances in heteroepitaxy have allowed the fabrication of lattice-mismatched, relaxed GeSi layers on Si with very few dislocations penetrating the upper layers. This larger GeSi lattice can be subsequently used for the lattice-matched growth of III-V materials like InGaP and GaAs. The ultimate goal is the co-habitation of III-V optical devices and Si integrated circuitry, allowing functionality and cost improvements in data storage, high quality printing, and high speed processing systems. The materials challenges are decreasing the residual dislocation density even further, improving the III-V/VI interface, and establishing process integration. Recent research results have revealed the critical nature of the materials processing at the GaAs/Ge interface. Without performing epitaxial growth within certain process windows the GaAs grown on this near-lattice matched substrate can possess a dislocation density as high as 10⁹cm⁻², whereas the optimized process results in GaAs with a defect density as low as 10⁴-10⁵cm⁻². Using these optimized interfaces, we have been able to integrate GaAs on Si with unprecedented perfection, as revealed by the cross-section TEM micrograph shown below. Such films can now be used for prototyping GaAs devices integrated on Si substrates. □

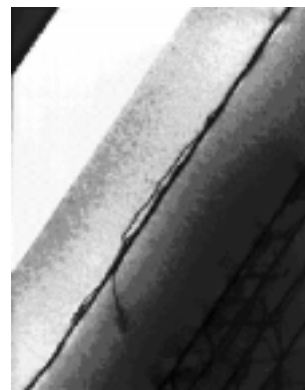


Fig. 1: Heteroepitaxial GaAs on Si using an advanced SiGe Relaxed Buffer Layer.

Si/SiGe Nanostructures

Personnel

M. Currie, T. Langdo, and G. Taraschi
(E. A. Fitzgerald)

Sponsorship

NSF/MRSEC and DARPA

In conjunction with a new initiative group, we are developing two dimensional electron and hole gases in the Si/SiGe system. Such structures require the use of relaxed, defect-engineered SiGe on Si substrates. The epitaxial films can be patterned laterally to produce low-dimensional structures. We are investigating the physics of carrier transport in SiGe/Si heterostructures and we are also interested in mesoscopic device sizes which may be experienced as Si CMOS technology matures. We have started a collaborative program with EE to investigate low-temperature selective Si and SiGe growth in 100 nm-sized windows. Successfully controlling this process will allow the fabrication of Si nanostructures and vertical nano-MOSFETs. □

Device Degradation

Personnel

M. Groenert
(E. A. Fitzgerald)

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Current electronic and optical devices are successful in the marketplace if performance, cost, and reliability are optimized. Achieving higher device reliability hinges on knowing the microstructural detail of the failure mechanisms. Techniques like transmission electron microscopy, electron beam induced current, chemical etching, electrical measurements, and statistical analysis can be used to determine the most important failure modes of device structures. In particular, the reliability of experimental laser structures which can possess a larger number of intrinsic defects are being explored, and methods for extending device lifetime are being developed. □

Novel Semiconductor LED and Laser Materials

Personnel

M. Bulsara, A. Kim, S. Ting, S. Makan, and S. Ransom (E. A. Fitzgerald)

Sponsorship

NSF/MRSEC and ARO

AlGaAs/GaAs and InGaAsP/InP laser materials have been developed due to the lattice-matching potential of the materials. However, there is an increasing number of applications needing wavelengths and power levels which can not be produced by these materials. Removal of the lattice-matching requirement allows one to design lasers which will emit at a variety of new wavelengths when fabricated on conventional substrates like GaAs and Si. In particular, visible light emitters in the InGaP system and 1.3 μm emitters in the InGaAs will be explored. The effect of engineered defect structure on the reliability of these devices will be a key issue in defining the utility of these lasers.

We have developed an understanding of the phase separation process in graded InGaAs/GaAs relaxed layers grown by OMCVD. The strain fields from buried misfit dislocations and the subsequent induced surface roughening aid phase separation, which can lead to high dislocation densities in the relaxed InGaAs. We have developed a model that explains this phase separation, and through application of this model, we have been able to produce relaxed $\text{In}_{30}\text{Ga}_{70}\text{As}$ on GaAs with low threading dislocation densities. \square

Silicon Microphotonic Data Link with Modulation and Gain Elements

Personnel

A. Agarwal, S. Ahn, T. Chen, J. Foresi, L. Giovane, K. Lee, L. Liao, D. Lim, M. Morse, E. Ouellette, A. Thilderkvist, and J. Michel (L. C. Kimerling)

Sponsorship

DARPA, Rome Laboratory - Hanscom AFB, and SRC - MPC Administered

Silicon microphotronics is a basic building block for optical sensing circuits, optical networking for telecommunications, and IC level optical interconnection. This program examines the performance and process optimization of integrated emitters and waveguide components, and studies the key materials integration issues for SOI and SiGe based structures. The advantages of a silicon-based optical interconnection technology are low cost, high bandwidth clock distribution, reduction of chip pin-out density by multiplexing, and reduced line driver power dissipation. We have demonstrated a silicon Light Emitting Diode (LED) that gives room temperature, sharp line emission at $\lambda = 1.54 \mu\text{m}$, based on Er implantation and standard CMOS process steps at MIT's Microsystems Technology laboratory. We have integrated these emitters with a MOSFET driver (3 dB roll off, light modulation at 20 kHz) and have realized the first optical voice link with a cooled Si:Er LED (200K) as the emitter. In addition to implantation, UltraHigh Vacuum Chemical Vapor Deposition (UHVCVD) has successfully incorporated high concentrations ($>10^{19} \text{cm}^{-3}$) of Er by using a metallorganic precursor. Moreover, strip and ridge silicon-on-oxide waveguides have been developed in parallel, since silicon waveguides are ideally suited for optimal coupling to silicon devices. Losses of less than 1 dB/cm were measured for these waveguides.

While these materials are excellent performers, polycrystalline silicon provides necessary flexibility in processing and photonic circuit architecture. We have studied the recrystallization of Er-implanted polysilicon and have demonstrated that it can be an efficient light emitter. Additionally, poly-Si:Er can be incorporated in a vertical cavity structure. Using a cavity of alternating Si/SiO₂ films, we can enhance the spontaneous emission rate of poly-Si:Er. We have fabricated cavities ($Q \sim 300$) with a resonance at the Er emission wavelength of 1.54 μm . We have also demonstrated small radius bends and high angle splitters in poly-Si strip waveguides with $0.2 \times 0.5 \mu\text{m}$ cross sections. Bend radii between 1 and 100 μm

continued

The Effects of Grain and Precipitate Structures on Interconnect Reliability

have been tested with losses less than 0.5 dB. Y-branch, 3 dB power splitters with splitting angles of 20° and 30° exhibit losses of about 1°. The real estate required for integrated devices using these waveguide components is greatly reduced compared to more typical III-V or SiO₂ waveguide systems. While the losses here are comparatively large, the smaller dimensions and embedded coupling of the integrated devices decreases the impact of this loss.

We have designed light modulators based on both free carrier absorption and free carrier refraction. One example is a modulator based on parallel silicon dielectric waveguide mode coupling. The index of refraction of one guide is controlled by free carrier injection and results in a change in the total power coupled from one waveguide to the other. This modulator is capable of 30 MHz bandwidth with 20 dB contrast at 0.5W power desorption with a 600 μm coupling length. □

Personnel

S. Riege, C. Hau, B. Knowlton, H. J. Frost, and J. J. Clement
(C. V. Thompson)

Sponsorship

SRC

We have studied the effects of widely different grain structures on electromigration in interconnects. We found that varying the grain size in unpatterned films over three orders of magnitude (1000Å to 100 μm) did not significantly affect the reliability of interconnects. However, we found that post-patterning annealing, which drives the microstructure from polygranular to near-bamboo to full bamboo morphologies, leads to dramatically improved reliabilities. We have simulated this post-patterning structure evolution, most recently including the effects of grain boundary pinning by Al₂Cu precipitates. In lines with bamboo structures, all grain boundary planes lie perpendicular to the axis of the line. As the lines evolve toward fully bamboo structures, in which all grain boundaries traverse the width of the line, clusters of non-bamboo grains remain. The numbers and the distribution of the lengths of such clusters are critical to the reliability of interconnects. Cu alloying retards electromigration, and Al₂Cu precipitates also function as Cu reservoirs during electromigration. However, precipitates inhibit the transformation to the much more reliable bamboo structure. We are comparing experimental results with results from analytic models and computer simulations of grain structure evolution and its effects on electromigration in order to calibrate and improve the models and simulations.

In addition to experimental studies of the effects of precipitates on the post-patterning grain structure evolution and reliability of Al-based interconnects, we are also carrying out in situ observations of grain structure evolution in continuous and patterned films of pure Cu. We are also investigating the use of scanned laser annealing techniques to produce controlled microstructures in both Al and Cu-based interconnects, for experiments on interconnects with specific grain structures.

continued

We are also developing new electromigration test structures and testing methodologies to test structure-sensitive simulations of electromigration and electromigration-induced failures. Calibrated and validated simulations of the effects grain structures and of alloy selection and design on electromigration-induced failure of IC interconnects will allow alloy and process design for optimum interconnect reliability. □

Ion-Beam-Induced Chemical Vapor Deposition of High Conductivity Lines or Films with Nanocellular Structures

Personnel

T. Chiang, F. Ross, and F. Greer
(H. H. Sawin and C. V. Thompson)

Sponsorship

NSF

A Focused Ion Beam (FIB) can be used to induce local chemical vapor deposition of a film for x-ray mask repair or circuit restructuring. We have characterized the growth kinetics and microstructure of Au and Cu films deposited using ion-induced MOCVD. We have developed detailed kinetic models for the energy transfer mechanism leading to decomposition, the surface reaction kinetics which govern the film growth rate and purity, and the evolution of the resulting polycrystalline structure. We have shown that global heating or laser-induced local heating allows the deposition of purer more highly conductive films, and that flooding the reaction zone with atomic hydrogen will have a similar effect. Our most recent work has focused on use of broad ion beams for deposition of films with *nanocellular* structures in which parallel metallic crystalline columns with 100A-scale diameters span the thickness of the films but are separated by thin, low-conductivity organic layers in the plane of the film. These structures are obtained under conditions leading to cellular growth caused by incorporation of non-volatile reaction products. Films with these novel microstructures have potential applications in microelectromechanical and magnetic devices. □

Process Analysis and Simulation for PV and IC Applications

Personnel

S. Ahn, A. Kelley, M. Platero, A. Smith, E. Wu, and S. Zhao
(L. C. Kimerling in collaboration with Siemens Solar, Camarillo, CA)

Sponsorship

NREL and Wafer Engineering & Defect Science Consortium

Our research effort continues to focus on the structure, stability, and kinetics of lifetime degrading defects in Si for the optimization of solar cells and integrated circuits. We have applied the knowledge base created by this research in the form of two process simulators. A simulator of Fe gettering during the Al back surface contact anneal incorporates our understanding of dopant-enhanced solubility and our results from Al gettering experiments. The second simulator treats defect reaction kinetics. An extensive set of defect reaction equations describes the role of defect, dopant concentrations and processing conditions. The process simulators provide a means of optimization of materials specifications and processes to achieve a desired minority carrier diffusion length.

We have constructed an Fe gettering simulator that quantifies the design and effectiveness of gettering treatments. The simulation includes the competing gettering mechanisms of Internal Gettering (IG), segregation to molten Al and acceptor-dopant enhanced solubility. The contamination, processing time-temperature profile of the gettering step, the material specifications, and the device structure are simulator inputs. The resulting contamination profile of the wafer is the output that determines the minority carrier diffusion length. We have produced experimental results to verify this model. Gettering experiments by Al back surface contact formation were performed at various annealing temperatures using a quench to study the instantaneous contamination levels. The data analyzed, according to the model, give values of precipitate density and size that are consistent with the Cz silicon used. Fe is a lifetime limiting defect and understanding its removal is of primary importance, however, the principles of the simulator can be easily applied to other transition metal contaminants.

The point defect reaction simulator allows for the analysis of the interaction of point defects to determine material specifications required for a desired minority carrier lifetime. The interactions among self-interstitials (Si), vacancies (V), impurities (C,O), and dopants (B,P) in silicon not only lead to the formation of undesirable point defect products which affect device operation, but they also generate defect associates that control processes such as diffusion of dopants. Within the framework of reaction kinetics, for the first time, we have simulated the defect reaction process.

The simulator can be used to construct the interstitial defect reaction hierarchy diagram, to predict defect behavior in device processing and to characterize background dopant and impurity concentrations (e.g., [B], [P], [O], and [C]) in Si by combined electron irradiation and DLTS measurement techniques. Due to an availability of controlled data, the simulator has been applied to the case of a Reactive Ion Etch (RIE), a process which induces point defect reactions, and the predicted defect depth profiles are consistent with those measured in the PhotoLuminescence (PL) experiments. □

Electrically Active Interfaces

Personnel

M. Spears and Y.-C. Chung
(H. L. Tuller)

Sponsorship

NSF/MRSEC

Electrically active grain boundaries are examined in ZnO ceramics. Boundaries with controlled dopants and oxidation states are prepared and examined by dc and ac impedance and Deep Level Transient Spectroscopy (DLTS) techniques. Individual electrically active boundaries are isolated by an in-diffusion process. A number of well defined DLTS peaks were obtained for each of the boundaries doped with Pr plus one or more of a number of transition metal elements including Mn, Ni, and Co. Presently, the focus is moving towards the growth of oriented ZnO films with more readily controlled boundary structures and chemistry and the interrogation of individual boundaries with the assistance of a micro-probe station. □

Ferroelectrics for High Strain Actuation

Personnel

Y. Avrahami C. Heremans
(H. L. Tuller in collaboration with Y.-M. Chiang and N. Hagood)

Sponsorship

ARO

Lead perovskite systems are being explored as potential candidates for high strain actuators with large thermal stability and low hysteresis. Field induced antiferroelectric-ferroelectric transitions show high strain levels in polycrystalline materials. The research focuses on actuation characteristics, in particular on polarization and strain dependence on the electric field.

Preferred orientation and single crystal growth is considered as possible means to further increase strain levels. Efforts are being initiated to grow single crystals by the top seeded solution method. □

Epitaxial Films for Micromechanical Devices

Personnel

M. Currie
(E. A. Fitzgerald)

Sponsorship

Draper Laboratories

Miniature, high-quality microphones, accelerometers, gyroscopes and other sensors can be fabricated from thin, unsupported semiconductor films. These films are fabricated by using selective etches which etch doped semiconductors much more slowly than undoped material. Currently, B diffusion is used to create a highly doped region. Unsupported films are created by using the selective etch to remove the substrate. Our research has shown that the diffusion process leads to a metastable balance between strain relief by dislocations and mismatched strain created by high boron concentrations. Epitaxial layers in the GeSiB system appear to be promising films for defect-free micromachined structures. We have recently discovered that the relaxed SiGe alloys we have been fabricating for the integration of III-V materials and SiGe FETs have unique etching properties that can be exploited in the fabrication of micromachined structures. We are currently optimizing the relaxed SiGe materials for micromachined structures and studying the etch-stop mechanism. □

Microengine Materials and Structures

Personnel

K.-S. Chen and K. Lohner
(S. M. Spearing)

Sponsorship

ARO and DARPA

Material characterization, thermo-structural analysis and refractory ceramic microfabrication process development are proceeding in support of the microengine project. The potentially very high power density of the microengine is predicated on achieving high rotational speeds and operating temperatures, which implies highly-stressed structures whose performance is limited by the strength, creep and oxidation of the materials of which they are made. Since silicon and refractory ceramics are very brittle, and therefore variable, materials it is essential to obtain strength data from specimens which have been fabricated by the same process and at similar sizes to the intended application. A testing procedure, utilizing microfabricated biaxial flexure specimens and radiused-hub flexure specimens, has been developed for this purpose. Strengths in excess of 4 GPa have been obtained for deep reactive ion-etched silicon, however, local strengths can fall far short of this if proper care is not taken with the etch conditions. The results of the mechanical testing are being combined with finite element structural and heat-transfer analysis of the microengine components in order to verify the overall structural integrity of the design, utilizing probabilistic methods. Work has been initiated to develop the necessary processes to microfabricate refractory ceramics, particularly silicon carbide, in order to increase the viable operating temperature of the engine. □

Personnel

L. Giovane, M. Bulsara, S. Samavedam, S. Ting, A. Kim, T. Langdo, M. Currie, V. Yang, G. Taraschi, and L. McGill (E. A. Fitzgerald)

Sponsorship

NSF/MRSEC, ARO, and Discovery Semiconductor

Completely relaxed mismatched epitaxial layers with relatively low threading defect densities can be achieved using graded-composition GeSi layers grown at high temperatures. Alternatively, completely strained and very metastable GeSi layers can be produced by limiting the number of dislocations which can readily nucleate. Yet, a complete understanding of dislocation nucleation and interaction in these structures is still absent. The details of nucleation of dislocations, how they interact, and new methods of decreasing threading dislocation densities in relaxed materials will be explored. Improvements in tailoring both strained and relaxed layers will be used in novel GeSi/Si structures which can absorb 1.3 μm light in relatively short lengths of material (1 - 5 μm). In the III-V materials systems, relaxed InGaP, InGaAs and GaAsP layers on GaAs will be engineered to have few defects, resulting in short wavelength and infrared LEDs and lasers on GaAs. Our research has led to an increased understanding of work hardening in graded epitaxial layers, as well as revealing strain-dependent phase separation in relaxed, graded InGaAs/GaAs structures.

Recently, we have capitalized on our increased understanding of the interaction between the epitaxial surface and the buried misfit dislocation structure. By inserting a planarization step within the relaxed SiGe graded layer, we have been able to drastically decrease the number of dislocation pile-ups that form in the material. The result is that we can produce strain-free Ge at room temperature with low threading dislocation densities ($\sim 1 - 2 \times 10^6 \text{ cm}^{-2}$). Due to the high-quality of the Ge, we were able to fabricate Ge photodiodes integrated on Si with near ideal characteristics and reverse leakage currents 2 orders of magnitude less than other reported Ge on Si photodiodes (below). \square

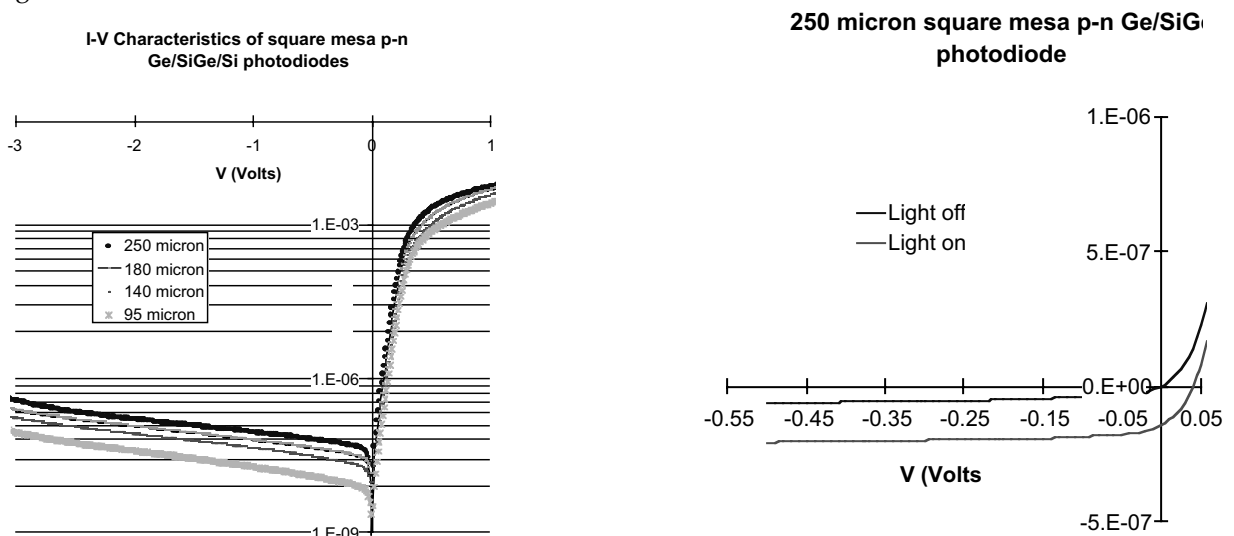


Fig. 2

Solventless Low Dielectric Constant Thin Films

Personnel

C. B. Labelle and K..S. Lau
(K. K. Gleason)

Sponsorship

NSF/SRC Engineering Research Center for Environmental Benign Semiconductor Manufacturing

Many candidates have been proposed for replacing CVD silicon dioxide as an Interlayer Dielectric Layer (ILD). The primary goal is to reduce the dielectric constant (k) in order to improve interconnect performance. Lowering k reduces RC time constants, cross-talk and power consumption. At the same time, the material properties of a new ILD must be sufficient to satisfy an array of process integration issues. For a manufacturable and sustainable process, these additional requirements must include Environmental Safety and Health (ESH) considerations of consumable chemicals and their by-products. For any given material, the ESH impact will scale with the number of ILD layers used. In this regard, the technological goal of lower k , which reduces the number of ILD levels, is also favorable from an ESH perspective. The maximum benefit will be derived by addressing the ESH concerns before implementing a low- k film production process.

Potential low- k ILD materials are produced either by spin-on and Chemical Vapor Deposition (CVD) processes. Spin-on application, which is also used for photoresist, requires solvents for dispensing the low- k material and for subsequent cup-rinsing. This raises potential concerns about worker exposure and waste disposal. Solvent screening studies with the goal of finding more ozone safe compounds which are and free from VOC regulations have been published by manufacturers of spin-on dielectrics.

CVD avoids solvent usage and is also compatible with the move towards dry processing and cluster tools. Of the CVD ILD candidates, the fluorocarbon (CF_x) films, have the lowest k , 1.9-2.3, depending on composition. PerFluorinated Compounds (PFCs) have been used to deposit CF_x films and may also be present in the effluent of the reactor or by chamber cleaning. In our laboratory, alternative precursors for CF_x deposition have been explored. Using pulsed plasma enhanced CVD and pyrolytic CVD from a non-PFC compound,

hexafluoropropylene oxide, films with $k < 2.0$ have been grown. This work suggests a key advantage of the hexafluoropropylene oxide is its known decomposition pathway to gaseous CF_2 (difluorocarbene). Unfortunately, hexafluoroacetone, a known teratogen, is an unavoidable impurity in hexafluoropropylene oxide. Thus, other volatile compounds with known decomposition pathways to difluorocarbene were identified. These were further screened on the basis of economic viability (supplier, cost, retooling). Further screening was based on health risks (acute toxicity, chronic toxicity, reproductive toxicity, carcinogenicity) and environmental impact (ozone depletion, global warming potential, atmospheric lifetime). Deposition rates, chemical composition and ESH impacts were evaluated for the remaining hydrogenated chlorofluorocompounds (HCFC) and hydrogenated fluorocompounds (HFC). The resulting films were found to have dielectric constants < 2.4 and low dielectric loss tangents (< 0.01). □