Statistical Metrology - Quantifying, Modeling, and Assessing the Impact of Spatial Variation in Semiconductor Manufacturing

Personnel

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Sponsorship

DARPA, AASERT, and ARO

As device and interconnect dimensions continue to scale below quarter-micron dimensions, maintaining process and structure uniformity at each processing step is increasing in importance and difficulty. Yield loss due to systematic sources of variation will begin to supersede loss due to particle defects and random sources of variation. Circuit performance will also become increasingly limited by device and interconnect variation.

Statistical metrology is a new methodology we are developing to quantify, model, and understand the impact of spatial variation in semiconductor processes and device/interconnect structures. Key elements of the methodology include test structures, experimental designs, and measurement methods to gather the large volumes of data needed for statistical analysis; the development of algorithms and tools to decompose and identify variation sources; modeling methods to capture the systematic elements of device or interconnect variation (particularly as a function of layout parameters); and CAD tools and methods to understand the impact of such variation on circuit performance and yield.

The application of these methods have been in two primary areas: pattern dependencies in Chemical-Mechanical Polishing (CMP), and variation in polysilicon and metal linewidths. The following abstracts summarize work on methods for rapid characterization and modeling of CMP in several process application areas, including metal dielectric (oxide) polishing, Shallow Trench Isolation (STI) formation, and in copper damascene polishing. Finally, development and application of CAD tools which utilize variation models (such as those generated in the above experiments) to study the impact of variation on circuit performance is summarized. These studies are deeply collaborative with partners at Texas Instruments, Sandia National Laboratories, Applied Materials, Hewlett-Packard, PDF Solutions, Digital Semiconductor, Lucent Technologies, and LSI Logic. ❑

The CMP Characterization Mask Set

Personnel

D. Ouma, B. Stine, and T. Park
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Sponsorship

DARPA, ARO, Intel, Sandia National Laboratories, Hewlett Packard, and SEMATECH

In order to enable the characterization and modeling of pattern dependencies in oxide CMP (as well as other CMP processes), we have designed the CMP Characterization Mask Set (Figure 1). The masks are intended to facilitate rapid CMP consumable, process, and tool characterization and evaluation. Each mask is targeted toward an individual source of pattern dependent variation. To this end, four separate single-layer masks have been designed to probe structure area, pattern density, line pitch, and structure aspect ratio effects, respectively. The masks support simplified metrology tools and techniques including optical film thickness and profilometry measurements. Each mask is designed to produce a 1.2 cm x 1.2 cm die; larger versions (2.0 cm x 2.0 cm) of the density, pitch and area masks have also been made available.

Fig. 1: CMP Characterization Mask Set.

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The first mask, the area mask, has patterned structures with areas ranging from 10 x 10 micrometers to 3 x 3 millimeters across a variety of pattern densities achieved by altering the fill pattern inside each structure. In addition to the area structures, there are also structures to test the role of geometric orientation (horizontal lines versus vertical lines).

The pitch mask is the second mask. The density of each structure is fixed at 50% (equal linewidth and linespace), and the pitch is varied from 2 to 1000 micrometers for a total of 36 structures per die. With the exception of the structures with a pitch less than 20 micrometers, each structure is 2 x 2 millimeters in size. Features with a pitch of 20 micrometers or less are lumped into a single 2 mm x 2 mm structure. There are also spatial replicates for many of the structures so that pitch effects can be separated from purely spatial effects.

In the density mask, the third mask, the pattern density (the ratio of raised metal area in each structure to the total area of each structure) was varied systematically from 4% to 100% from lowest in the lower left corner to greatest in the upper right corner while the pitch of each structure was fixed at 250 mm. A total of 25 structures each 2 mm x 2 mm are arranged in a 5 x 5 grid, in addition to a border region which extends 1 mm from the edge of the 25 structures to act as a buffer. Without the border, structures with the lowest density would contact structures with the highest density (on neighboring die) and interact strongly.

The fourth mask is designed to explore the role of the ratio of perimeter to area. A total of 8 structures replicated twice are designed. In addition, each set of 16 structures is replicated six times across the die but with different spacings between structures ranging linearly from 10 to 60 micrometers for a total of 96 structures.

Figure 2 shows the results of oxide thickness variation measured and extracted for each mask using profilometry in process experiments using two different polishing pads – a key consumable in CMP: the IC-1400 and IC-2000. Several striking results are readily seen. We find that pitch and perimeter/area ratio have almost no impact on polishing performance, while density has a large linear effect on the final oxide thickness. Finally, structure area size has no clear impact once the density variations have been accounted for. The mask set thus enables simple empirical modeling, and is being used to extract key empirical parameters (such as planarization length) needed in analytical/physical modeling of the process. Through on-going work with the SEMI CMP standards committee, we hope to establish the characterization mask set and analysis procedures as a standard vehicle for evaluating CMP consumables, processes, and tools. ❑

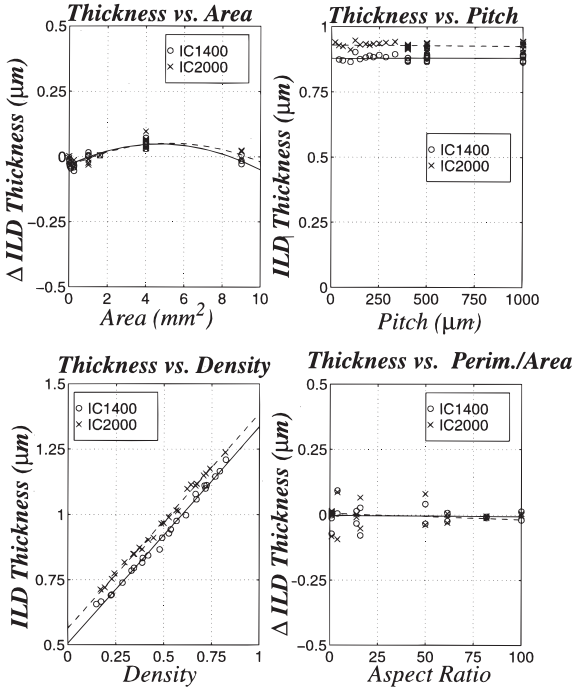

Fig. 2: Empirical results from CMP characterization mask set.

An Integrated Characterization and Modeling Methodology for CMP Dielectric Planarization

Personnel

D. Ouma, B. Lee, C. Oji, and B. Stine
(D. Boning and J. Chung)

Sponsorship

DARPA, Texas Instruments, and PDF Solutions

Efficient chip-level CMP models are required to predict dielectric planarization performance for arbitrary layouts prior to CMP. We are developing an integrated calibration and modeling methodology for oxide planarization which extends previous work in several important ways. First, we have developed improved characterization methods for model calibration, including new short flow test masks and simplified planarization model parameter extraction. Second, we have developed an efficient physically motivated density calculation and integration with a planarization model for prediction of oxide thickness above and between metal structures across the entire die. Predictions based on the model show excellent agreement when applied to layouts not used in model calibration.

In previous work, we have developed an analytic model for oxide CMP based on an effective layout density calculation. The critical parameter in this model then becomes the "planarization length" or method for determining the effective density. As shown in Figure 3, a new variant of mask sets have been designed which enable this planarization extraction using abrupt "step density" changes in the layout. Using experimental measurements from wafers fabricated and polished with

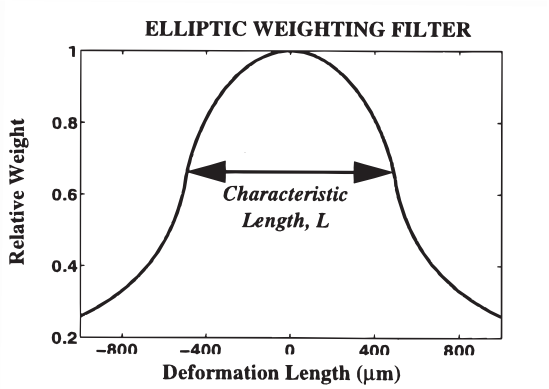

Fig. 4: 1-D cross-section of an elliptic weighting filter. The characteristic length is defined as the section length when the relative weight has dropped to $2/\pi$. The filter shape corresponds to the deformation profile of an elastic material under distributed load in a circle of radius L/2.

Fig. 3: Characterization masks showing lines along which optical measurements were taken for model calibration (L1 and L2) and verification (L3-L6). Mask 1 was used for calibration and Mask 2 for verification of the modeling methodology.

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these masks, we are able to extract a "planarization response function" as shown in Figure 4. Using this weighting function, we are able to calculate an effective pattern density for a given layout, such as the density pattern shown in Figure 5 for Mask 1.

Using the improved extraction and planarization response function, excellent predictions of oxide polishing performance are possible, as shown in Figure 6 (for the oxide thickness along cut lines shown in Figure 3). ❑

Fig. 5: Effective pattern density optained with an elliptic weighting filter.

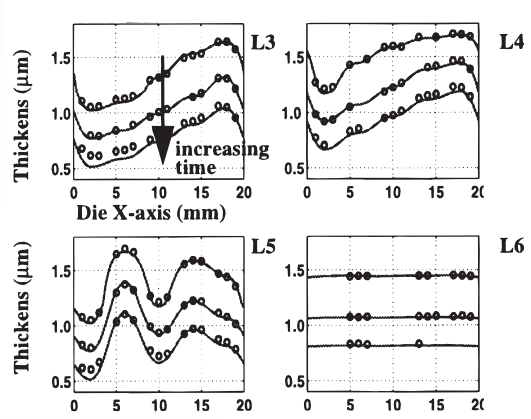

Fig. 6: Model prediction for ''up'' areas polished under process a for different times. The elliptic weighting filter length is 3.80 mm.

Layout Pattern Dependencies in Chemical Mechanical Polishing for Shallow Trench Isolation (STI)

Personnel

D. Ouma, T. Park, and J. Yoon
(D. Boning and J. Chung)

Sponsorship

DARPA, Applied Materials, and
Sandia National Laboratories

Shallow Trench Isolation (STI) is emerging as the isolation methodology of choice as the drive for device density intensifies. However, solution of layout pattern effects at the CMP planarization phase is critical to cost-effective single-mask STI processes. Pattern effects in STI are particularly severe and complex; it is first manifest at the overburden oxide polish phase resulting in a nonuniform time-to-reach the nitride capping layer across the die. This necessitates over polishing to completely remove the oxide and ensure complete nitride stripping. The over-polishing together with higher oxide polish rate results in substantial dishing of the trench oxide in dense trench regions and rounding of silicon nitride around the trenches. In order to control and account for the pattern dependencies, understanding of the polish mechanism in both phases is needed.

The goal of this project is to study and model the pattern dependencies exhibited at the two polish stages. Using a dedicated mask to delineate the specific pattern dependencies, the study will explore a range of polishing process conditions and consumables such as pads and slurries. Different oxide deposition techniques will also be examined; in particular, the oxide topography generated by HDP plasma versus TEOS deposition is important. Model development will begin with extensions to existing oxide polish models to incorporate finite pad bending and explicit quantification of the chemical effect of the slurry. Greater attention will also be paid to hydrodynamic erosion which may play a greater role once the overburden oxide is polished. The end goal is to generate die and wafer-level models applicable to this composite material structure. ❑

Modeling the Effect of Interconnect Variation on Circuit Performance

Personnel

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Sponsorship

DARPA, ARO, PDF Solutions, Intel, and IBM

In order to study the impact of spatial and pattern-dependent variation on circuit performance, CAD tools must be extended and integrated in innovative ways. In this work, we are developing the CAD infrastructure to study device and interconnect variation (both within-wafer and within-die variation) impact on circuit performance. The methodology is also being applied to understand the circuit impact for specific important circuit families such as high speed microprocessors, ASICs, etc.

One such case study is a study of the impact of oxide thickness variation resulting from CMP on circuit performance. A hypothetical chip floorplan is shown in Figure 7 (top), where the goal is to carry the clock signal generated at the center of the chip along the four different paths in such a way that no clock skew results. Unfortunately, the metal clock paths lie over regions of different underlying circuit or metal density. For example, path 1 runs over random logic (with perhaps a 30% density), and then over embedded memory with a higher density of perhaps 50%. Path 3, on the other hand, lies entirely over 30% local density.

This layout density difference will result in non-ideal polishing of the interlevel dielectric between the clock line metal layer and the circuit metal layers, as shown in the lower part of Figure 7. As a result, the ILD thickness along the clock paths, as well as the layer to layer capacitance those paths experience, will be substantially different, as shown in Figure 8 (top). This disparity can be expected to have an impact on the resulting clock skews; as shown in the lower part of Figure 8, for example, the difference between the desired and actual timing for path 3 is about 17% in this example.

In addition to methods for modeling and understanding spatial variation impact on circuit performance, methods are also being explored to reduce that variation. In particular, "dummy fill" methods which insert non-active metal lines or structures in a metal layer have been analyzed, so that the density can be made more uniform at the same time as the capacitance impact is minimized. ❑

Fig. 7: Hypothetical balanced H-bar clock tree floor plan (above); corresponding predicted ILD thickness map (bottom).

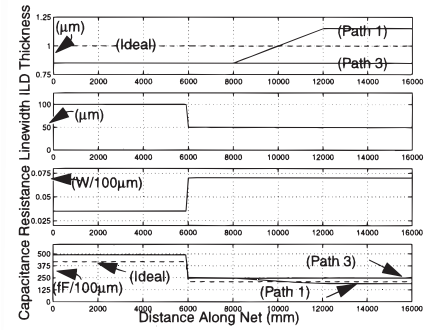

Fig. 8: Resulting ILD thickness and capacitance along clock paths (top); resulting clock skews (below).

Novel Methods for Run by Run Process Control

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Sponsorship
SEMATECH, NSF, and SRC

Novel methods are being explored for the run by run control of semiconductor fabrication processes. In such approaches, periodic recipe modifications from one run to the next are made in order to maintain specified quality, throughput, environmental, and other objectives. Implementation and comparison of an Exponentially Weighted Moving Average (EWMA) controller, a Predictor-Corrector Controller (PCC), and Artificial Neural Network (ANN) controllers have been accomplished. These methods are explored with respect to their stability, responsiveness (optimal or otherwise), ability to incorporate practical issues and their applicability to the CMP, plasma etch, sputter deposition, silicon epitaxy, and other processes. These characteristics have been evaluated through both simulation and control experiments performed on various CMP and etch tools.

Key contributions to run by run control methods have been made in two areas. First, extensions to the run by run controller have been made to address practical issues in dealing with real data in a manufacturing environment. In particular, data that is non-periodic (that is, appears at a random time interval), has missing or intermittent values, and which suffers recurring events (e.g. kit changes) are problematic for many control approaches. These have been addressed in an extension of the EWMA and PCC, and demonstrated for the control of metal sputter deposition.

The second key contribution is the development of a framework for benchmarking of run by run control algorithms and implementations. A network-based interface has been developed that consists of (a) a number of process "simulators" that deal with successively challenging control problems and scenarios (e.g. plasma etch, CMP); (b) a standard message-based interface for candidate external controllers to use to communicate with the benchmark system; and (c) example implementations and interfaces for both C and Java-based run by run controllers. ❑

Run to Run Model Based Process Control on a Dual Coil Transformer Coupled Plasma Etcher

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Sponsorship
SRC and NSF

A novel technique for improving the etching uniformity in a high density polysilicon process has been implemented. Blanket polysilicon on 6 inch wafers are etched in a high density plasma etcher that has been modified to provide a means to control the etching uniformity. The etching is monitored with an *in-situ* Full Wafer Interferometry (FWI) system that provides etching rate information at multiple locations across the wafers. The plasma is also monitored with a multi-fiber optical emission spectrometer. This information is reduced and used by a model based run to run controller to provide recipe advice for the next wafer as to ensure that the polysilicon is etching uniformly across the wafer.

Etching uniformity is adjusted by controlling the power delivered to a dual coil TCP system. Instead of a single inductive coil in a Transformer Coupled Plasma (TCP) etcher, we have installed two concentric independent antennae on a modified Lam TCP. With this geometry, the macroscopic etching uniformity of the wafer can be tailored. By increasing the power delivered to the outer spiral coil in the dual coil system, the etching rate at larger radii is increased, likewise, by increasing the power delivered to the inner coil, the etching rate at smaller radii is increased. Holding other variables such as pressure and gas flow constant, it is possible to find a power setting that will maximize the wafer level etching uniformity. The dual coil TCP provides a means to change the macroscopic etching uniformity. In order to control the etching uniformity in a shifting or a drifting etch process, a means to measure disturbances is needed.

FWI is an *in-situ* diagnostic that provides that capability. The etching rate at many locations across the wafer surface is obtained from the FWI system. A three-level three-variable full factorial experiment allows a response surface mapping of the etch rate at 81 different locations on the wafer to the process variables. A neural network is trained to this data to provide a smooth model that relates the process inputs to the etch rate at various locations across a wafer.

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The neural network model is integrated into an Artificial Neural Network Exponentially Updated Moving Average (EWMA) controller. The EWMA update of the bias layer in the neural network allows for the controller to adapt to process disturbances. Experiments with this configuration shows that the controller can stabilize the etching uniformity and bring the non-uniformity down to less than one percent one sigma STD. To further this work we integrated spatial OES data into the controller. The OES data provides information about the plasma state. This data is reduced by means of Partial Least Squares analysis. A response surface model is built that relates that reduced PLS data to the process parameters. This OES model is then used by the ANN EWMA controller to ensure that the plasma state is similar on a run to run basis, and if it is not, the OES model provides guidance as to which process parameters should be adjusted.

FWI provides information about the wafer state while the spatial OES system provides information about the plasma state. These two diagnostics coupled to the ANN EWMA controller is shown to stabilize disturbances introduced in the etching system. We etch blanket polysilicon wafers and introduce an etching uniformity disrupting shift in the process. The controller is able to respond to the disturbance, and within 3 wafer runs, the product is back within specifications. The ANN EWMA controller with the FWI and spatial OES diagnostics on the dual coil TCP is found to be able to control etching uniformity. Further work is underway to develop and extend the approach for patterned wafer etch uniformity control. ❑

CMP Sensors and Process Control for Reduced Consumption

Personnel

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Sponsorship

NSF/SRC ERC for Environmentally Benign Semiconductor Manufacturing and Texas Instruments

Chemical-mechanical polishing is a process that is still in early adolescence. Despite poor understanding and poor control in the process, it is being widely pressed into service because it is the only process able to deliver the global planarity required in present and future IC technology. The use of CMP is expanding beyond oxide planarization; it is widely used in metal polishing for plug formation, polysilicon polishing for DRAM cell formation, is crucial to device isolation using shallow trenches (STI), and will be essential for future damascene processes. These expanding applications place stress on water and slurry consumption, pad consumption, monitor and look-ahead wafer usage, and generation of waste and potentially hazardous materials. Most CMP process development is currently conducted without consideration of environmental issues. It is the objective of this project to reduce the consumption of slurry, water, and excess wafers. More broadly, the intent is to develop process control and optimization methods that incorporate environmental objectives as a key concern. For example, there is considerable research and development effort in copper damascene metallization approaches; very little attention has been paid to date to the environment issues in copper waste production or other environmental issues in the copper slurries being considered.

The approach being developed in this research is the practical run by run control of the CMP process, through which the process can be optimized for minimal consumption, and the use of monitor and look-ahead wafers eliminated.

One key barrier is the lack of *in-situ* sensors for the measurement of polishing uniformity across the wafer. We are developing an approach to indirectly sense and monitor the uniformity of a wafer being polished *in-situ*. The system incorporates an infrared (IR) sensor which is used to monitor the temperature of the polish pad immediately after it has been in contact with the wafer.

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An IR temperature profile can be obtained by monitoring a series of points corresponding to varying radii along the pad surface. This profile is then analyzed spatially to determine the non-uniformity of the polishing conditions. By understanding the correlation between the pad temperature and the spatial wafer temperature profile during polishing we can predict the nonuniformity of the wafer that has been polished *in-situ* eliminating the need for look- ahead wafers.

Slurry usage during polishing can also be minimized through the usage of this system. The minimum flow rate can be determined by observing the temperature profile during polishing. Initial results using multiple single point measurements show a clear relationship between slurry flow rate and temperature (as well as wafer) uniformity. Work is underway to extend this to simultaneous real-time measurements using an IR camera. In this case, the temperature profile can be fed into a control system to alter the slurry flow during the polish based upon the analysis of this profile. The IR camera provides an exciting opportunity for monitoring of CMP uniformity *in-situ*, which provides the ability to make process adjustments during polishing which can minimize the consumption of slurry and reduce monitor and look-ahead wafer and processing consumption, as well as improve process quality.

In order to overcome other practical barriers to adoption of run by run control for CMP, additional key issues are being examined. First, integration with an in-line film thickness measurement tool (the Nova sensor) is needed. Second, methods for addressing film thickness differences among different products are required. Finally, stable and robust control methods are being applied to achieve reduced wafer consumption, while also addressing practical issues such as missing sample data.

Finally, semi-physical models of the CMP process are being developed. These models can be used to determine the minimal and optimal oxide film deposition thickness needed, together with the minimal polish time, in order to achieve the best within-die planarity results. In addition, these models offer the hope of rapid control adjustments for a large variety of product layouts. ❑

Remote Monitoring and Diagnosis

Personnel

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(D. Boning)

Sponsorship

DARPA, MIT Leaders for Manufacturing, and Ford
(in collaboration with Stanford University)

In billion dollar factories, the penalty for down time for any individual piece of manufacturing equipment is very high, not only in lost production, but also in potentially undetected problems in in-process inventory. Early detection of problems, preferably before they become serious, and rapid response to repair or compensate are a high priority for all manufacturing facilities. The problem is made more complex because the number of machines at any location is typically small and there is little sharing of information between locations, even within the same company. The trend towards increased equipment instrumentation and data collection is pervasive, and applies across a large spectrum of manufacturing domains, including semiconductor, automotive, and other industries. As the amount of information that is gathered during normal operation increases with improved instrumentation, the difficulty of assimilating that information also increases making the problem of detection and diagnosis more difficult.

In this project, we have teamed with Stanford University to examine two key aspects of the problem. First, software and network architectural issues to support and enable remote access and monitoring of advanced equipment and manufacturing lines are being explored. For example, an interesting trend is toward the embedding of ubiquitous network interfaces and real time operating systems (e.g. via variants of Java) on individual pieces of equipment and sensors. Led by Stanford, the team is further exploring the impact of such interfaces on diagnostic system architectures.

One application for monitoring and diagnosis being explored is the detection of pick and place failures in printed circuit board fabrication. Working with Ford, we have been able to identify key opportunities for reducing the volume of scrap chips and the improvement in equipment down time through improved electronic monitoring and diagnosis.

Second, we are developing the algorithmic basis for dealing with the large volumes of manufacturing data that will become available via such interfaces. In particular, "data rich" situations in which hundreds or thousands of time-sampled data streams are available pose interesting challenges and opportunities for monitoring, detection, and diagnosis. We have been exploring variants of multivariate modeling approaches to incorporate the issue of time, including Principal Component Analysis (PCA), Partial Least Squares (PLS), multiway PCA, and other variants.

One particularly exciting application is in the detection of different stages of a complex manufacturing process through multivariate "signature" analysis of the process. In this novel approach, we have applied PCA, but examine both the "loadings" and "scores". That is, we are interested not only in the projection of the data on the eigenvectors of the data, but also on the orientation and directionality of those eigenvectors. The application to low-open area oxide etch endpoint detection in semiconductor manufacturing is being explored. ❑

Architecture for Distributed Design and Fabrication

Personnel
M. McIlrath, D. Boning, and D. Troxel

Sponsorship
DARPA

The design and fabrication of state-of-the-art semiconductor devices and integrated circuits requires an increasingly diverse and expensive set of resources, including manufacturing equipment, people, and computational tools. Advanced semiconductor research activities can be even more demanding, frequently requiring unique equipment and processing capabilities.

We are developing a flexible, distributed system architecture capable of supporting collaborative design and fabrication of semiconductor devices and integrated circuits. Such capabilities are of particular importance in the development of new technologies, where both equipment and expertise are limited. Distributed fabrication enables direct, remote, physical experimentation in the development of leading edge technology, where the necessary manufacturing resources are new, expensive, and scarce. Computational resources, software, processing equipment, and people may all be widely distributed; their effective integration is essential in order to achieve the realization of new technologies for specific product requirements. Our architecture leverages current vendor and consortia developments to define software interfaces and infrastructure based on existing and emerging networking, CIM, and CAD standards. Process engineers and product designers access processing and simulation results through a common interface and collaborate across the distributed manufacturing environment. ❑

Exploring Semiconductor Device Parameter Space using Rapid Analytical Modeling

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Sponsorship
DARPA

The creation and implementation of a semiconductor device parameter space exploration tool has been accomplished which can assist circuit and device designers. Such a tool allows the designer to analyze trade-offs between parameter variations (after defining electrical constraints at the circuit level of abstraction) as well as receive information about feasible device structures. In addition, it is also be possible to compare device parameter variations within a technology family, as well as across different technology families.

The technique of exploring parameter space utilizes a method of rapid analytical modeling to allow for faster, but less accurate, evaluations than one might get through established methods of numerical simulation tools such as MEDICI or PISCES, offering an alternative to such simulators for circuit designers who wish to have rough estimates of parameter variation information, or device structure feasibility. The tool can be a valuable addition to any circuit or device designer's CAD environment. ❑

Modeling of Interconnect Reliability

Personnel
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(C. V. Thompson and D. E. Troxel)

Sponsorship
DARPA

Recent research has demonstrated interconnect failure due to electromigration effect to be strongly dependent not only on current density but also on metal film crystal grain size distribution and geometries of interconnect patterns. This type of failure is manifest as a depletion of interconnect metal forming a "void" (open-circuit) or an accumulation possibly forming a "short" to neighboring interconnect.

Our research work focuses on:

i) developing abstract, physically-based, micro-structural interconnect failure models to more accurately predict electromigration induced failure.

ii) ERNI (Electromigration Reliability for Network Interconnect) our prototype computer-aided design tool based on these abstracted micro-structurally based models.

A release of ERNI 2.0 is expected during Spring 1998 with extensions supporting hierarchical designs and utilizing higher-performance circuit simulation engines. This release will incorporate client and server programs implemented in Java. With this, multiple designers at different locations will be able to cooperatively design integrated circuitry which incorporates electromigration reliability models. ❑

Distributed Process Control Architecture

Personnel
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Sponsorship
DARPA and Stanford University

Semiconductor fabrication requires an increasingly expensive and integrated set of tightly controlled processes, driving the need for a fabrication facility with fully computerized, networked processing equipment. We have designed an integrated, open system architecture enabling distributed experimentation and process control for plasma etching. The system was developed at MIT's Microsystems Technology Laboratories and employs *in-situ* CCD interferometry based analysis in the sensor-feedback control of an Applied Materials Precision 5000 Plasma Etcher (AME5000). Our system supports accelerated, advanced research involving feedback control algorithms, and includes a distributed interface that utilizes the internet to make these fabrication capabilities available to remote users.

The system architecture is both distributed and modular: specific implementation of any one task does not restrict the implementation of another. The low level architectural components include a host controller that communicates with the AME5000 equipment via SECS-II, and a host controller for the acquisition and analysis of the CCD sensor images. A Cell Controller (CC) manages communications between these equipment and sensor controllers. The CC is also responsible for process control decisions; algorithmic controllers may be integrated locally or via remote communications. Finally, a System Server manages connections from internet/intranet (web) based clients and uses a direct link with the CC to access the system. Each component communicates via a predefined set of TCP/IP socket based messages. This flexible architecture makes integration easier and more robust, and enables separate software components to run on the same or different computers independent of hardware or software platform. ❑

Remote Microscope for Collaborative Inspection of Integrated Circuits

Personnel

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Sponsorship

DARPA

The internet remote microscope was developed to enable users to inspect a microscope specimen remotely by using an ordinary workstation computer connected to the internet. The remote microscope is a distributed system that consists of one or more graphical client interfaces that communicate over the internet with a microscope server unit consisting of hardware and software needed to automatically control an inspection microscope. The client interface presents the user with a graphical microscope control panel and two image panels that show static images of the microscope specimen that can be updated upon request. Because it is not important to have live video when examining many types of specimens, especially in the context of inert semiconductor wafers, this approach gives acceptable performance while requiring only limited bandwidth. From the control or instrumentation panel, the user may select a new magnification, pan position, and focus setting (manual or automatic), and can then instruct the system to capture a new image at the specified coordinates. The new image can be placed in one of the two arbitrary display windows, allowing the user to keep a previous image for reference. Typically, one would actually use one window to show a global or panoramic view of the specimen at low magnification, while using the other window to show a more detailed region of interest at high magnification. The server system consists of a Zeiss microscope, an automated stage accurate to 0.4 μm for X-Y translation and 0.1 μm for Z direction, a video camera, and an ordinary personal computer running OS/2 that services requests over the internet from clients. The PC contains a framegrabber board that can capture an ordinary NTSC video signal from a CCD camera that is mounted on top of the microscope, and the PC is also responsible for controlling the stage, turret, and focus settings for an automated Zeiss microscope. Except for the initial placement of a wafer on the stage, this system is fully automated and controllable from the client control panel. Essentially, the remote microscope allows distant users to access and view a specimen remotely as if they were controlling the microscope themselves. An additional capability of the internet remote microscope is that multiple clients can view the microscope simultaneously during a conference inspection mode. This enables any number of experts anywhere on the internet to simultaneously view the microscope images collaboratively, although only one person at a time is in control and allowed to change the system settings.

Users use the remote microscope by retrieving the client applet from a web server, residing on the same system as the remote microscope server application. This design has made the client program platform independent, allowing the use of the client on any machine which supports Java applets. The Java client currently includes all the functionality of the original client, as well as many of the new manual focusing options currently being designed.

New features added include a text chat tool, online help files, a mini tools window, and a layout based navigation tool. The text based chat tool allows users to send small text messages to one another, while inspecting a wafer. The online help contains a complete users guide, trouble shooting tips, and other remote microscope related material. These help files will be directly available through the web server. The mini tools window allows for quick zoom, move, and grab commands, as well as including some measurement functions. A Java based MAGIC file viewer in our group serves as the basis for an easy and quick navigation tool. ❑

Semiconductor Process Repository

Personnel

M. Verminski and W. Moyne,
(M. McIlrath and D. E. Troxel)

Sponsorship

DARPA

The goal of this research task is to create a system to facilitate distributed process research and design. Such a system will allow users to retrieve and examine process flows from multiple process libraries across the network.

Work has proceeded on the design and development of a distributed process repository interface. The repository Application Programming Interface (API) is encapsulated by an OMG CORBA distributed object model and defined by an Interface Description Language (IDL) specification. The process object model used to encapsulate the process repository API is based on the Semiconductor Process Representation (SPR) Information Model. The IDL specification is programming language-neutral; application clients and repository services may be implemented in any language supported by a CORBA-compliant Object Request Broker (ORB) and interoperate across a local or wide-area network. Process repositories may be distributed; process objects and services may be located at various sites transparently to application clients. Applications and services may interoperate using entirely distinct ORB implementations if a common protocol such as the Internet InterORB Protocol (IIOP) or appropriate bridges are available.

The present SPR IDL development includes the Base Information Model. This standard process representation interface provides a common facility to communicate fabrication processes. The fabrication process information organizes processes into smaller subprocesses. At each level, the process can be described from different views. These include the 'effect' of a process on the wafer, the 'environment' around the wafer during the process, and the 'equipment' settings during the process. Each view contains parameters that describe some aspect of the wafer, environment, or equipment during some interval of time. Dynamic attributes (property lists) are also supported for maximum extensibility. The base SPR IDL has been extended to include specific effects and parameters with statistical information.

Two SPR-based repository implementations are in progress. One uses the Xerox InterLanguage Unification (ILU) ORB to provide an SPR wrapper to processes in the MIT CAFE CIM system used by the Microsystems Technology Laboratories. Repository object implementations are built directly on the CAFE GESTALT object oriented programming layer. This repository implementation now integrates IIOP directly, supporting operation with clients using heterogeneous ORBs without the need for the request-level bridging employed earlier.

A distributed software architecture for semiconductor process design has been defined and implemented in Java with the OrbixWeb Object Request Broker (ORB). The implementation communicates with any ORB adhering to the Internet Inter-ORB Protocol (IIOP). A persistent storage mechanism has been implemented using Object Design ObjectStore PSE (Persistent Storage Engine) for Java.

Other services to manage, query and find distributed objects are being developed. Their interfaces are based upon the Object Management Group's (OMG) CORBA services specifications. A Life Cycle service for creating, deleting, copying, and moving distributed objects has been developed. Work has begun on implementing a Query service and a Trader service. Together, the services will be essential for the development of distributed and shared applications for semiconductor process research and design.

We have also been collaborating with the Sematech CIM Framework project in the areas of Specification Management and CIM Architecture. This work is also CORBA IDL-based and we are investigating the possibilities for interoperation of these environments. ❑

Labnet Software

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Sponsorship
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University microfabrication laboratories are facing many new challenges and opportunities: facilities are becoming more expensive and difficult to manage; resources and expertise need to be shared and made available to a wider community; education and research are becoming more dependent on multi-institutional collaboration. Given the above challenges, there is a growing desire for a new distributed information infrastructure, that will allow remote collaboration, access to remote sites' data and sharing of end-user software applications, in the face of differences between remote sites in computer platforms, operating systems, and technical resources. Past research has been done within this application domain but most working systems are too tightly coupled to their local facilities, suffer from portability problems and have never addressed the issue of data distribution and remote site interaction.

The Labnet Software Project was initiated in recognition of a need for universities to share the development and support effort needed to develop and maintain new distributed laboratory information systems. Joint development work was initiated between MIT, Stanford University and the University of California at Berkeley to:

- Assess the applicability of emerging technologies such as the Object Management Group's (OMG) Common Object Request Broker Architecture (CORBA), OMG's Interface Definition Language (IDL), Sun Microsystem's Java language, and object databases.
- Explore infrastructure to enable collaborative distributed design and fabrication (including object-oriented distributed programming interfaces and web-based user interface capability).
- Develop abstract specifications of programming interfaces to both data and services.
- Explore standards to achieve software compatibility such as the Sematech CIM Application Framework.

In the last year, substantial progress has been made in developing a prototype distributed reservation system. The system utilizes a Java user interface which enables the reservation module to run on standard web browser clients anywhere on the network. On the back end, information is managed through JDBC database connectivity. The system is now being used to gain user feedback, as well as to evaluate implementation options and architecture decisions. ❑