# Environmentally Benign Process Chemistries and Chemical Recycling


## Personnel

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## Sponsorship

NSF/SRC Center for Environmentally Benign Semiconductor Manufacturing and Wafer Engineering and Defect Science Consortium


In today's silicon electronics, control of the surface properties of the starting material, crystalline silicon, is essential for achieving a high process yield for devices with submicron dimensions. While wet cleaning cycles continue to be used widely in IC processing because of their excellent ability to remove particles and native oxides, environmental concerns will restrict the use of chemicals employed in these cleaning processes. It is, therefore, necessary to develop new cleaning processes by understanding the surface chemistries and, based on this knowledge, develop and evaluate alternative chemistries. We have developed a contactless monitoring tool based on the measurement of minority carrier lifetime which is capable of detecting very low levels ($10^8$ atoms/$cm^2$, or ppm surface states) of surface defects on high quality silicon wafers. This Radio-Frequency PhotoConductance Decay (RF-PCD) measurement detects any contaminants that generate mid-gap electronic states, including Si dangling bonds and metal adsorbates.

We have developed a new cleaning process using iodine dissolved in alcohol to replace dilute HF as a final cleaning step prior to gate oxidation or epilayer growth. In collaboration with a group in the Department of Chemistry at Stanford University, we have determined that iodine radicals catalyze bonding between surface silicon atoms and oxygen atoms of the alcohol. Further studies have shown the stability of this passivation in air to be superior to the stability of conventional dilute HydroFluoric acid (HF) passivation. We are currently investigating the impact iodine/alcohol passivation has on Gate Oxide Integrity (GOI).

We have studied the processes by which metals in solution contaminate the silicon surface. We have used RF-PCD on a silicon monitor wafer to detect *in-situ* metal contamination in a cleaning bath. Figure 1 shows the monitor response to 1 - 5 ppb of Cu in a 5% HF solution. This monitor is part of point-of-use HF recycling system designed with our collaborators at Millipore Corporation. ❑

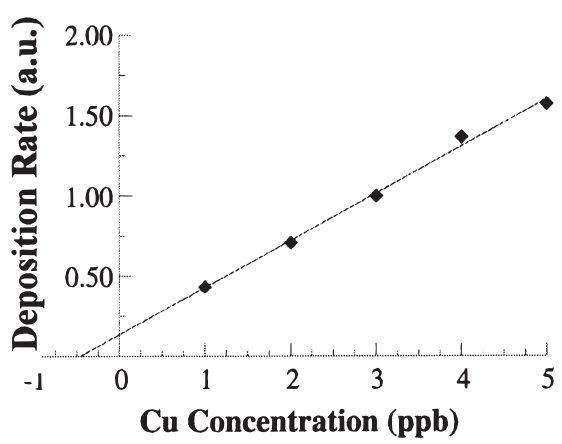


*Fig. 1*

# Alternative Chemistries for Wafer Patterning and PECVD Chamber Cleaning


## Personnel

S. Karecki and L. Pruette
(R. Reif)



## Sponsorship

NSF/SRC Engineering Research Center for Environmentally Benign Semiconductor Manufacturing


Gases such as fully fluorinated alkanes - $CF_4$, $C_2F_6$, $C_3F_8$ - as well as inorganic compounds like $NF_3$ and $SF_6$, collectively termed as PerFluoroCompounds (PFCs), are used heavily by the semiconductor industry for the etching of dielectric films in wafer patterning and Plasma-Enhanced Chemical Vapor Deposition (PECVD) chamber cleaning applications. Their use and emission is problematic, however, from an environmental standpoint because of the global warming nature of these substances. Relative to $CO_2$, the most commonly emitted global warming gas, PFCs have Global Warming Potentials (GWPs) three or four orders of magnitude larger. Moreover, they tend to have atmospheric lifetimes of thousands to tens of thousands of years. The principal options presently being pursued by the semiconductor industry in an effort to reduce PFC emissions are process optimization, abatement technologies, recovery systems, and the use of alternative chemistries.

Work is being carried out at MIT's Microsystems Technology Laboratories to identify and develop alternative dielectric etch chemistries to be used in wafer patterning and PECVD chamber cleaning processes. A large pool of candidate chemistries was initially drawn up. Molecular structure and environmental, safety, and health considerations were used as the selection criteria.

### *Earlier Work*

In earlier stages of this project, etch viability tests were carried out with a number of chemistries belonging to the hydrofluorocarbon (HFC) and iodofluorocarbon (IFC) families, as well as with trifluoroacetic anhydride (TFAA). In 1997, etch viability tests with two additional IFC chemistries (1-iodoheptafluoropropane and iodotrifluoroethylene) were completed. As Table I indicates, this preliminary work was performed on an Applied Materials Precision 5000 etch tool housed at MIT. Since this time, actual chamber clean and etch process tests were performed with the most promising candidates identified so far, all in collaboration with semiconductor companies and/or equipment manufacturers.

| Compound | $GWP_{100}$ | Atm. Lifetime (yrs.) | Viability Tests (AMAT Precision 5000 Mk II) | Etch Process Tests (AMAT Centura 5300 HDP) | Chamber Clean Tests (Novellus Concept One 200) |
|---|---|---|---|---|---|
| 1H-heptafluoropropane | ~5000 | 132 | X | | |
| 2H-heptafluoropropane | 2900 | 36.5 | X | X | |
| Pentafluoroethane | 2800 | 32.6 | X | | |
| 1,1,1,2-Tetrafluoroethane | 1300 | 14.6 | X | | |
| Trifluoroethylene | N/A | N/A | X | | |
| Difluoromethane | 650 | 5.6 | X | | |
| Trifluoroacetic anhydride | negl. | negl. | X | | X |
| Iodotrifluoromethane | <1 | <0.005 | X | X | |
| Iodopentafluoroethane | negl. | negl. | X | | |
| 1-iodoheptafluoropropane | negl. | negl. | X | X | |
| 2-iodoheptafluoropropane | negl. | negl. | X | X | |
| Iodotrifluoroethylene | negl. | negl. | X | | |
| Dilute $NF_3$ | 8100 | 740 | | | X |

a Estimated source [1]
b source [2]
c source [3]

*Table I: Compounds evaluated to date.*

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## *High Density Plasma Etch Studies*

Data generated in the earlier etch viability studies was used to select four compounds for further testing in collaboration with Motorola's Advanced Products Research and Development Laboratory (APRDL): 2H-heptafluoropropane, iodotrifluoromethane, 1-iodoheptafluoropropane, and 2-iodoheptafluoropropane. Designed experiments were used to evaluate both etch performance and emissions. The test vehicle used for processes developed in this work was a high aspect ratio TEOS via etch application. Via holes with nominal printed dimensions down to 0.35 μm were etched. The process tool used for this study was a high density plasma etch tool - an Applied Materials Centura 5300 platform equipped with HDP etch chambers.

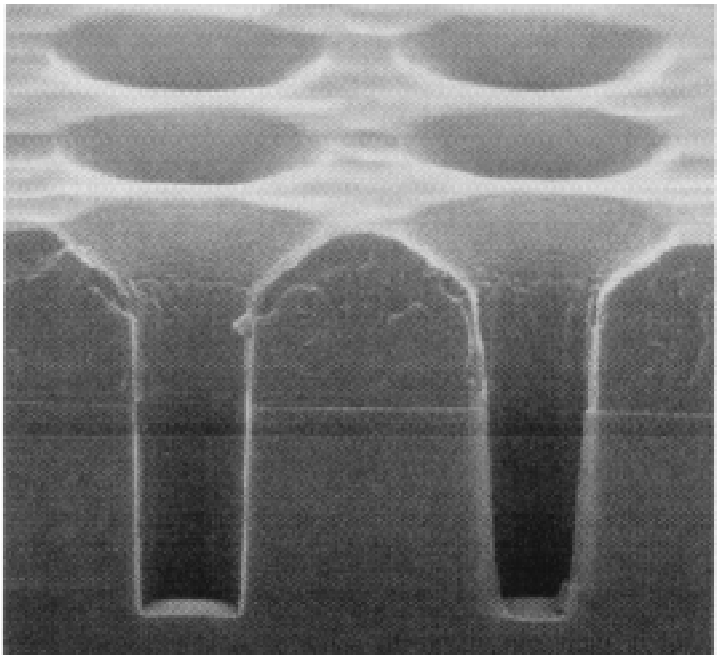

*Fig. 2: Array of 0.6 μm (nominal printed CD) vias etched with a 2H-heptafluoropropane process.*

Of the four gases studied, all gases were found to have promising results in terms of emissions reductions. However, from a process standpoint, the use of iodotrifluoromethane was found to be problematic. On the other hand, encouraging results were achieved with 2H-heptafluoropropane and the iodoheptafluoropropanes from both emissions and process (see Figure 2) standpoints. Emissions reductions ranging from ~60% for 2H-heptafluoropropane to ~95% for 1-iodoheptafluoropropane (vs a $C_3F_8$-based reference via etch process) were attained for the processes studied. Follow up studies involving the development of a process for an HDP via etch application based on 2H-heptafluoropropane as well as an isomer of iodoheptafluoropropane have already been initiated; further work is scheduled to take place in the near future, once again in collaboration with Motorola.

## *Chamber Clean Studies*

In the course of the last year, two chemistries have also been evaluated as etch gases in a dielectric PECVD chamber clean application – trifluoroacetic anhydride (TFAA) and dilute $NF_3$. Both projects were also collaborative efforts between MIT and industrial partners: the former involving Air Products and Chemicals and Novellus Systems, whereas the latter, a follow up effort to initial work carried out by IBM, involved IBM and again Novellus Systems as well as Air Products. A Novellus Concept One 200 dielectric PECVD tool housed at MIT running a silane oxide process was used for the experiments.

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In the TFAA study, emissions reductions on the order of 25X relative to a standard $C_2F_6$ process (and up to 8X relative to an experimentally optimized $C_2F_6$ process) were attained. TFAA was found to be effective as a chamber clean gas in the Concept One tool, however, some difficulties, stemming from the high boiling point of the compound, were experienced when delivering the high gas flows required. In the $NF_3$ experiments, $NF_3$ was combined with a diluent gas as a chamber clean chemistry. A substantial improvement in process emissions (over 90% vs a standard $C_2F_6$ process) was found to be achievable, in conjunction with a decrease in chamber clean time. The principal difficulty that was experienced in these experiments was maintaining the stability of the electronegative $NF_3$ plasma under certain experimental conditions. However, the results were sufficiently encouraging to warrant further development of clean processes based on this chemistry. This work is presently taking place at Novellus Systems and is scheduled to be completed by mid-1998.

In the course of this project, a number of fluorinated compounds have been screened and evaluated as potential replacements for PFCs in dielectric etch and clean applications. In wafer patterning applications, several of these, namely 2H-heptafluoropropane, as well as 1- and 2-iodoheptafluoropropane, have been found to be particularly promising, based on the data available so far. In chamber clean applications, one very attractive candidate appears to be dilute $NF_3$. Further work is planned to follow up on the results obtained to date. It is the investigators' desire to produce a body of work which will be directly usable by semiconductor tool vendors and IC manufacturers and to work in collaboration with IC manufacturers as well as tool vendors toward that end. ❑

# Pattern Dependencies in Copper Damascene CMP Processes

## Personnel

T. Park and T. Tugbawa
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## Sponsorship

DARPA and SEMATECH

Copper, due to its lower resistivity and higher melting point (higher electromigration resistance) compared to aluminum, is the choice of metal for next generation VLSI interconnect. Unlike aluminum, there is no viable means of patterning and etching copper. Consequently, one has to resort to a damascene processes and use Chemical Mechanical Polishing (CMP) for planarization, thereby accurately defining the copper lines in the trenches. Copper damascene CMP processes are now in the development phase in industry to resolve various issues such as process integration, reliability, defect, and yield.

The goal of this project is two fold. First, we want to characterize, understand, and model pattern dependencies of density and pitch in copper damascene CMP processes using both conventional $SiO_2$ and low-k dielectrics. These pattern dependent issues include dishing of copper and erosion of oxide, interaction range (planarization length), edge rounding of copper lines which are illustrated in Figure 3, as well as yield issues of line continuity and shorting. The characterization mask set used in this study is a single level mask that contains primarily density structures, pitch structures, serpentine/comb yield structures, and oxide-fill structures as shown in Figure 4. It is designed for both electrical characterization and physical characterization. The pitch structures are simply vertical lines with pitch in the range 0.5 μm - 500 μm (pitch is copper line width plus oxide spacing), at a constant pattern density (pattern density is metal line width divided by pitch) of 0.5. The density structures are vertical lines with different pitch values, and the pattern density ranges from 0.10 to 0.90. The oxide-fill structures are bond pads with oxide pillars of different sizes and patterns embedded in them.

Second, we want to fully understand and model multilayer effects such as propagation of pattern dependencies from metal one to metal two, and polishing dependencies of metal two on metal one topographies. The

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development of such a model will greatly facilitate the full development of multi-layer copper interconnects. In the second phase of this work, two and three-layer tests masks are being developed. In the new two-level masks (with SEMATECH), we are interested in understanding the impact of underlying topography on the patterning and polishing of second level copper lines. In the three-level masks (with Rockwell), we are also interested in the impact of topography and pattern dependencies on via formation and reliability. ❑

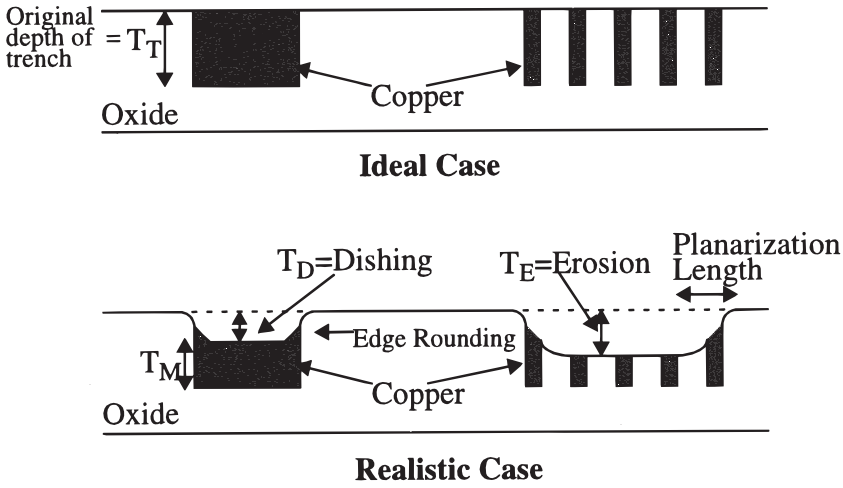


*Fig. 3: Ideal case vs. dishing and erosion in realistic copper polishing.*

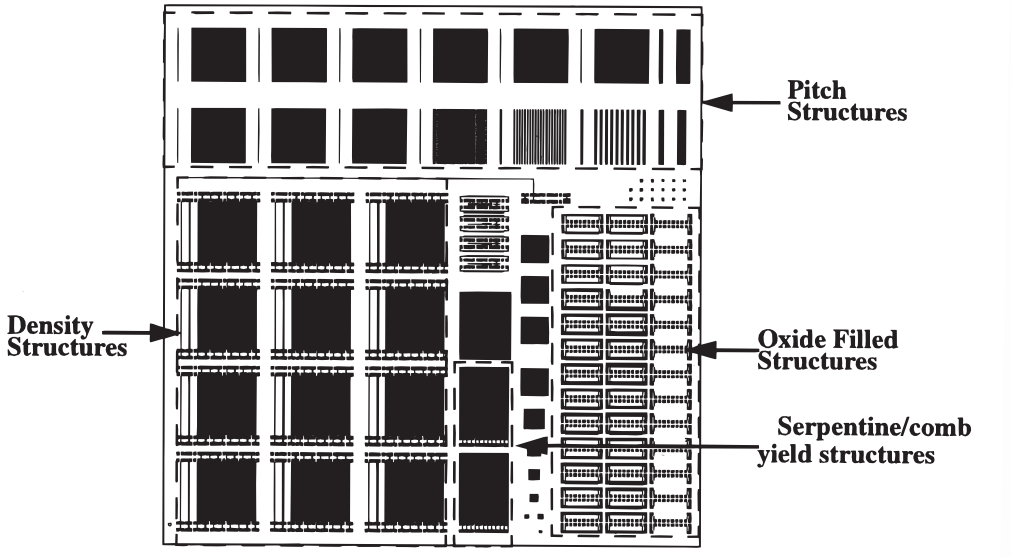


*Fig. 4: Copper Damascene CMP Characterization Mask (single layer).*

# Aligned, Selective-Area Wafer-Scale Bonding of Optoelectronic Devices on GaAs Integrated Circuits

## Personnel

D. Crankshaw
(C. G. Fonstad, Jr.)

## Sponsorship

NSF, Lockheed Martin

The purpose of the OPTOCHIP project is to create optical devices on commercially fabricated electronics. The electronics portion of the chip is processed out-of-house by Vitesse, leaving wells open for the devices, either LEDs or VCSELs. Previous work has successfully produced LEDs inside of these wells by MBE growth. VCSELs, however, are more challenging, requiring higher quality than the LEDs. Wafer bonding offers an alternative method. Wafer bonding is the method of attaching two semiconductor wafers face-to-face, so that they may be considered one wafer. Using this technique, the lasers can be grown in bulk on a separate substrate, then processed into pillars to fit inside the wells. The pillars may then be bonded into the wells and separated from the original substrate.

Some of the common bonding methods in use are Epitaxial Lift Off (ELO), Palladium bonding, and wafer fusion. The most attractive is wafer fusion. Wafer fusion uses heat and pressure to bond the wafers, creating covalent bonds between the atoms of the two semiconductors. This gives the best optical properties, as well as excellent mechanical and electrical properties.

One of the unique aspects of this research is that the bonding is done over a very small area. Wafer bonding is generally done over the relatively large area ranging from a 20 $mm^2$ chip to a full wafer. This project requires the fabrication of pillars on these chips of areas around 10 to a 100 μm in width. This structure and the extraordinarily small area raises some unique problems. First, the small area can make it difficult to accurately apply a force which corresponds to an appropriate pressure. This can mean that extraordinary pressure is applied to the surface, possibly causing damage. Added to this is mass transport, the diffusion associated with mobile atoms of Group III elements at elevated temperature. Deformations in the structures have been observed, most likely due to these factors, but they are small compared to the scale of the features and unlikely to cause difficulty.

Another unique feature of this research is the requirement that the two wafers be aligned prior to fusion. The pillars must be aligned with the wells before the wafers are placed together and subsequently fused. This project seeks to demonstrate that alignment of III-V materials is possible using the same infrared alignment techniques used to align silicon wafers for bonding. ❑

# Hyperthermal Molecular Beam Dry Etching of III-V Compound Semiconductors

## Personnel

I. Hoshino
(C. G. Fonstad, Jr.)

## Sponsorship

JSEP/RLE and DARPA/NCIPT

A novel Ultra-High Vacuum (UHV) compatible etch reactor has been designed, constructed, and characterized. The etch mechanism is dependent solely on the chemical reactivity of the neutral etchant gas, enhanced by its kinetic energy, and does not utilize any plasma or ion source in obtaining directionality or acceleration. As described in a recently completed Ph.D. thesis, this work also reported the first demonstration of molecular chlorine etching of InP, this being done at chlorine pressures of $1 \times 10^{-7}$ Torr with no ion, plasma, or e-beam assistance. It is expected that this etching technique will introduce very little damage in specimens, unlike the situation with ion-beam and plasma techniques.

The etchant gas in the present system is accelerated to supersonic speeds through the use of a free-jet expansion nozzle, skimmer, and differentially-pumped vacuum chamber. By varying the nozzle temperature and the concentration of chlorine in the gas matrix, the energy of the incident beam can be varied. The directionality of the molecular beam produced is maintained by using it in a UHV environment with background operating pressures of $1 \times 10^{-7}$ Torr, or less. Since the translationally-activated molecules contribute to collision-induced dissociative chemisorption, a chemical reaction can be initiated in this way in an otherwise unreactive material system.

Both indium phosphide and gallium arsenide were etched using a translationally-activated molecular chlorine beam. Both directional and (111) crystallographically-preferential etch profiles were observed. The preferential etch was found to be the predominant etch profile at low beam energies, while directional etching was achieved when the beam energy was increased. Etch rates ranging from 0.2 μm per hour to 2.0 μm per hour were obtained at substrate temperatures ranging from 200° C to 350° C under various beam conditions.

Two quantitative *in-situ* process monitoring methods were also devised for this work: (1) a surface roughness measurement method which uses the reflected intensity of a 633 nm He-Ne laser beam, and (2) a technique for calibrating the substrate holder thermocouple at low-temperature which is based on monitoring the vacuum background pressure during the initial stages of the substrate temperature ramp.

It was found that under certain etch conditions an aluminum compound was deposited on the specimens which subsequently interfered with the etch process, thereby limiting the range of parameters and conditions which could be investigated. Subsequent study revealed that the source of the deposit was an aluminum ring holding the skimmer in position. This ring has recently been replaced. Funds are presently being sought to continue the development and application of this etch tool. ❑

# Si-on-GaAs: Monolithic Heterogeneous Integration of Si CMOS with GaAs Optoelectronic Devices using EoE, SOI, and MEMS Techniques

## Personnel

J. London and J. Ahadian
(C. G. Fonstad, Jr. and J. Mikkelson)

## Sponsorship

DARPA and General Motors Fellowship

As electronic technology becomes faster and denser, electrical interconnects (wires) have begun to limit the performance of the systems that depend on them. In order to alleviate this problem, optical interconnects are being considered as an alternative. Some of the benefits of optical interconnects include higher speeds of operation with low drive requirements and minimal power dissipation; reduced size, weight, and cost; freedom from electromagnetic interference, crosstalk, and eavesdropping; and ease of layout and routing.

In order to implement optical interconnects, OptoElectronic Integrated Circuits (OEICs), which integrate both electrical device (transistors) with optical devices (optical detectors and emitters), must be created. Silicon is the dominant material used in electronic integrated circuits such as digital signal processors, microcomputers, and memory. However, due to the intrinsic structure of silicon, this material is not capable of emitting light efficiently. Compound semiconductors such as gallium arsenide, on the other hand, can be used to make light emitting devices such as light emitting diodes and lasers. Engineers have been trying without success for some time to develop the technology that would support the monolithic integration of these two types of semiconductors.

A new technology has been proposed by our group at MIT which will combine silicon and gallium arsenide substrates by wafer bonding. This process builds upon pre-existing expertise at MIT in the area of wafer bonding silicon substrates. Yet, due to the vastly different composition of gallium arsenide, this process will have to be significantly modified in order to result in success.

Two other technologies, which have been studied at MIT, are Silicon On Insulator MOS technology (SOI) and Epitaxy on Electronics (EoE). SOI is a method of fabricating CMOS transistors in a thin layer of silicon, which is separated from the silicon substrate, by an insulating layer of silicon dioxide. SOI has become important recently because this process is able to significantly reduce stray capacitances, and this will ultimately lead to higher performance devices. EoE, which is described in more detail elsewhere in this report, is a technology in which optoelectronic devices are monolithically integrated with gallium arsenide electronics by growing optoelectronic device heterostructures epitaxially directly on fully processed integrated circuits. The EoE technology has been perfected using electronic devices made in gallium arsenide, yet, in order to obtain wide scale acceptance in industry, silicon electronics must be used instead. This will now become possible by combing wafer bonding, SOI, and EoE techniques.

Once the silicon and gallium arsenide are bonded, electrical devices will be fabricated in the silicon. Windows will be etched through the silicon to the underlying gallium arsenide so that optical device heterostructures can be grown following standard EoE techniques.

Wafer bonding, SOI, and EoE will allow us to overcome the previously insurmountable problems caused by the large thermal expansion coefficient mismatches and lattice mismatches between silicon and the compound semiconductors. By taking advantage of these recently developed techniques, it will now be possible to monolithically integrate state-of-the-art silicon CMOS electronics and high performance III-V optoelectronics devices producing OEICs of unprecedented complexity and performance. The successful demonstration of this technology will have significant technological and economic ramifications, and will make practical many applications of optical interconnects that have long been anticipated, but have yet to be realized. ❑

# A Fully-Passivated, Low-Temperature Process for Reliability Studies of InP-Based HEMTs

## Personnel

R. R. Blanchard
(J. A. del Alamo)

## Sponsorship

Lockheed-Martin

InP technology is emerging as the most promising technology for millimeter-wave communications applications, with a record $f_t$ and $f_{max}$ of 340 GHz and 600 GHz respectively. This is a direct result of the excellent properties of the InAlAs/InGaAs heterostrucuture system. However, very little work has been done on the reliability of InP-based High Electron Mobility Transistors (HEMTs), and an understanding of the physical mechanisms responsible for device degradation is still lacking. This understanding is essential to the development of lifetime-prediction models. The small band gap of the InGaAs channel results in significant impact ionization at even moderate current levels, affecting hot carrier reliability. In addition, exposure to hydrogen at elevated temperature with a partial pressure as low as 2-3 torr produces threshold voltage shifts. This low level of hydrogen is comparable to the ambient created in a sealed package as a result of hydrogen out-gassing from the package.

In order to address these and other reliability questions, we have developed an industry-compatible process which allows us to examine the detailed physics of degradation using specialized test structures developed at MIT. The process developed for this project is comparable to state-of-the-art industrial processes, with the exception of an optical photolithography gate technology. Key features include a fully-selective gate recess, side-wall recessed channel, ECR-RIE mesa etch, and a low-temperature, low-stress ECR-PECVD $Si_3N_4$ passivation. This process has been successfully demonstrated on a 0.8 μm double-heterostructure InP HEMT (shown in Figure 5), producing a peak transconductance of 600 mS/mm, a maximum drain current of 620 mA/mm and a breakdown voltage of 6.7V.

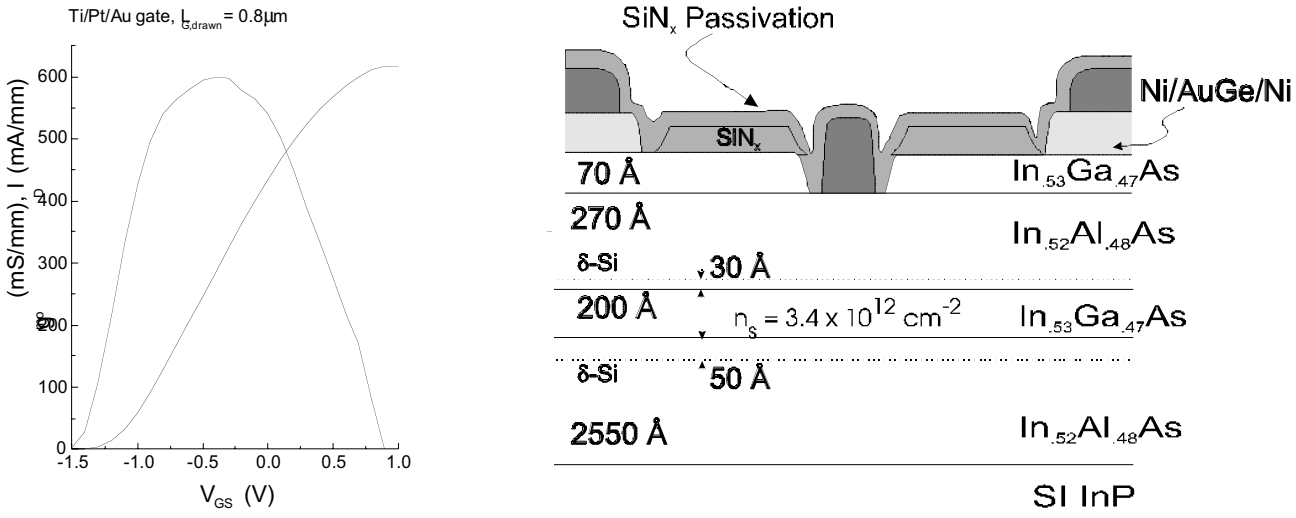


*Fig. 4: Transfer characteristic of the InAlAs/InGaAs HEMT shown in inset. This device was fabricated with the low-temperature, fully-passivated InP-based HEMT process developed at MTL.*

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Studies are underway to examine the issue of hydrogen poisoning in InP HEMTs. For this study, measurements of MIT fabricated devices have been used to corroborate measurements of unpassivated 0.15 μm state-of-the-art devices fabricated by industrial partners. The key results from this work indicate that a thermal effect results in gate sinking and an increase in the Schottky barrier height, producing a positive $V_t$ shift in devices annealed in $N_2$. Slightly less $V_t$ shift is observed for devices annealed in forming gas (5% $H_2$). To separate the thermal effects from hydrogen effects, similar anneals were performed on devices that had already undergone a high temperature $N_2$ anneal. While the subsequent $N_2$ anneals produce no change in device characteristics, the additional forming gas anneal results in a negative $V_t$ shift. Future work will focus on determining the relative time scales of the thermal and hydrogen related effects, identifying how hydrogen produces this $V_t$ shift, and investigating the role that silicon nitride passivation may play in preventing or accelerating device degradation. ❑

# SiGe Heterostructure Technology for Low-Power CMOS

## Personnel

M. A. Armstrong
(K. Ismail - IBM and D. A. Antoniadis)

## Sponsorship

ARPA and IBM Fellowship

As conventional MOSFET scaling becomes more and more difficult to continue, alternative methods of improving device performance are becoming more attractive. One such technique is to increase the effective mobility in the channel through the use of epitaxially-grown SiGe substrates. The effective mobility in contemporary sub-micron MOSFETs is typically 350 $cm^2/Vs$ for electrons and 90 $cm^2/Vs$ for holes. These numbers improve to 2500 for electrons and 800 for holes in SiGe strained-layer heterostructures.

We have used a two-dimensional poisson, continuity and energy balance equation solver (MEDICI) which takes into account the combined effects of series resistance, charge sharing, velocity saturation and velocity overshoot to study the characteristics of heterostructure-containing MOSFETs with 0.2 μm effective channel length. The channel structure of the simulated devices allows for both an electron channel and a hole channel in the same heterostructure.

The simulations predict an increase in saturated current drive of 125% in the n-MOSFET and 23% in the p-MOSFET over state-of-the-art numbers for 1.5 V supply voltage. The average carrier velocity in the channel is significantly higher in SiGe devices as compared to bulk silicon devices. When the devices are operated at lower supply voltages, the effects of velocity saturation are reduced, and the relative improvement of SiGe over Si devices is increased. This indicates the utility of SiGe devices for low power applications.

At this point in time, one of the main technological hurdles to the integration of SiGe heterostructures into mainstream CMOS is the limitation on thermal budget. Conventional silicon device fabrication involves high temperatures (greater than 1000° C) during such steps as gate oxidation and source/drain implant annealing. However, strained-layer heterostructures can withstand only limited thermal cycles (less than 600° C) so as to

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preserve the high-mobility properties of the epitaxially-grown substrate. Excessive thermal energy will relax the pseudomorphically-strained layers and diffuse the sharply defined heterostructure. As the strain decreases and the carriers become less well confined, the mobility drops rapidly. This work addresses these and other issues with the goal of demonstrating a high-mobility device. ❑

# Electron Beam Focusing for Field Emission Displays

## Personnel

L. Dvorson
(A. I. Akinwande)

## Sponsorship

DARPA

Field emission devices are a promising technology for Flat Panel Displays. Like a CRT, a Field Emission Display (FED) is an *emissive* display; thus, its luminous efficiency, brightness, and viewing angle characteristics are superior to transmission-based displays, such as LCDs. Unlike a CRT, which contains a single electron gun that is scanned across the display, an FED is based on an addressable array of mini electron guns. This produces a thin and compact display suitable for use in portable technologies. A typical FED consists of a base plate containing the addressable electron guns, and a phosphor coated screen; the screen and the base are separated by insulating spacers.

In today's FEDs there exists a trade-off between luminous efficiency and display resolution. *Proximity focused* FEDs use a low voltage phosphor screen separated from the base by a thin (~ 0.3 mm) spacer. Although this allows a small pixel size, and, hence, a high resolution display, the thin spacers can easily break down due to high anode voltages. Thus, a proximity focused display requires the use of low voltage phosphors, which have a lower luminous efficiency than high voltage, CRT-type phosphors. To use a high voltage phosphor screen, it is necessary to increase the base to screen separation to prevent the spacers from suffering dielectric breakdown. Since the electron beam produced by the field emitters has a certain angular spread, the lateral extent of the beam increases with the distance from the emitter. Thus, a high voltage screen would have a larger pixel size and, hence, lower resolution. The goal of the present project is to overcome this trade-off by using a high voltage phosphor screen and *electrostatically focusing the electron beam*. The focusing electrodes and the emitting structures are to be integrated on the same substrate and fabricated in a single process.

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The basic structure for our 3D model of a self-focused field emission tip is shown on Figure 6. The model utilizes several software packages: commercial (I-DEAS) and MIT (MEMCAD, FASTLAP—boundary element solver for Laplace's equation.) The model was implemented mostly by the MEMCAD group (Joseph Young). We have used the model to investigate the dependence of focusing on voltage and on the geometric parameters of the focusing electrode: radius of the opening; height above the gate; thickness; and slope of the sidewalls. The results show that increasing the radius of the opening in the focal electrode results in radial (focusing) electric fields of smaller magnitude and greater spatial extent, in agreement with analytical considerations. Somewhat surprisingly, changing the thickness of the focusing electrode has almost no effect on the radial electric field (Figure 7), possibly because the field is dominated by the lower rim of the focal electrode. Due to the difficulties involved in calculating the fields near the tip of the emission cone, the preceding calculations included only the gate and focus electrodes. The final step of the modeling — trajectory calculations — will incorporate the cone.

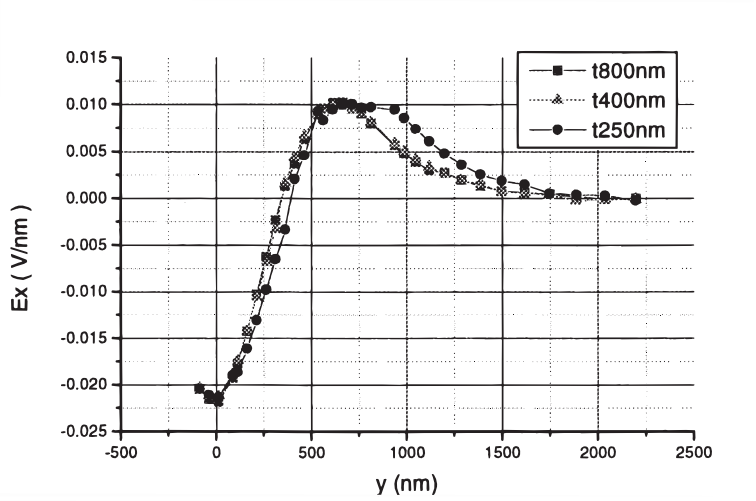


*Fig. 7: Radial Electric Field (Ex) vs. Height (Y) along the line x=250. Gate: Y = -87 to +87; Focus: Y= +537 to 787; 937; 1437.*

*Fig. 6: 3D Model of a Self-focused Field Emission Tip*

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The fabricated device (Figures 8, 9) has polysilicon electrodes separated by silicon dioxide spacers. The cones are formed by a Spindt-type process, utilizing angular evaporation of aluminum and gold parting layers, followed by vertical evaporation of molybdenum. After the cones are formed, the parting layer is lifted off, removing unwanted molybdenum.

Next, we plan to use the above technology in a new process, which will involve two masks, providing contact pads for individual devices, and add Chemical-Mechanical Polishing (CMP) of the gate and focus electrode. ❑

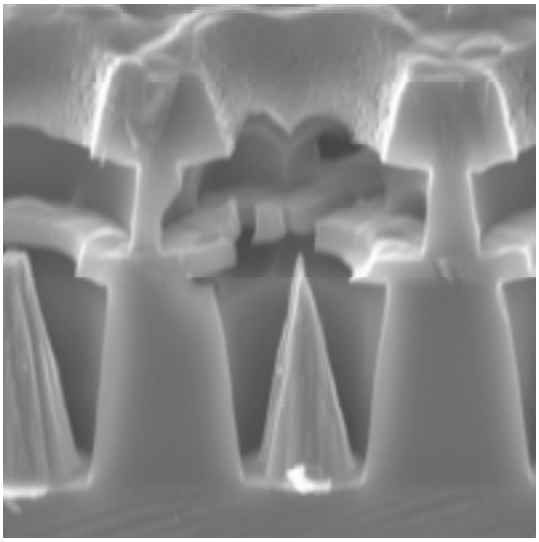

*Fig. 8: Array of Self-focused Field Emission Tips.*

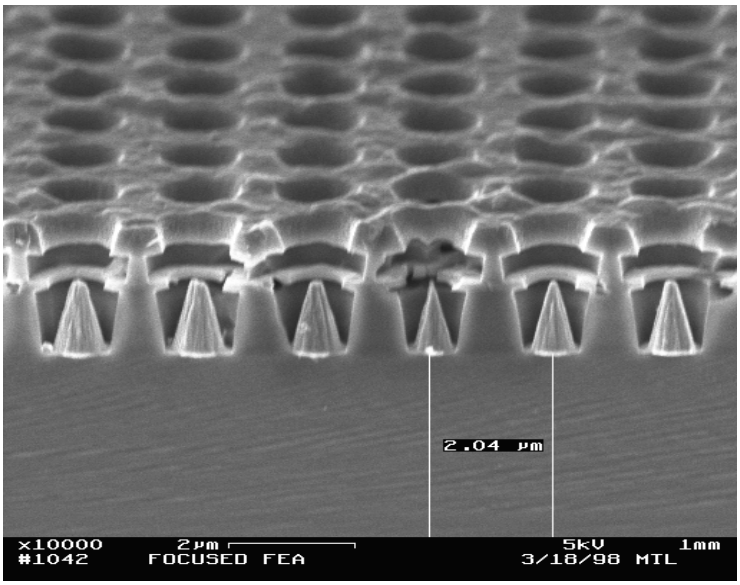


*Fig. 9: Self-focused Field Emission Tip.*

# Field Emitter Array Fabrication and Characterization

## Personnel

M. Ding
(A. I. Akinwande and R. Ashoori)

## Sponsorship

DARPA

Field Emitter Display (FED) technology is attracting interest because of its projected advantages of flat, small, high resolution, high brightness and high luminous efficiency. A FED uses an addressable two-dimensional array of field emission devices as a flat electron source. Each field emitter is made up of a cone located within a gate aperture. A voltage applied to the gate induces a high electric field on the silicon or molybdenum cone and leading to the field emission of electrons. The electrons are then accelerated to a phosphor screen due to anode voltage and consequently generate photons. The electron emission process is essential to the performance of FEDs and it is heavily dependent on the topology and the surface potential of emitter. Understanding the mechanism of the electron emission process and the parameters that effect it will allow improvements and advances in the performance of field emission devices.

We are fabricating FEAs with different emitter materials or coatings and will study how these processes affect the performance of the devices. We are developing a Scanning Maxwell-stress Microscope (SMM) system to determine simultaneously the topology and the surface potential of the emitter. A block diagram of the system shown in Figure 10 is based on a commercial UHV AFM/STM system. The microscope operates by applying DC- and AC-voltage bias between the imaging tip and the sample surface. As the tip is scanning across the sample, electronic forces deflect the cantilever which modulates the signal of the reflected laser beam to the photo-detector. The interaction force consisting of a DC part, a first-harmonic AC-part and a second-harmonic AC-part. Lock-in amplifiers (Lock-in I and Lock-in II) are used to detect the two harmonic parts. The first harmonic part depends on the local surface potential and will vanish when the applied DC voltage is exactly equal to the local surface potential. The second harmonic part depends on the local capacity between tip and sample. In distance regulation mode it is essentially measuring images of "constant local tip-sample capacitance" which is identical with topography images for conducting samples.

We are concurrently fabricating very high aspect-ratio imaging tips that will be used in our UHV AFM/STM system for the SMM task. The imaging quality is significantly dependent on the aspect-ratio of the imaging tip. We are fabricating imaging tips with an aspect ratio as high as 5:1 and 10:1 in order to obtain images of maximum quality. To the best of our knowledge, if proven successful, this will be the highest aspect ratio tip available in the present industry. ❑

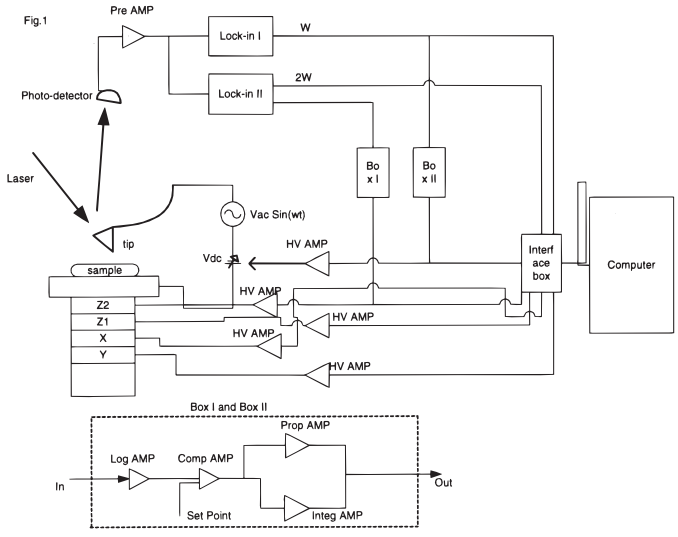


*Fig. 10*

# Technology Development for Coated Si Field Emitter Arrays

**Personnel**
H. Kim
(A. I. Akinwande)

**Sponsorship**
IAE

There is growing interest in Field Emission Display (FED) technology due to its projected advantages. These are low power consumption, small volume, wide viewing angle and temperature insensitivity. The FED is an emissive display and for this reason it has the potential to have higher brightness and luminous efficiency than the Liquid Crystal Display (LCD) which dominates the flat panel display market at this time. The performance of FEDs is directly related to the electron emission efficiency of field emitter arrays—high emission current at low applied voltage. Several approaches to improve field emission efficiency have been reported. One approach is to use to reduce the barrier height by coating the emitter with low workfunction materials. Materials selection for field emitter arrays is thus very important.

The objective of this research program is to fabricate gated Si FEAs with thin low workfunction coatings. Our approach is to use Si as mold on which materials with desirable emission properties are deposited. We have fabricated (a) Si Tip arrays (shown in Figure 11), (b) Si Tip Field Emitter Arrays with Cr Gate (shown in Figure 12) and (c) Si Tip Field Emitter Arrays with n-Poly Si Gate(shown in Figure 13). The next step in our work is to coat the Si tips with metal silicide, tungsten and diamond-like carbon (DLC). ❑

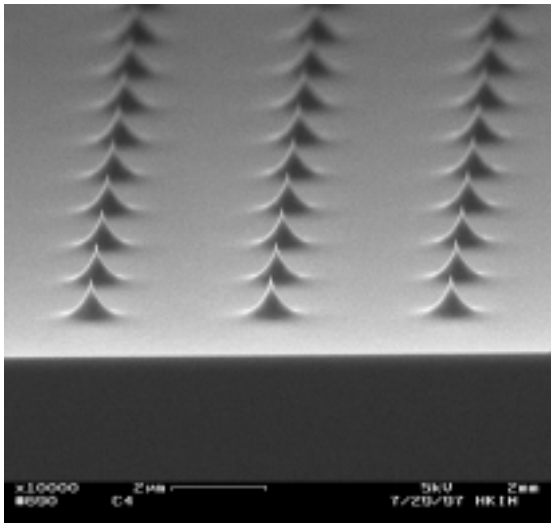

*Fig. 11: Si-Tips (a) array and (b) single tip.*

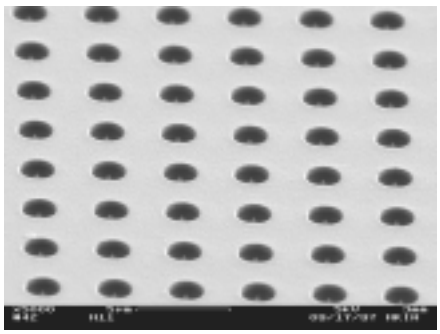

*Fig. 12: Si -Tip field emitter array with Cr gate.*

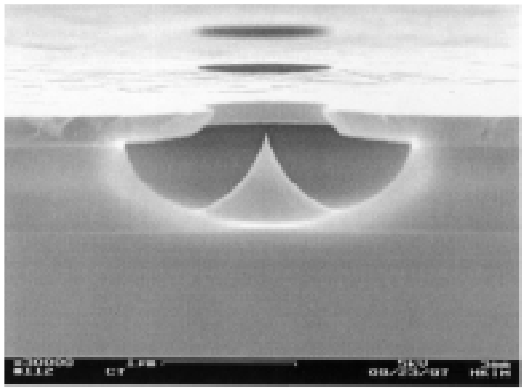

*Fig. 13: Si -Tip field emitter with n- poly-Si gate.*

# Inductively Coupled Time Multiplexed Deep Etching

## Personnel

A. A. Ayon, R. Braff, R. Bayt, and C. C. Lin
(H. Sawin and M. Schmidt)

## Sponsorship

DARPA and ARO

We have characterized the response dependence of silicon etching rate, Aspect Ratio Dependent Etching, photoresist etching rate, uniformity and anisotropy, on operating conditions for a time multiplexed inductively coupled plasma etcher. The data were collected by running matrices that included up to 8 variables. The relevance of RF-bias power, inductive power, pressure and gas flow rates was analyzed and compared with data reported by other authors concerning high density plasmas. The observed behavior serves as a complementary tool to locate and optimize operating conditions to etch high aspect ratio structures. The performance of the deep etcher in MTL allows the tailoring of etch rates of 4+ microns per minute with anisotropic profiles, nonuniformities of less than 4% across the wafer, and RIE-lag control with a depth variation of less than 1 micron for trenches of dissimilar width. Furthermore it is feasible to prescribe the slope of etched features from positive to reentrant. ❑

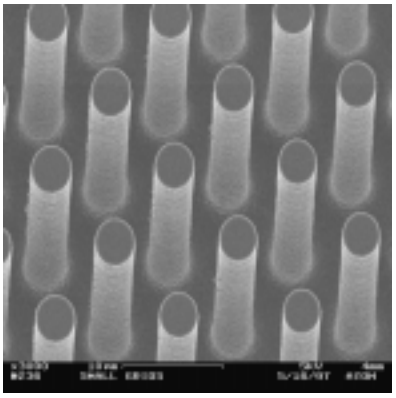

*Fig. 12: Micrographs showing high aspect ratio structures micromachined using Ti me Multiplexed Deep Etching (TMDE). With this approach it is feasible to obtain anisotropic profiles with silicon etching rates in excess of 3 microns per minut e, and selectivities to photoresist greater than 80:1. Several MIT pprojects are currently applying this technology in areas as diverse as turbomachinery, soft photolithography and electric induction machinery.*