CMOS Technology for 25 nm Channel Length

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Personnel
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The scaling of CMOS transistors into the sub-100 nm region is extremely challenging because of short-channel effects. We are pursuing two distinct approaches that should permit scaling to 25 nm channel lengths. Both can be considered 3-dimensional-gate CMOS (3DG-CMOS) technologies. One is a planar twin-gate configuration, with either joint or independent control of the two gates per MOSFET; the other features a gate that surrounds a pillar-like vertical channel.

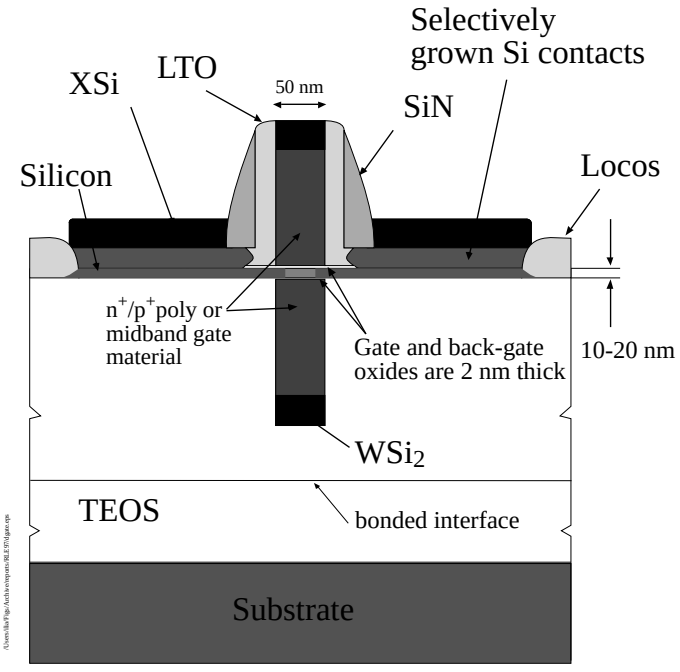

Fig. 1: Dual gate n-MOS transistor with 25 nm effective channel length.

Monte-Carlo modelling predicts that twin-gated devices that are scaled to L_{eff} = 25 nm will have transconductances G_m in excess of 2000 mS/um, while maintaining almost perfect sub-threshold slope. However, models also predict that the tolerance in aligning front and back gates has to be within Lg/4 in order to avoid performance deterioration due to overlap capacitance. The Lg/4 requirement translates into 6 nm alignment tolerance for a 25 nm channel. In order to meet this alignment challenge we will use the IBBI alignment technique which achieves sub-nanometer misalignment detectivity. The planar twin-gate devices will be fabricated starting with a SIMOX wafer. First the gate stack for the back-gate will be deposited and patterned by x-ray lithography. The structure will then be covered by a layer of CVD oxide, planarized, and bonded to a "handle wafer". The bulk of the SIMOX wafer will then be chemically etched using the back-oxide of the SIMOX wafer as the etch-stop. The fabrication will then follow a conventional SOI process, with front gate precisely aligned to back-gate layer using the IBBI alignment scheme. The final structure is depicted in Figure 1.

The second approach to 3DG-CMOS utilizes epitaxially grown vertical pillars of Si. Such a structure addresses two major problems in ultra-short-channel MOS fabrication. First, a surround-gate has maximum possible control of the channel potential, improving sub-threshold slope and reducing short-channel effects to allow scaling of the effective channel length (L_{eff}) down to 25 nm for pillar MOS device 40 - 50 nm in diameter. Second, epitaxial definition of a vertical channel allows almost arbitrarily short Leff with tighter control than is possible with current lithography technologies. In planar MOS devices, gate length is limited by lithography; the inherent variability in the lithography and etch processes can lead to unacceptable variation in Leff from device to device and wafer to wafer. This is especially critical in ultra-short-channel devices, where the threshold voltage is extremely sensitive to gate length.

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Previously demonstrated processes for epitaxially-defined vertical MOS structures generally start with the etching of a pillar from the epi wafer, and suffer from severe difficulties in the subsequent contact and isolation of gate and source/drain regions. These problems are avoided in our proposed vertical-MOS process, illustrated in Figure 2, where the gate electrode material and dielectrics for source/drain isolation are deposited prior to hole-definition and epitaxial growth.

We are currently experimenting with selective epitaxial growth in features down to 100 nm in diameter patterned in oxide on silicon, a key technology for our novel vertical-MOS process. ❑

Fig. 2: Process for Fabricating Surrond-Gate Vertical MOS Devices.

Design and Fabrication of Single-Mask 50 nm MOSFETs

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DARPA, ONR, and NSF Graduate Fellowship

Personnel

K. M. Jackson and Z. Lee
(D. A. Antoniadis and H. I. Smith)

As MOSFET dimensions are scaled to lengths below 100 nm, significant challenges arise in controlling fabrication processes. Rapid turnaround between process changes and device results, and an ability to extract the exact structure and doping of the fabricated device are tools critical to this development. The first requires a short-flow process that focuses only on the fabrication steps that critically define device performance in a minimum number of steps. The second tool, known as inverse modeling, couples a device simulator with an optimizing routine that shifts the doping in the simulated device until the current-voltage and capacitance characteristics of the simulated device match those of the real device. This project focuses on creating a short-flow process for 50 nm channel-length MOSFETs and coupling it with currently exisiting inverse modeling capabilities.

The short-flow process we have conceived will allow working MOSFETs to be fabricated in one mask step. It is shortened from a normal full-length MOSFET process by eliminating the need for oxide isolation around the devices and by eliminating the need for the passivation and metal layers at the end of the process. Two types of structures will allow devices to be operational MOSFETs without field-oxide isolation. The first structure is an annular device where the source is completely enclosed inside of a gate and the drain is outside of the annular gate. The second structure is a figure-eight configuration (Figure 3) where the parasitic out-of-channel (i.e. field region) source-to-drain current is less than 0.02 times the in-channel current under the gate in the center of the structure. By using a self-aligned cobalt-silicide process (salicide) the source and drain will be low

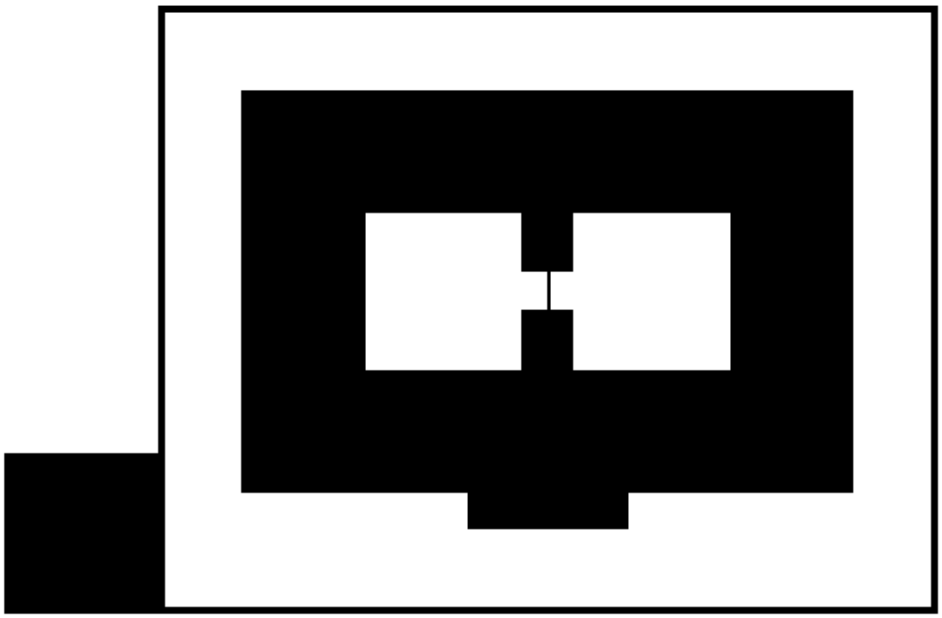

Fig. 3: Gate mask layout of a figure-eight geometry MOSFET. The inner two white square areas are the source and drain probe pads that will be salicided. The dark wide ring is the gate pad with the active gate being the fine line in the center. The outer ring is a guard ring.

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Device Design to Minimize Hysteretic Effects in SOI MOSFET's

Personnel

A. Wei and A. Ritenour
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SRC

enough in resitivity that they can be contacted directly by probes. Even though two significant steps of the conventional fabrication process are left out, the steps that define the device operation - the gate stack, implantation, and critical high temperature steps - are all contained in the short-flow process.

The gate-level lithography (the only lithography step) for the short-flow process will be done using X-ray lithography, easily allowing linewidths down to 50 nm. The mask will be fabricated with a mix of optical steps for the large features and e-beam writing for the fine gates. Using optically placed e-beam registration marks, the e-beam tool can match the in-plane scale and distortion of the optical projection tool to achieve good pattern placement.

The key elements in the fabrication of sub-100 nm devices are the placement of dopants and the use of very thin gate oxides. A process to grow 20 Å oxides in N_2O has been developed. With such thin oxides, etching the polysilicon gate and stopping on the gate oxide will be the major challenge. The placement of the dopants calls for a combination of implantation and diffusion. We are investigating very-low-energy implants for the source and drain of these devices. Dopant diffusion will be carefully controlled by a few high temperature, rapid thermal anneals. Building on our previous successes in fabricating robust 100 nm NMOS, we will explore the optimization of source and drain design.

Once devices are fabricated using the short-flow process, their doping and structural components can be evaluated via inverse-modeling, using current-voltage and capacitance measurments. Understanding what doping profiles were achieved versus the original design then will allow us to go back and adjust the process and to see how changes affect the doping profiles in the device. This approach should facilitate the optimization of device fabrication for deep-sub-100 nm MOSFETs. ❑

SOI MOSFET's offer many performance benefits over bulk MOSFET's including reduced junction capacitance and reduction of the negative back-bias effect in pass-gates and stacked transistors. However, floating-body operation of partially-depleted SOI MOSFET's leads to switching-history-dependent body charge, and hence hysteretic device threshold voltage. This is of serious concern in SOI-CMOS circuit design because floating-body-induced threshold-voltage variation, ΔV_T, contributes to propagation delay variation, particularly as the supply voltage is reduced. It is important to develop a device design methodology which minimizes this threshold-voltage variation.

Body charge in a SOI MOSFET with the body floating is switching-history dependent because on the timescale typical of digital switching, body charge typically removed and replenished by a body contact cannot be completely removed or replenished by the diodes and impact ionization schematically shown in Figure 4; the bias voltage on the body is determined by the capacitive network shown in Figure 5. Thus it takes many switching cycles to establish a switching-steady-state per a

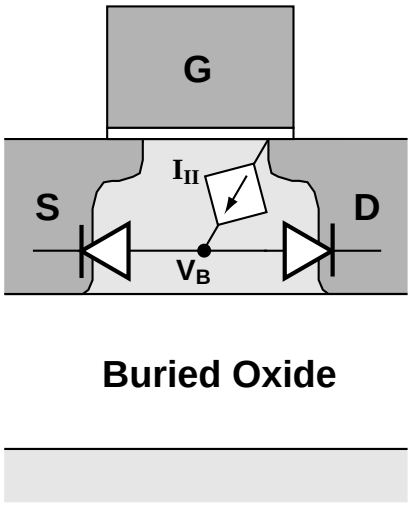

Fig. 4

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particular switching waveform, and a long time to relax to initial conditions. Also, starting from these initial conditions, there is already an initial imbalance in body charge between devices in different logic states. This difference in initial body charge and the history dependence of body charge leads to an initial ΔV_T, which then changes during subsequent device switching.

It is possible to minimize ΔV_T by design of the device film thickness, such that body charge is unchanged in the two different logic states OUT-HI and OUT-LO. Design of the device for decreased gate-body capacitive coupling and non-ideal body-source/drain diode behavior also tends to minimize ΔV_T. Both of these designs are in accordance with bulk MOSFET scaling trends, with shrinking gate length and increased peak channel doping. However, minimization of hysteresis by reduced gate-body capacitive coupling and non-ideal body-source/drain diode behavior tends to negate some performance advantages by reducing capacitively coupled on-current overshoot and by introducing a high initial body voltage which leads to increased off-state leakage and poor subthreshold slope. ❑

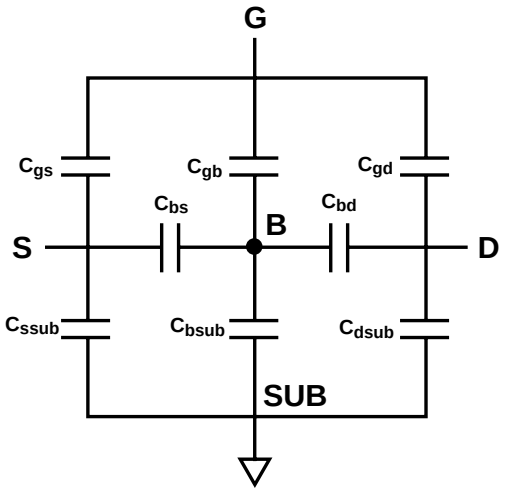

Fig. 5

Self-Aligned Dual-Gate Variable Threshold Voltage (VT)CMOS Technology

Personnel

A. Wei and A. Ritenour
(D. A. Antoniadis)

Sponsorship

SRC

Continued power supply scaling in CMOS technology requires scaling of device threshold voltage to maintain circuit performance. However, reduced device threshold voltage leads to unacceptably high off-state leakage current, particularly as device dimensions are reduced. A variable threshold-voltage CMOS technology allows for reduced threshold voltage during periods of high circuit activity and an increased threshold voltage when the circuit is idle for long periods of time.

Silicon-On-Insulator with Active Substrate (SOIAS) has been demonstrated in which a buried back gate is used to modulate the front gate threshold voltage of a fully-depleted SOI MOSFET. Fully-depleted SOI MOSFET's are ideal for variable threshold voltage technology due to their inherently low threshold voltage, and the addition of the backgate facilitates fully-depleted SOI MOSFET scaling into extreme submicron regimes. Alignment of the front and back gates is difficult, however, and SOIAS technology used an oversized backgate, formed in buried unpatterned polysilicon. Oversize of the backgate leads to a large drain-to-backgate overlap capacitance resulting in degraded performance.

Shown below in Figure 6 is a representational cross-section of a self-aligned dual-gate variable threshold voltage CMOS. The structure is a fully optimized version of SOIAS technology featuring self-alignment of front and back gates, silicided front and back gates, and silicided raised source/drain to minimize series resistance in the fully-depleted MOSFET. It is fabricated by forming the backgate stack on an SOI wafer. The backgate stack is silicided, patterned, filled with dielectric, chemical-mechanical-polished flat, flipped, and bonded to a handle wafer. The substrate of the SOI wafer, now on top, is removed in a chemical etch, and the buried oxide of the SOI wafer is removed leaving the SOI film on which to build devices. Devices are aligned to the prepatterned backgates. The prepatterned backgates are oversized relative to the front gate in order

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to meet alignment tolerances. Full self-alignment is achieved by counterdoping of the backgate through the frontgate in order to form regions with low doping. This should significantly reduce overlap capacitance. A raised source/drain is then formed by selective epitaxy and the top device is silicided and contacted.

The feasibility of this technology will be evaluated relative to device design requirements dictated by device scaling. ❑

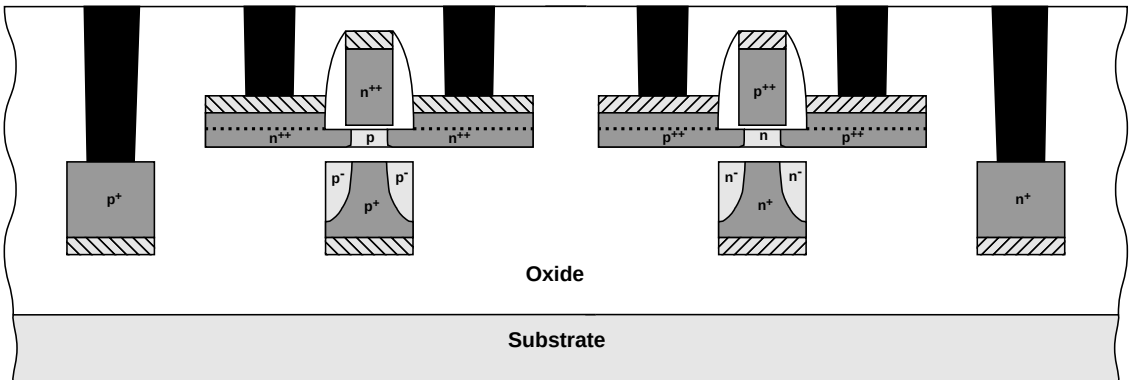

Fig. 6

RF SOI LDMOS Power Devices

Personnel
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(J. A. del Alamo and D. A. Antoniadis)

Sponsorship
SRC

Our project involves the design and fabrication of RF (Radio Frequency) SOI (Silicon-On-Insulator) LDMOS (Laterally Diffused MOS) power devices. SOI-LDMOS is well suited for the development of devices for the high-frequency, high efficiency power amplifiers that are required by portable wireless communication handsets. It is also a technology that could potentially enable the integration of analog, digital and RF circuits onto a single substrate and provide an avenue for the realization of a single-chip wireless communication system.

A cross-section of the RF SOI LDMOS device that we have designed is shown in Figure 7. The device is a MOSFET with several enhancements to give it superior RF power performance. The laterally doped body is designed to increase the device's gain at high frequency, while the lightly doped N-type drift region combined with a body tie under the source increases the device's power handling capability. Silicide on the source, gate, and drain improves the device's power efficiency. The insulating buried oxide layer reduces the parasitic drain capacitance and improves the isolation between different devices on the same substrate. The device fabrication process has been designed to avoid exotic processing techniques so that it will ultimately be possible to integrate the power device process into a standard digital SOI CMOS process. Microwave and DC test structures are being fabricated to measure the power device performance, the isolation properties of the SOI substrate, and to understand how the SOI substrate affects the LDMOS fabrication process. ❑

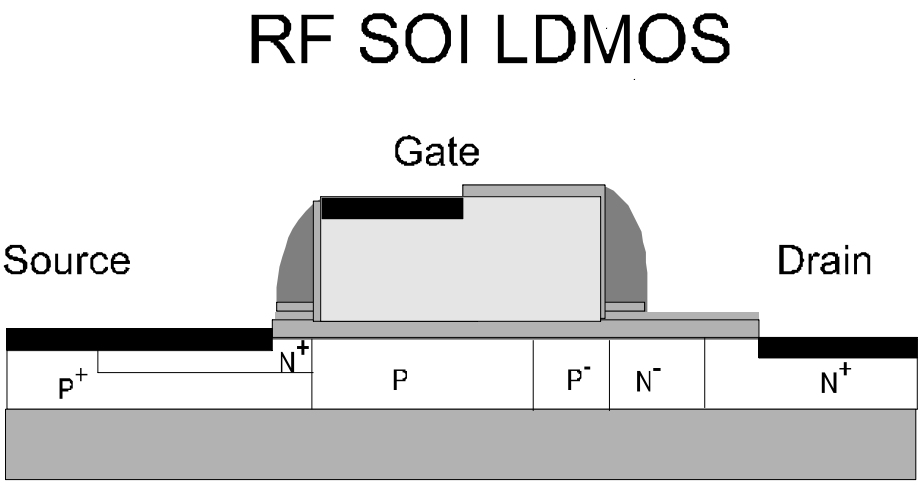

Fig. 7: RF SOI LDMOS Power Device.

Correlation of Silicon Microroughness on Electrical Parameters of SOIAS (Silicon-On-Insulator with Active Substrate)

Personnel
H. Nayfeh
(D. A. Antoniadis)

Sponsorship
DARPA

The SOIAS process previously developed at MIT allows the transfer of a thin single-crystalline layer of device-quality silicon from a SIMOX (Separation by Implantation of Oxygen) wafer to a bulk carry wafer. As the carry wafer can potentially have pre-fabricated layers of interconnects and gates, this technology holds promise for future 3D integration. We have studied the surface quality of this transferred silicon layer, and have developed a chemical-mechanical polishing process to improve this surface.

The single-crystalline silicon layer is flipped in the process of bonding to the carry wafer. Thus, the top surface of the SOIAS wafer, to be used for subsequent device fabrication, is the poorer quality buried silicon interface from the initial SIMOX wafer. This calls for a proper investigation and optimization of the surface properties of SOIAS. Novel Chemical Mechanical Polishing (CMP) techniques were used to achieve minimum surface roughness. Electrical parameters are being determined by measuring the interface state density (D_{it}) using charge pumping, the dielectric breakdown using Time-Zero Dielectric Breakdown (TZDB), and the effective mobility (μ_{eff})as a function of vertical electric field. The surface has been characterized using Atomic Force Microscopy (AFM) as can be seen in Figures 8 and 9. The relationship between surface roughness and these parameters is being determined by measuring the above electrical parameters on fabricated gated P-i-N diodes and NMOS transistors with different initial surface roughness.

Surface roughness on the atomic scale is expected to contribute to interface trap states. These sites can then be occupied by carriers resulting in more scattering events that lead to lower values of mobility. It has also been shown that smoother surfaces have a better coupling between gate voltage and surface potential leading to higher mobilities. In addition, as the scaling down of transistor dimensions becomes a viable thrust in the technology industry to achieve larger density of integrated circuits, reduction of the oxide thickness becomes mandatory. This poses a serious challenge to avoid dielectric breakdown. It has been reported that roughness reduces the intrinsic breakdown field strength by field enhancement at pointed bumps at the irregular Si-SiO_2 interface. Therefore, the quality of the Si-SiO_2 will be crucial in achieving this goal. ❑

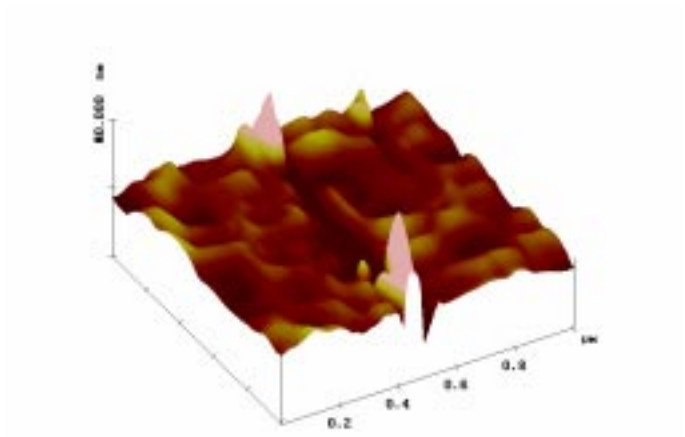

Fig. 8: SOIAS Wafer - 3.96 nm RMS.

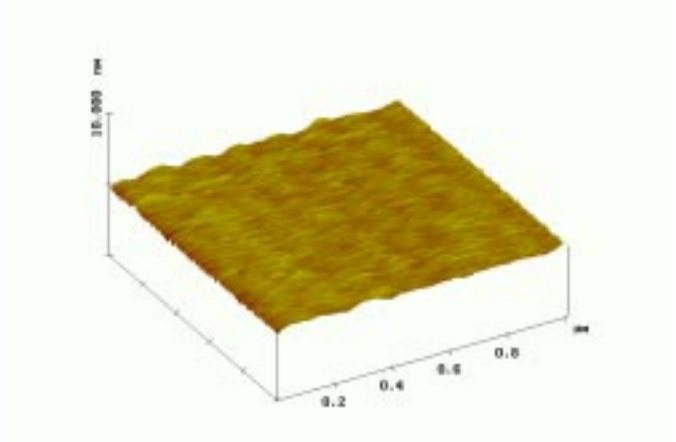

Fig. 9: SOIAS Wafer After Touch Polish - .123 nm RMS.

On-State Breakdown in Power HEMTs: Measurements and Modeling

Personnel

M. Somerville
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Sponsorship

JSEP

Although great strides have been made in understanding and improving off-state breakdown (BV_{off}) in High Electron Mobility Transistors (HEMTs), work on the on-state breakdown voltage (BV_{on}) has been limited due to difficulties in defining and measuring this figure of merit. This is problematic, as BV_{on} is now recognized as the crucial parameter limiting HEMT power performance. We have recently proposed a simple, unambiguous, reproducible, and non-destructive *gate current extraction* measurement for BV_{on}. This method, in conjunction with detailed temperature-dependent measurements and sidegate measurements, has revealed the roles of impact ionization and tunneling plus Thermionic Field Emission (TFE) in BV_{on} and BV_{off}. It has also allowed us to develop a simple model for BV_{on}. Our findings suggest that depending on device design, either BV_{off} *or* BV_{on} can limit the maximum power density of a HEMT.

The inset of Figure 10 depicts the measurement technique for BV_{on}. I_G is held constant at a desired value (a typical condition is 1 mA/mm), and I_D is ramped from I_G to some reasonable value (typically 1/5 I_{Dmax}). This technique traces a locus of V_{DS} versus I_D for constant I_G; we define this locus as BV_{on}. This definition is sensible in several respects: (1) it ramps from BV_{off} which is usually defined as $I_G = I_D$; (2) it defines a locus of significant gate conductance; (3) it is a reasonable predictor for device burnout.

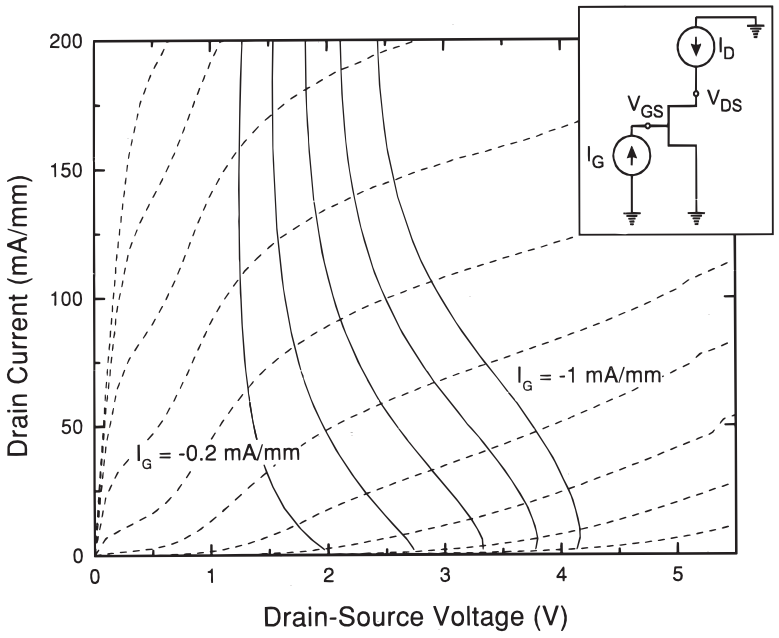

Fig. 10: BV_{on} versus I_D for 0.1 μm InAlAs/InGaAs HEMT for different values of I_G. The data are superimposed on the output characteristics. The constant I_G criteria additionally tracks the sudden rise of drain conductance often associated with BV_{on}. The inset shows the biasing condition for the gate current extraction measurement. A constant current (typically 1 mA/mm) is extracted from the gate while I_D is swept from the off-state (1 mA/mm) to the on state (200 mA/mm). The technique traces a breakdown locus of V_{DS} versus I_D.

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The technique is illustrated on a state-of-the-art 0.1 μm InAlAs/InGaAs HEMT in Figure 10, where BV_{on} loci for several values of I_G are superimposed on the output characteristics. As the device is turned on, BV_{on} drops from 4.2V (BV_{off}) to less than 2.5 V. For $V_{DS} > BV_{on}$, the drain conductance begins to rise, indicating that the device is approaching a dangerous bias region. Burnout measurements show that this analysis is correct — we have found that once the device is turned on, burnout occurs at an approximately constant value of I_G.

Because the technique is safe and reproducible, we have been able to perform temperature dependent measurements of BV_{on} and BV_{off}. These measurements, in conjunction with sidegate measurements, have allowed us to create a comprehensive picture of off-state and on-state breakdown. In the off-state, I_G is almost purely thermionic field emission. However, as I_D rises, impact ionization starts to produce holes which escape to the gate. To maintain constant I_G, V_{DG} must drop. Once the device is fully on, BV_{on} is dominated by impact ionization. Due to the exponential dependence of impact ionization on field, the locus of BV_{on} of becomes almost vertical.

Our simple picture of BV_{on} has lead to a phenomenological model that can assist device and circuit designers. The model accurately predicts the behavior of BV_{on}, for a variety of devices, and makes it clear that the *shape* of the transition from BV_{off} to BV_{on} is crucial to a device's power potential.

In summary, we have developed an unambiguous definition and a simple, non-destructive measurement for BV_{on} in HEMTs. Both BV_{off} and BV_{on} must be considered when designing a power device. ❑

Drain Resistance Degradation in InAlAs/InGaAs Power HEMTs

Personnel

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Sponsorship

HP

InAlAs/InGaAs High Electron Mobility Transistors (HEMT) hold promise for power-millimeter wave applications. A major reliability concern in some of these devices is the degradation of the drain resistance that is at times observed when the device is stressed for a long time at bias conditions necessary for power applications. The goal of this project is to find the physical origin of this reliability problem and to provide a solution to it.

State-of-the-art InAlAs/InGaAs power HEMTs, provided by our sponsor, Hewlett Packard, were stressed under different biasing schemes. One of these methods consists of forcing constant gate and drain currents through the device of a magnitude that corresponds to a typical bias point for power operation. As can be seen on the example shown in Figure 11, under the selected conditions the drain resistance degrades quickly. There are four noticeable regimes to R_d degradation in this device. First, a small but immediate degradation of about 2%. This is followed by a linear degradation for about 150 minutes. After this, the degradation rate decreases, but seems to be linear for another 300 minutes. For longer time, the degradation rate slows down considerably.

A whole suite of device measurements is taken at frequent time intervals during stressing. In addition to drain resistance degradation we have found that the source resistance initially improves about 5% until a certain saturation value is reached. The off-state breakdown voltage improves about 10%, at first, but after a long period it decreases quickly by as much as 50%. The peak transconductance decreases approximately linearly by about 9%, but the intrinsic transconductance increases by about 2%. The threshold voltages increases initially by about 2%, but after 500 minutes it starts to decrease. Dependent on the stressing conditions, some devices fail ("burnout") after a certain stressing time.

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The combination of results that we have obtained suggest that major changes are occurring at the drain side of the device as a result of the bias stressing. However, it appears that some changes are also taking place at the source and in the intrinsic portion of the device. Much more work is needed before the physical origin of this reliability concern is identified. ❑

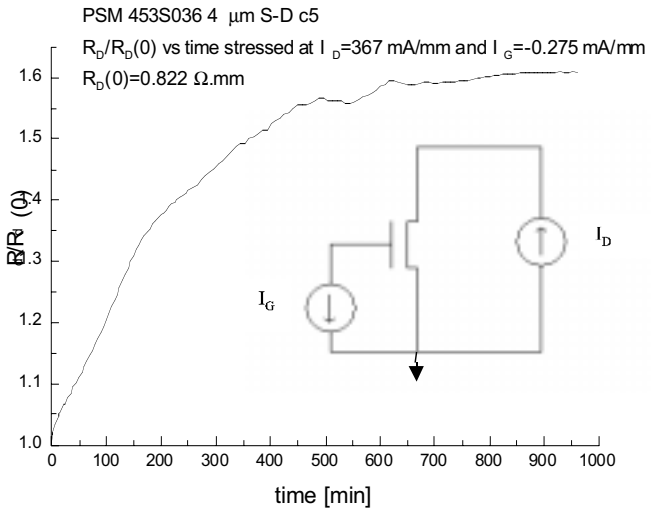

Fig. 11: Time evolution of the drain resistance of a InAlAs/InGaAs power HEMT stressed at I_D = 392 mA/mm and I_G = -0.275 mA/mm.

GaN Solar Blind UV Photodetectors

Personnel

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Sponsorship

DARPA

There is considerable interest in fabrication of solar-blind UV photodiodes for a number of applications, including early missile detection system. The $Al_xGa_{1-x}N$ material system is ideal for these applications since this system consists of direct band gap semiconductors tunable between 3.4 eV (364 nm) for GaN and 6.2 eV (200 nm) for AlN. However, significant problems exist in this material system due to the relatively high dislocation densities (10^8-10^{10} cm^{-2}), the difficulty in growing high carrier concentration p- doped material, and the lack of good low resistance p-ohmic contacts. The goal of this collaboration between the Molecular Beam Epitaxy (MBE) laboratory at Boston University and MTL at Massachusetts Institute of Technology is to fabricate p-i-n photodiodes using the $Al_xGa_{1-x}N$ system which show high responsivity, sharp absorption cutoff above 364 nm and low dark currents.

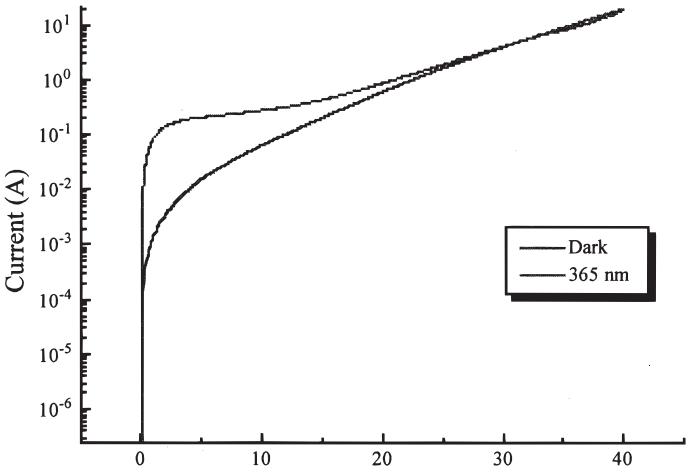

Fig. 12: IV Characteristics of .0401 mm^2 area device in the dark and under 365 nm illumination.

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The p-i-n GaN films are grown by MBE on either c-plane sapphire, or 25 μm thick n-type GaN substrates grown by hydride vapor phase epitaxy. Fabrication of the device consists of a three-mask process to create a mesa and to deposit ohmic contacts. The device is fully passivated using a SiN_x layer. Fabricated devices on a single wafer have varying geometries so that dark current can be studied as a function of both device perimeter and area. Presently, our studies on fabricated devices show that dark currents scale with area, suggesting that our leakage currents are primarily due to a bulk rather than a surface effect. Figure 12 shows the IV characteristics of a p-i-n device both in the dark and under illumination by 365 nm light. An additional masking step is being explored to introduce a dielectric pad upon which a large area p-ohmic contact can be placed. This contact pad isolation would reduce the overall electrical area of the device so that dark current can be minimized.

The ultimate objective of this project is to fabricate an array of Avalanche photodetectors that are sensitive in the UV solar blind regime. The reverse leakage current have to be significantly reduced in order to obtain internal gain by avalanche multiplication. Our efforts are being focused on reducing the defect density to a level that will lower the dark currents at the high voltages required for avalanche multiplication. ❑

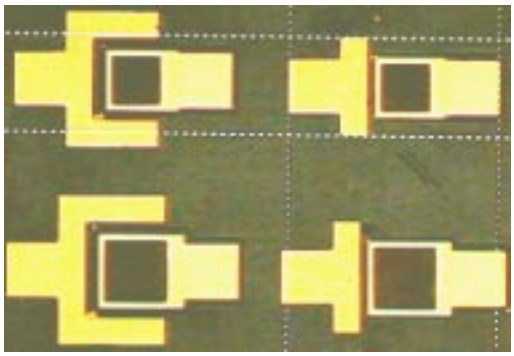

Fig. 13: Photo p-i-n GaN photodetector.

Linearity of GaAs HBTs

Personnel
R. Chatterjee
(J. A. del Alamo)

Sponsorship
None

AlGaAs/GaAs Heterostructure Bipolar Transistors (HBT) are important for high-performance RF Power Amplifiers (PA) and are especially attractive because of their superior linearity properties. There are several performance figures of merit that an HBT must be designed for in RF power applications. These include the Gain (G), power output (P_{OUT}), Power Added Efficiency (PAE), and third order Intermodulation Distortion (IMD3) which is a measure of linearity. A high G is desired so that the PA can be constructed with a minimum number of stages. A high PAE is necessary for long operation times on battery operated systems. The P_{OUT} is a system requirement. A low IMD3 is needed so that signal spillover to an adjacent channel is minimized. Currently there is a good understanding of the aspects of device design that impact P_{OUT}, G, and PAE. Much of the work directed towards designing for linearity relies on crude models with poor fundamental basis. A solid understanding of the relation between the structural parameters and the linearity of HBTs is crucial for successful RF power device design. Contributing this understanding is the goal of this project.

IMD3 is a figure of merit for linearity that is based on two-tone intermodulation distortion measurements. In this technique, two different sinusoidal signals of frequencies f_1 and f_2 are input to a PA. Since the HBT is not perfectly linear, these two frequencies produce several harmonics on the output. The power of the output signal at a frequency of $f = 2f_1 - f_2$ is the low-frequency third-order intermodulation distortion (IMDL) and the power at the frequency $f = 2f_2 - f_1$ is the high-frequency third order intermodulation distortion (IMDH). The IMD3 figure of merit is derived when IMDL is normalized by $P_{out}(f_1)$ which is fairly close to the result of normalizing IMDH by $P_{out}(f_2)$. The units of IMDL and IMDH are dBm and the unit of IMD3 is dBc. If f_1 and f_2 are not very different, these two spurious frequencies, $(2f_1 - f_2)$ and $(2f_2 - f_1)$ could fall in an adjacent channel producing undesirable interference.

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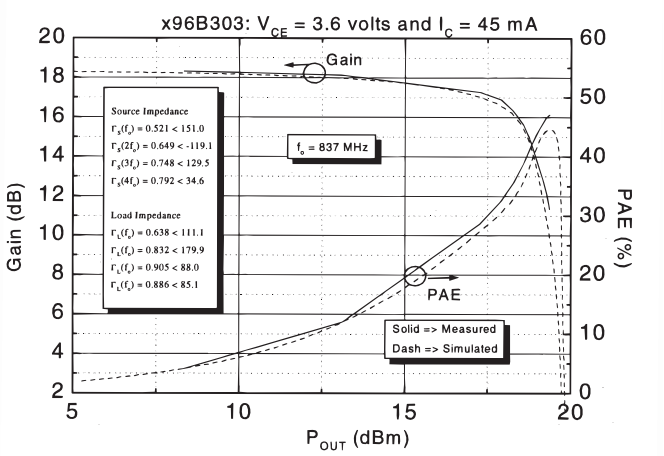

Fig. 14: Measured and Simulated G and PAE vs. P_{OUT} for a state of the art AlGaAs/GaAs HBTs.

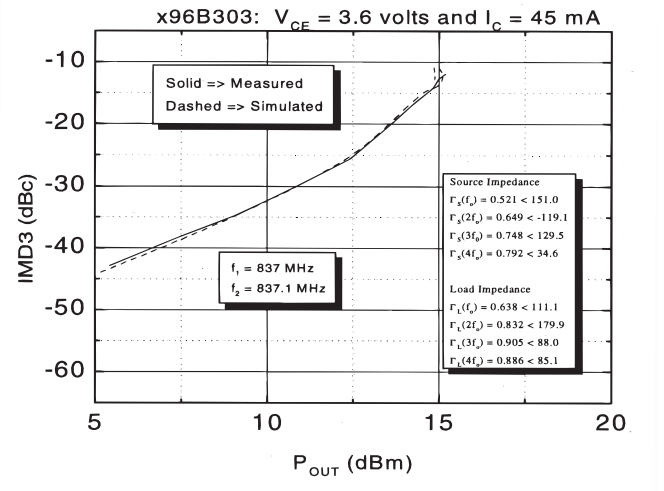

Fig. 15: Measured and Simulated IMD3 vs. P_{OUT} for a state of the art AlGaAs/GaAs HBTs.

This is relevant because while the PA is being used, it will have inputs of many frequencies within some bandwidth. The IMD3 figure of merit attempts to account for potential interference among frequency components in this bandwidth by examining only the interplay of two frequencies as a representation of the intermodulation of any of the other frequencies in that bandwidth.

To assess the linearity, an adequate simulation environment must be used. HBTs operating in the large signal regime are typically modeled with the Gummel-Poon Bipolar Transistor Model (GP). The GP model is used in many commercial CAD systems such as HP-Libra. Figure 14 shows measured and simulated data for PAE and G from single tone simulation and measurement.

Figure 15 shows measured and simulated data for IMD3 in the HP-Libra simulation environment. Two signals with different frequencies (f_1 = 837 MHz and f_2 = 837.1 MHz) are input into a state-of-the-art AlGaAs/GaAs HBT in a common-emitter configuration. As can be seen from these plots, the simulation is very good at predicting the measured results. This excellent agreement between simulation and measurement are a good basis to understand what aspects of device design impact IMD3.

From the GP model, several sources of non-linearity are seen. Some of the most significant ones are: the exponential relationship between V_{BE} and I_C, the exponential relationship between V_{BE} and I_B, the V_{BC} dependence of base to collector capacitance (C_{BC}), and the V_{BE} dependence of base to emitter capacitance (C_{BE}). The next step is to develop analytical models of each of the device nonlinearities that would help us identify the dominant sources of intermodulation distortion. ❑

Physical Mechanisms Limiting the Manufacturing Yield of Millimeter-Wave Power InP HEMTs

Personnel

S. Krupenin
(J. A. del Alamo)

Sponsorship

MAFET Program (through Sanders Lockheed Martin)

Despite the improving prospects for InP High Electron Mobility Transistors (HEMTs) in millimeter-wave power applications, an understanding of the factors affecting the manufacturing yield of these devices has been hampered by the considerable amount of work that it takes to evaluate millimeter-wave power figures of merit. Manufacturing yield improvement is critical because high cost represents a significant road block in the development of millimeter-wave systems.

We have addressed this issue by developing a yield assessment methodology that is based on a statistical study of DC figures of merit obtained in actual transistors. We measured the threshold voltage, maximum drain current and transconductance, on- and off-state breakdown voltages, and other figures of merit that strongly impact millimeter-wave performance of InP HEMTs. We characterized 50 power 0.1 μm double-heterostructure InAlAs/InGaAs HEMTs on InP on an experimental 3-inch wafer from Sanders Lockheed Martin.

A Principal Component Analysis (PCA) was carried out in an attempt to uncover the physics underlying the correlation between these figures of merit. PCA performs a coordinate transformation from the original space of electrical measurements to the space of uncorrelated "principal components". These are ordered according to the total variance that they account for in the original data: first the variance explained by P1 is maximized; then the second component, P2, is selected to maximize the variance of the residual after P1 is removed, and so on. In a first pass, all figures of merit were weighted equally. Customer demands can be taken into account by introducing appropriate weights.

PCA showed that the main source of variability, "principal component" P1, accounts for 51% of the total variance of the process. Correct identification of this component, followed by appropriate corrective action, can significantly improve the manufacturing yield. The second and the third components account for 21% and 13% of the total variance respectively.

Fig. 16: (Left) schematic diagram of a typical HEMT device showing the physical interpretations of P1 and P2, the dominant sources of manufacturing variability. (Right): bar chart showing the impact of each principal variance component on the measured figures of merit.

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The physical origin of P1 and P2 was identified by examining details of their correlation with the DC figures of merit. P1 has been linked to the concentration of Si dopants in the delta-doping layers of the device that is produced during the molecular-beam epitaxial growth of the heterostructure. This identification was independently verified through measurements on gateless test structures. P2 was related to gate-source distance variations that are introduced in the electron-beam fabrication process of the gate.

The methodology that we have developed can be easily implemented in a manufacturing environment for continuous process yield diagnostics and improvement. The most important sources of manufacturing variations are found using the Principal Component Analysis, with all the necessary statistical data obtained from simple DC measurements on actual transistors – no specialized test structures were required. ❑

Arrays of Nanomagnets for High Density Information Storage

Personnel

M. Farhoud, J. M. Carter, J. M. Bae, and M. Hwang
(C. Ross, H. I. Smith, and K. Youcef-Toumi)

Sponsorship

3M Corporation

For several years, the areal density of information storage in thin-film hard disks has been increasing rapidly through improvements in magnetic materials, head design, signal processing, and mechanical design; while prices have fallen with equal rapidity. This trend clearly cannot continue forever, and in fact will soon slow down unless a new paradigm for magnetic information storage is invoked. Following earlier work by S. Y. Chou, R. L. White, and others we have initiated a program to develop fabrication technologies for ultra-high-density information storage based on discrete pillars of ferromagnetic materials, as illustrated in Figure 17. In order to exceed the extrapolated information density of conventional hard discs, the pillars must have diameters less than 100 nm and a spatial period less than 200 nm (aerial density of 2.5 x 10^9 /cm^2). In fact, our

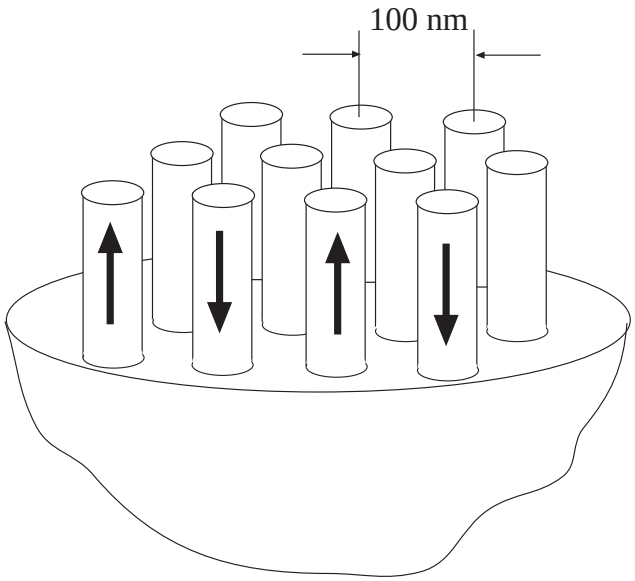

Fig. 17: Schematic of high density magnetic information storage based on discrete sub-100 nm sized magnetic pillars.

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goal is to achieve aerial densities of 4×10^{10} /cm^2, corresponding to a spatial period of 50 nm in the array of magnetic pillars. An important focus of our research is to realize such densities via techniques that are compatible with low-cost manufacturing. The lithography candidates are therefore restricted to interferometric lithography, X-ray lithography, achromatic-interferometric lithography, and nanoimprint lithography. At present our work is confined to the first, using a process illustrated in Figure 18. The magnetic materials of choice at present are nickel and cobalt, both of which are electroplated into the holes produced in an AntiReflection Coating (ARC) by the process illustrated in Figure 18. Figure 19 shows some results of electroplating cobalt.

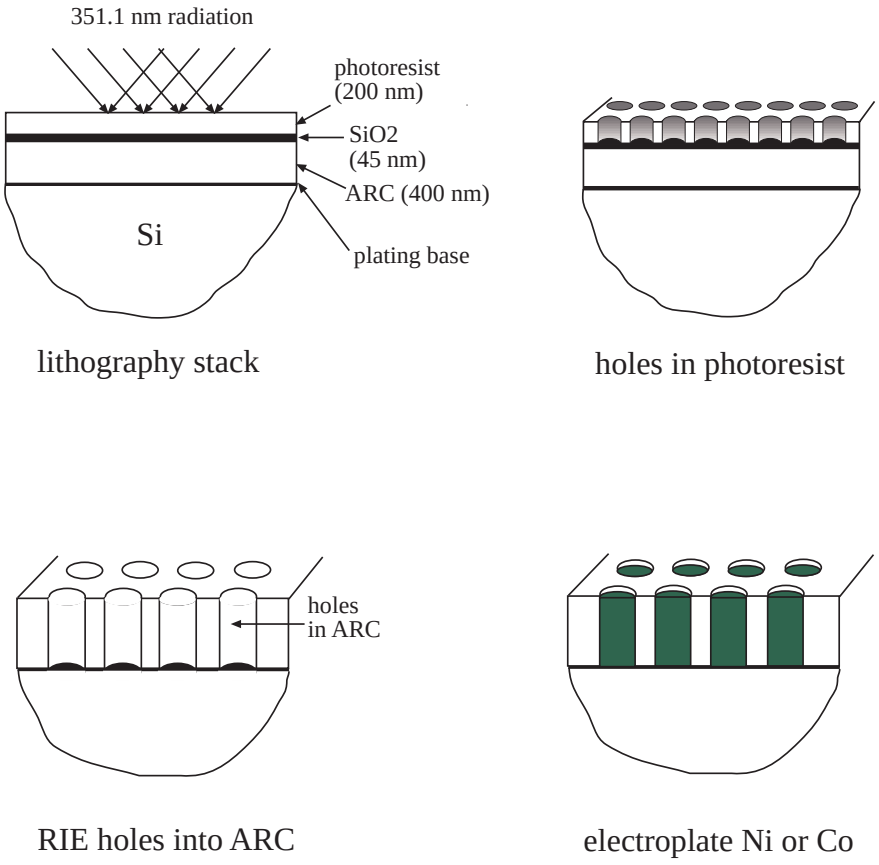

Fig. 18: Schematic of the process currently used to fabricate 100 nm-scale magnetic pillars. Photoresist exposure is by interferometric lithography using the 351 nm line of the Ar ion laser. The antireflection coating (ARC) prevents backreflection from the substrate from interfering with the lithography. Circular holes in the SiO_2 and ARC are created by reactive-ion etching in CHF_3 and O_2, respectively.

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Reading and writing of the information stored in the magnetic pillars appears to be the most formidable problem of the proposed new paradigm. Because the magnetization is vertical, a scheme akin to the magnetic-force microscope with multiple reading heads will presumably be required. Interferometric lithography cannot produce nanopillar arrays in a cylindrically-symmetric configuration compatible with rotating disc reading and writing; it can provide only a Cartesian geometrical arrangement. Accordingly, if interferometric is the lithography of choice, entirely new apparatus for reading and writing must be developed, presumably utilizing micromechanical schemes, such as electrostatic motors that move exclusively in X and Y. If, on the other hand, a rotating scheme is desired, x-ray nanolithography or nanoimprint lithography will be used to produce the nanomagnet arrays. Both of these schemes are compatible with 25 - 50 nm pillar dimensions. Both the x-ray mask and the nanoimprint master would have to be made by scanning electron beam lithography.

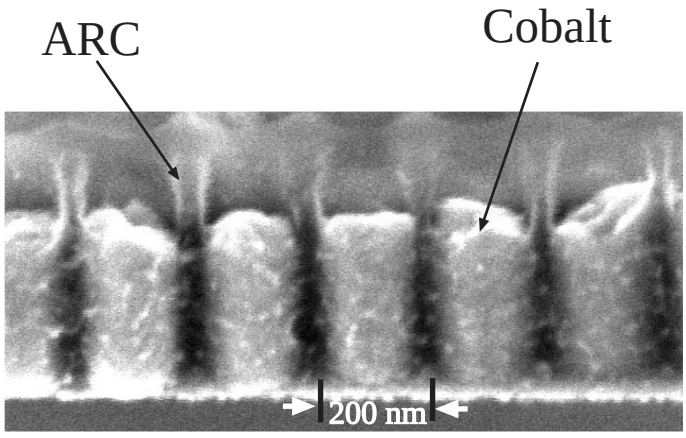

Fig. 19: Scanning-electron micrograph of cobalt pillars electroplated to a height of 200 nm still embedded in ARC. The spatial period is 200 nm.

An important focus of our research will be the basic study of how discrete nanoscale magnets switch direction of magnetization. It has been predicted theoretically that below a certain size, which depends on the magnetic properties of the material, the magnetization will switch coherently. This as well as other mechanisms of switching will be studied. ❑

Integrated Si-MOSFET/FEA

Personnel
C.-Y. Hong
(A. I. Akinwande)

Sponsorship
DARPA

The Field Emission Display (FED) is essentially a thin flat CRT. Unlike a CRT which uses a raster scanned single electron source to generate images on a phosphor screen, the FED generates images by using a two dimensional array of matrix addressed micro-electron sources which are row-scanned and proximity-focused on a phosphor screen. Field emitter arrays operate on the basis of electron tunneling into vacuum when a high electric field is applied to the field emitter tip. The device performance (current density, operating voltage, beam spread, temporal and spatial uniformity) are essentially determined by the characteristics of the energy barrier formed between the emitter (metal or semiconductor) and vacuum. Silicon FEAs have recently been fabricated in our laboratory (see report by Dr. Han Kim) using metal or poly-Si gates. Si FEAs have good emission characteristics and reliability similar to Mo micro-tips. In addition, they are easy to fabricate using silicon microfabrication technology. However, Si FEAs also have temporal and spatial current uniformity problems just like their Mo-tip counterparts. The problems stem from the inherent nature of the electron emission process—electron tunneling through a barrier. Electrons tunnel out of the emitter when the barrier is made narrow by the application of a gate voltage and the enhancement of the tip electric field by using a very sharp tip. The emission current varies exponentially with the applied voltage. Spatial and temporal non-uniformity in the emission current result when small changes occur in the barrier height or width occurs. Traditionally, current non-uniformity and stability have been addressed by adding a series resistor to determine the operating point of the device. At a fixed current, the operating voltage becomes more uniform as the value of the series resistor is increased. In the limit, the best series element for current stabilization is a current source. An effective way to control the field emission current is to add an n-channel MOSFET in series with the FEA. This is relatively easy if the FEA is fabricated on a Si substrate.

Fig. 20: The integrated MOSFET / FEA device structure.

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Other important benefits of integrating Si FEAs with Si n-MOSFET is the ability to (I) drive displays using integrated MOSFET, (ii) implement current drive schemes using the Si-MOSFET and (iii) explore new display architectures through the addition of sophisticated signal processing circuits to the display.

The objective of this project is to demonstrate the integration of Si-MOSFET technology with S-FEAs. The devices we are fabricating have a relatively simple structure in which the n-Si FEA tip is also the drain of the n-MOSFET. The MOSFET has very light doping at the drain to improve its breakdown voltage. This is necessary because the MOSFET must be able to withstand the gate voltage of a field emitter. The proposed Si MOSFET structure is shown in Figure 20. ❑

Low-Power Row and Column Drivers for Field Emission Displays

Personnel

A. Ranadive
(A. I. Akinwande)

Sponsorship

DARPA and NSF Career Award

The Field Emission Display (FED) is being widely studied as a viable alternative to existing flat panel technologies. The FED is an emissive display that has inherent advantages over the existing flat panel displays, higher luminous efficiency, wide viewing angle, low volume and high performance. One aspect of field emission displays that has not received very much attention is the display electronics. Field emission displays, like most other displays, are composed of a matrix of pixels. The display electronics are responsible for addressing and controlling these pixels based upon the data that needs to be displayed. To perform this crucial addressing function, modern flat panel display electronics can consume up to one-third of the power dissipation in the display. Since the trend with portable flat panel displays is to minimize the power consumption, the power dissipation in the display electronics is therefore an important aspect to investigate.

The objective of this research project is to design low-power row and column display drivers based upon the specific requirements of the FED. There were several design requirements for the FED row and column drivers. Functionality requirements included the ability to accommodate eight-bit gray scale (256 gray levels), the ability to introduce column data for a monochrome VGA (640 x 480 resolution) display with 75 Hz refresh rate, and the ability to scan rows and assert data upon the appropriate columns simultaneously. The area requirement was to conform to a pixel pitch size of approximately 200 μm. The row and column drivers are intended to drive a highly capacitive electrode at high voltages. Finally, all of the design must be done with the intention of minimizing the power consumption of the device.

Several approaches were considered to implement the gray scale requirements of the FED, including amplitude modulation and pulse width modulation. Although simple amplitude modulation would have reduced the overall power consumption the best, the performance of

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the FED would suffer at low voltage values due to lack of uniformity. Thus, the decision to use pulse width modulation to achieve gray scale voltages was made. The challenge was then to use low-power techniques to reduce the amount of power consumption with pulse width modulation.

One major technique employed to reduce the power consumption of the row and column drivers was half-power point switching. Pulse width modulation mandates that a consistent voltage level is applied for a portion of the maximum possible time corresponding to the data value desired. For example, for the eight-bit (256) gray scale requirement, the row time is multiplexed into 256 intervals. If we wanted to assert gray level 128, then we would apply a consistent voltage to the output for half of the row time. If we wanted to assert gray level 64, then we would apply a voltage to the output for one-fourth of the row time. Half-power point switching shifts the active period of every odd row time to eliminate one transition every two cycles. Thus the number of transitions is reduced by 50%, and so is the dynamic power dissipation. The essence of half-power point switching is shown in Figure 21.

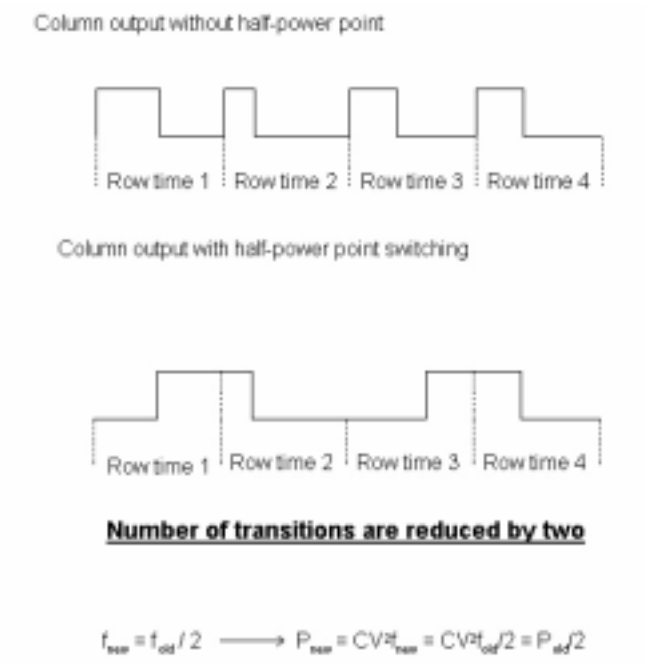

Fig. 21: Half Power Point Switching

A second technique being considered to reduce power consumption involves charge conservation, or energy recovery. We will utilize a large storage capacitor that naturally maintains a DC bias point that is located midway between the low and high voltage transitions. At the beginning of a transition, the output of the row (or column) driver is momentarily isolated from the electrode and is connected to the large storage capacitor. The driver output quickly decays to the potential of the storage capacitor node, which is the half-voltage swing bias point. After this brief configuration, the driver output is again connected to the pixel electrode and then driven to its final voltage value. The benefit of this charge-sharing configuration is that the effective voltage swing is reduced by 50%. The dynamic power dissipation is therefore also reduced by 50% since $P_{dyn} = P_t (C_L V_{swing} V_{DD} f_{clk})$. In the preceding equation, p_t is the probability that a power-consuming transition occurs (the activity factor), C_L is the loading capacitance, V_{swing} is the voltage swing between high and low, V_{DD} is the power supply voltage, and f_{clk} is the clock frequency. We will conduct a feasibility study to determine what the costs and benefits of this charge conservation method would be. ❑