Nanotechnology

Lithographically Defined Isolated CNTs for Field-emission Arrays

S. A. Guerrera, L. F. Velàsquez-Garcìa, A. I. Akinwande
Sponsorship: DARPA

High-current field-emission arrays (FEAs) have garnered much interest in the areas of displays and microwave devices [1]. While most of today's research in field emitters has been performed with field-emission display (FED) applications in mind, there is growing interest in using FEAs as the electron source in high-frequency vacuum electronics to be able to amplify signals extending into the upper millimeter-wave spectral range, where conventional silicon electronics cannot efficiently operate.

State-of-the-art FEAs currently use silicon that has been thinned and sharpened by oxidation to achieve atomically sharp tips or vertically aligned carbon nanotubes (VA-CNTs) [2]-[3] as their emission sources. In the past, the catalyst locations that allow for isolated CNT growth were defined using e-beam lithography and liftoff [4]. However, this method is expensive and low-throughput. Thus, we are moving towards a lithography process that incorporates standard CMOS bulk-processing techniques to attain higher throughput and more repeatable results.

We believe that many field-emitter-array designs are hindered by non-uniform current emission. A central cause of this non-uniform emission could be variations in the radius of each field emitter tip [5]. To combat this variability, we are ballasting each VA-CNT field-emitter tip by incorporating a high-aspect-ratio silicon pillar into each emitter. The current in the silicon pillar saturates at high drain-to-source voltages, resulting in current-voltage characteristics similar to that of an ungated FET. The current source-like behavior of the silicon pillar prevents destructive joule heating in the sharper tips while still allowing duller tips to emit, potentially leading to higher overall current emission, better uniformity, and higher reliability.

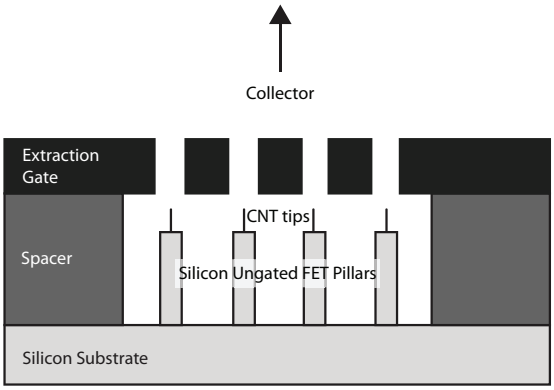

FIGURE 1: Schematic diagram of the CNT field emitters with ballasting ungated FETs.

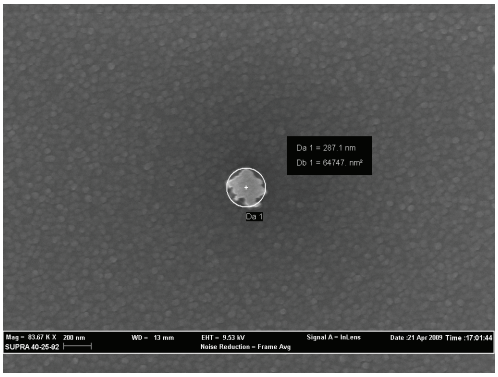

FIGURE 2: One CNT catalyst dot on silicon before etching, part of a 388x888 array with 10µm spacing. The dot is sized such that isolated CNTs will be formed.

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PECVD CNT-based Gas Ionizers for Portable Mass Spectrometry

L. F. Velásquez-García, A. I. Akinwande
Sponsorship: DARPA

MEMS-based analytical instrumentation has been actively researched for over a decade. In particular, efforts have focused on developing rugged gas chromatography and mass spectrometry (GC/MS) systems that are smaller, lighter, cheaper, faster, and more power-efficient [1]. Pumping requirements drive the power consumption, size, and weight of these systems. Therefore, relaxation of the pressure level at which the system components can operate would enable its portability. Portable GC/MS systems, either as individual units or as parts of massive networks, can be used in a wide range of applications including *in-situ* geological survey, law enforcement, environmental monitoring, and space exploration [2]-[3].

The ionizer is a core component of an MS system. We report the fabrication and experimental characterization of a novel low-cost carbon nanotube (CNT)-based electron-impact ionizer (EII) with an integrated gate for portable mass-spectrometry applications. The device achieves low-voltage ionization using sparse forests of plasma-enhanced chemical-vapor-deposited (PECVD) CNT field-emitter tips, and a proximal gate with open apertures to facilitate electron transmission. The gate is integrated using a deep-reactive-ion-etched (DRIE) spring-based high-voltage MEMS packaging technology [4]-[5]. The device also includes a high aspect-ratio silicon structure (μfoam) that facilitates sparse CNT growth and limits the electron current per emitter [6]. The devices were tested as field emitters in a high vacuum (10^{-8} Torr). Electron emission starts at a gate voltage of 110 V and reaches a current of 9 uA at 250 V (2.25 mW) with more than 55% of the electrons transmitted through the gate apertures. The devices were also tested as electron-impact-ionizers using Argon. The experimental data demonstrate that CNT-EIIs can operate at mtorr-level pressures while delivering 60 nA of ion current at 250 V with about 1% ionization efficiency. Figure 1 shows a cross-section schematic and a picture of a fabricated ionizer; Figure 2 shows experimental data that demonstrate that the ionizers work as described by the electron-impact-ionization model.

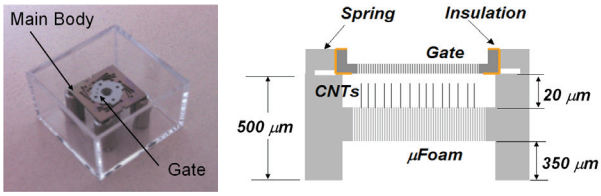

FIGURE 1: A fabricated PECVD CNT-based ionizer (left) and cross-section schematic (right).

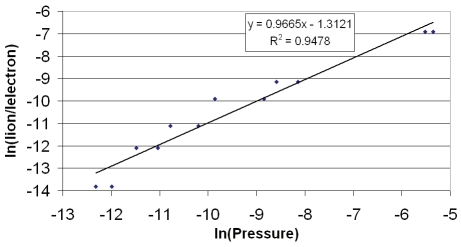

FIGURE 2: Ratio of ion current to electron current vs. pressure. Ideally, the data from electron impact ionization describes a line with slope 1 using a log-log plot. The experimental data describes a line (R^2=0.95) with slope 0.97.

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Sub-40-nm Patterning of Au of GaAs for Nanowire Catalysis

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Sponsorship: IBM, SRC/FCRP MSD

In this work, we demonstrate sub-40-nm patterning of Au features on GaAs substrates using a bilayer-resist structure. Patterning of small Au features onto GaAs substrates is of particular interest due to their use as metal catalysts for GaAs and GaAs-alloy nanowire growth. Semiconducting nanowires have a variety of potential applications, such as field-effect transistors (FETs) [1], and their size-dependent properties have been exploited for a variety of optoelectronic devices [2]. However, much work remains in creating lithographically-templated nanowires for integration into future manufacturing processes.

Au in particular has shown particular promise in producing oriented, size-selected nanowires [3]. While the patterning of Au features onto other III-V materials, such as InP, has been demonstrated down to 50 nm [4], sub-100-nm patterning of Au on GaAs has not been demonstrated, due to the poor adhesion of Au onto GaAs substrates. Because nanowire diameter exhibits a strong dependence on catalyst particle size [5], the smallest-diameter nanowire that can be grown is limited. With use of a bilayer-resist process and the introduction of a Cr adhesion layer, metal feature sizes under 40 nm were achieved.

The bilayer-resist structures used had a 50-nm-thick top layer of polymethyl methacrylate (PMMA) and a bottom layer of polymethyl glutarimide (PMGI) with thicknesses between 50 and 150 nanometers. The PMMA/PMGI resist stack was exposed by electron-beam lithography, and then the PMMA and PMGI layers were developed in turn. The PMMA layer was first developed by a cold development process [6], and then a controlled undercut was created in the PMGI layer [7]. A metal stack of Au and Cr was evaporated, with the Cr serving as an adhesion layer. Using a 3-nm-thickness of Cr, we were able to create sub-40-nm metal structures. These structures were subsequently used to grow GaAs nanowires by metal-organic chemical-vapor deposition (MOCVD) with diameters as small as 30 nm.

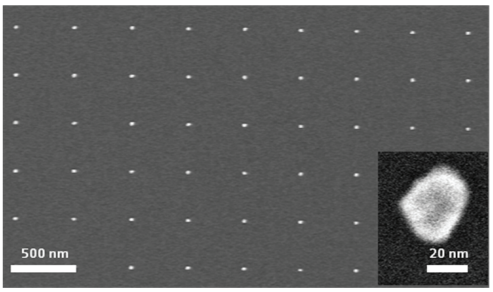

FIGURE 1: An array of sub-40-nm-diameter features consisting of a metal stack of 10-nm Au atop 3-nm Cr on a GaAs substrate, deposited by metal-evaporation onto a patterned PMMA/PMGI bilayer resist stack.

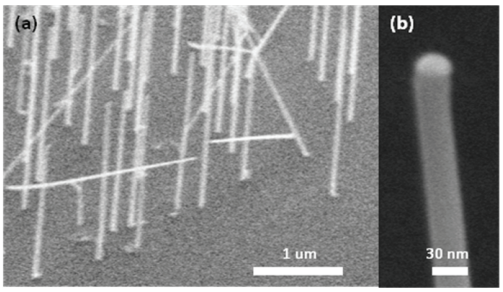

FIGURE 2: (a) An array of GaAs nanowires grown epitaxially by MOCVD, catalyzed by patterned Au/Cr metal features. (b) A 30-nm-diameter GaAs nanowire, with the metal catalyst clearly visible at the top of the nanowire.

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High-resolution Lithography with a Focused Helium-ion Beam

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Sponsorship: NSF GRFP (D. Winston), NSF NNIN, NRI/INDEX

Focused-ion-beam lithography [1] is not as widely practiced as scanning-electron-beam lithography for resist-patterning, in part due to resolution constraints and in part due to substrate sputtering. However, helium ions in particular may enable nanostructure fabrication with higher resolution than electrons. The over-three-orders-of-magnitude higher mass of helium ions relative to electrons should reduce lateral scattering in the resist, thus conceivably enabling patterning of small features at higher density than is possible with electron-beam lithography. Helium ions achieved ~ 200 nm lithographic resolution as early as twenty years ago [2], but only recently has a scanning-helium-ion-beam column been engineered with a focused spot size on par with electron beam columns [3]; the specified spot size of this commercial system is below 1 nm. We have used a commercial scanning helium-ion microscope to demonstrate lithography of hydrogen silsesquioxane (HSQ) on silicon. The HSQ is already used as a high-resolution electron-beam resist [4], and it permits high-resolution inspection after development in a scanning-electron microscope without requiring pattern transfer. As shown in Figure 1 and Figure 2, sub-20-nm feature sizes were achieved.

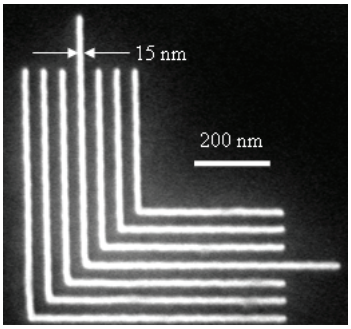

FIGURE 1: Scanning-electron micrograph of 46-nm-pitch nested "Ls," patterned in a 30-nm-thick layer of HSQ on silicon.

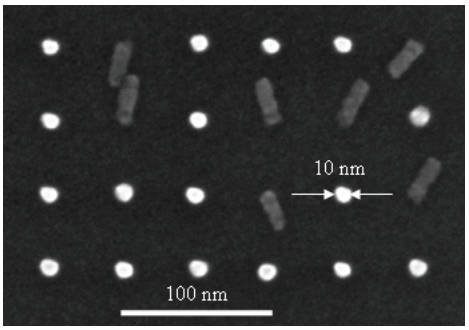

FIGURE 2: Scanning-electron micrograph of a 46-nm-pitch pillar array, patterned in a 30-nm-thick layer of HSQ on silicon. This image was chosen to show the pillars' 3:1 aspect ratio and good edge profile, as some of them have fallen. Exposing with a higher dose prevents pillar collapse.

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Controlled Self-assembly of Linear Structures for Nanoscale-device Fabrication

J. K. W. Yang, Y. S. Jung, J. Chang, C. A. Ross, K. K. Berggren
Sponsorship: NRI/INDEX, ONR

Electron-beam lithography (EBL) has sub-10-nm patterning performance with good pattern registration. However, it is slow and not economical for patterning dense structures over large areas. Alternatively, block-copolymer (BCP) self-assembly can form nanostructures economically and in parallel over large areas, but it lacks global registration. Fortunately, EBL can be combined with BCP self-assembly to overcome their collective shortcomings. The result is a nano-manufacturing approach that achieves high resolution, registration accuracy, and throughput. This approach was demonstrated previously using sparse arrays of EBL-patterned templates to guide BCPs into ordered periodic structures [1-3]. However, periodic structures have limited utility, and one needs controlled but arbitrary patterns in device fabrication.

Here, we controlled cylindrical morphology BCP into line structures that resembled integrated-circuit interconnects and dense nanowire arrays. In addition to achieving long-range order, we were also able to direct the local orientation of individual BCP microdomains into various geometries. In the examples shown here, the structures were made with an effective increase in throughput, as the EBL exposed only a fraction of the patterns and the BCP completed the missing structures.

Without a guiding template, the BCP lines were locally ordered but globally disordered. To achieve global ordering, we used a template consisting of a sparse array of nanoposts fabricated by EBL patterning of hydrogen silsesquioxane (HSQ) resist [4]. As shown in Figure 1, an array of EBL-patterned HSQ nanoposts (bright dots) arranged in a rectangular array successfully guided a subsequently applied film of PS-PDMS BCP into well-ordered lines. The different orientations of the lines were achieved by increasing the spacings between the posts in the template.

To achieve arbitrary pattern formation, we broke the symmetry of the template by using "dash" structures instead of circular posts, and strategic positioning of the posts. Figure 2A shows that an array of dashes was able to guide the BCP into accurately-positioned bends. Furthermore, as shown in Figure 2C, we were able to locally control individual BCP microdomains into meandering lines by strategic positioning of posts. The resulting well-controlled linear structures have potential for use in the fabrication of integrated circuit interconnects and dense nanowire arrays.

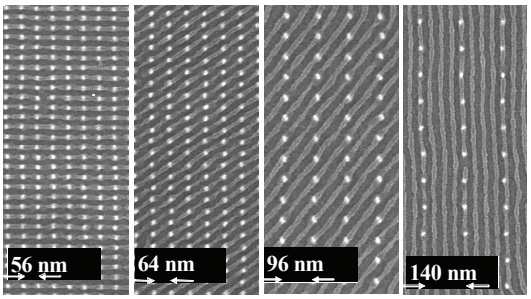

FIGURE 1: An SEM of the self-assembly of cylindrical-phase block copolymers (BCP) that were guided by an electron-beam-patterned template of HSQ nanoposts (bright dots) to form ordered gratings of lines. The progression of grating orientations from horizontal to vertical from left to right occurred due to the tendency of the BCP to preserve its natural period of ~35 nm even as the template-spacing was increased.

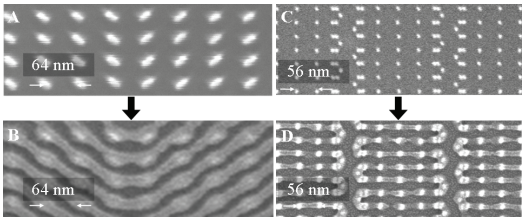

FIGURE 2: (A) An SEM of a template consisting of dashes arranged such that the BCP that aligns along the dashes will form bends as shown in (B). (C) An SEM of a template consisting of an arrangement of posts designed to guide the BCP into an array of meandering structures as shown in (D).

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Understanding Hydrogen Silsesquioxane Resist for Sub-5-nm Half-pitch Electron-beam Lithography

J. K. W. Yang, B. Cord, J. Klingfus, J. Chang, S. Nam, K. Kim, M. J. Rooks, K. K. Berggren
Sponsorship: NRI/INDEX, INSIC

Electron-beam lithography (EBL) provides one of the highest achievable patterning resolutions. As demonstrated by electron-beam induced deposition (EBID) methods, patterns as small as 1.6-nm-half-pitch can be achieved [1]. However, EBID methods are typically orders of magnitude slower, due to the high exposure doses required, and less reproducible than resist-based processes. Therefore, EBID is less practical in patterning high-resolution structures over large areas.

On the other hand, the resist-based process using EBL exposure of hydrogen silsesquioxane (HSQ) resist is a promising approach for patterning high-resolution structures due to its higher speed (compared to EBID) and the high etch-resistance of HSQ. In the past, we demonstrated the patterning of 7-nm-half-pitch structures using this process followed by a high-contrast salty-development step [2]. However, the development mechanism of HSQ was not well understood.

Here, we report on progress in understanding the contrast enhancement mechanism in HSQ and demonstrate 4.5-nm half-pitch structures using this resist-based process. Figure 1 shows a SEM of 4.5-nm half-pitch nested-"L" structures patterned using Raith's latest EBL tool, the Raith 150TWO at 10 kV acceleration voltage in 10 nm-thick HSQ resist. Patterning at 10 kV instead of higher acceleration voltages sped-up our exposures without significant loss in resolution. To the best of our knowledge, this is the highest resolution achieved using resist-based EBL to date.

The development of HSQ is self-limiting, i.e., development stops beyond a certain development time. This self-limiting nature of the development process often results in footing between closely spaced structures and limits resolution. However, as shown in Figure 2, the addition of NaCl salt to the NaOH developer appears to allow continued resist development, which resulted in further contrast enhancement with increasing development time. This effect was not seen in development in NaOH alone without salt.

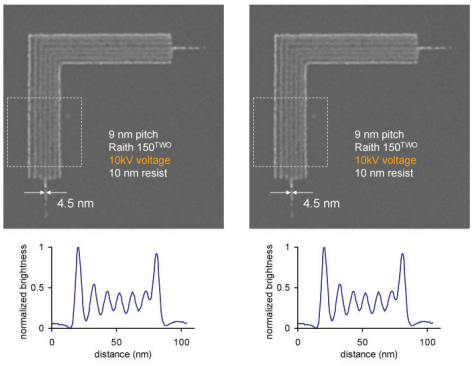

FIGURE 1: (Left) An SEM of 4.5-nm-half-pitch nested-"L" structures patterned using a Raith 150TWO EBL at 10 kV acceleration voltage in 10-nm-thick HSQ. (Right) The plots of normalized brightness vs. distance at the bottom of both images were obtained by averaging the brightness values of the SEM image along the length of the HSQ lines within the dashed rectangles shown.

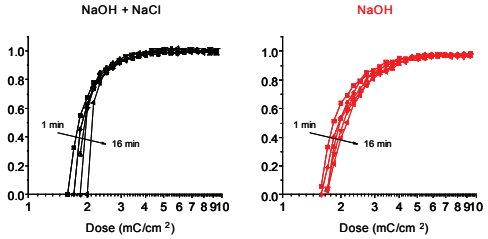

FIGURE 2: Contrast curves for HSQ developed in 1% wt NaOH, 4% wt NaCl solution for HSQ exposed by 100 keV energy electrons and developed for 1, 2, 4, 8, and 16 mins. Plots show improvement in contrast with increasing development time. The addition of salt appears to enable continued development.

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Advanced Planarization Technology

J. Johnson, W. Fan, D. S. Boning

Sponsorship: SEMATECH/SRC Engineering Research Center for Environmentally Benign Semiconductor Manufacturing, National Semiconductor, JSR

Benchmark modeling work has been conducted in the Boning Group investigating a critical and costly process in silicon integrated circuit (IC) fabrication process. chemical mechanical polishing or planarization (CMP). However, challenging device dimensions, novel materials, and advanced toolsets call for a deeper level of physical understanding and more empirically sensitive models. Therefore, two transformative approaches to better understanding and modeling of CMP have been undertaken.

First, die-level modeling of STI CMP using novel slurries like Ceria are currently being explored. However, in experiments using traditional Silica slurries, more effective ways of modeling have been discovered. Pattern-density models in the Boning Group have evolved; however, none of these models have explored the evolution of pattern density itself. Current work is seeking to model the change in pattern density and deposition profiles as a response to step-height reduction over time in order to enhance the model specificity and, consequently, accuracy. We believe that pattern density will increase parabolically as the step height decreases (i.e., time increases), and have proved this experimentally as shown in Figure 1.

Second, previous assumptions that the CMP pad surface has the same Young's modulus as the bulk were reassessed. Comparison of the most current CMP model with the direct measurement of a JSR pad shows that the model's extracted bulk modulus proved to be on the order of five times higher than the actual measured result. In order to attribute this discrepancy to either a high surface modulus or a high bulk Poisson's ratio, a preliminary experimental study was performed using nanoindentation measurement techniques as shown in Figure 2. Current work is exploring the statistical confidence of the technique and its incorporation of the proper modulus towards a more physically accurate die-level CMP model.

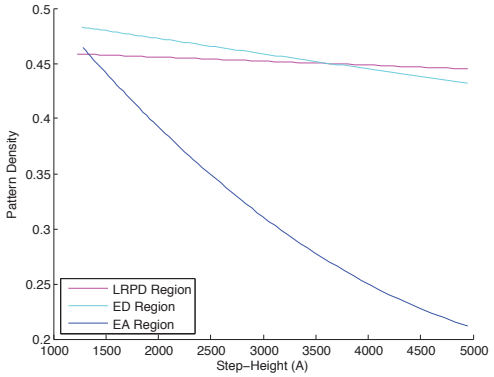

FIGURE 1: Local pattern density, ρ, as a function of step height, h, observed a decrease of almost 40% over the course of the STI CMP process in areas with structures <10μm in length.

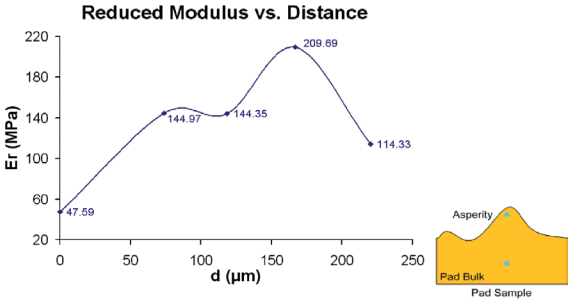

FIGURE 2: The first successful scan of nanoindentation on a JSR pad follows the hypothesized trend of pad asperity effective modulus being significantly less than that of the pad bulk effective modulus.

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Modeling of Nanoimprint Lithography

H. K. Taylor, D. S. Boning

Sponsorship: Singapore-MIT Alliance

Nanoimprint lithography (NIL) enjoys growing interest, particularly for the fabrication of bit-patterned hard disk drives and solid-state memories. In NIL, a thermoplastic or ultraviolet-curing resist material is imprinted with a re-usable stamp. Full adoption of the technique is difficult to envisage without reliable methods for simulating the parasitic elastic distortions of the stamp that occur during imprinting, as well as for predicting any locations of incomplete pattern replication. Conventional mechanical simulation techniques are far too slow to extend to the feature-rich patterns of complete devices. Building on our earlier work simulating pattern dependencies in thermoplastic micro-embossing [1], [2], we are developing a computationally inexpensive method for simulating NIL.

Our work currently models the imprinting of spun-on thermoplastic resists and is being extended to the so-called "step-and-flash" ultraviolet-curing variant of nanoimprint. We describe the mechanical behaviors of the resist and the stamp using the responses of their surface profiles to a normally-applied impulse in space and in time. The overall topography of the resist for any given stamp pattern is predicted through a series of steps in which the resist's impulse response is convolved with an iteratively-found estimate of the time-evolving stamp–resist contact-pressure distribution. Preliminary experiments conducted in the MTL show that the method successfully captures key pattern interactions at the micron scale (Figure 1) [3]. A simple modification of the simulation method has shown promise for modeling the shear-thinning resist behavior that can occur in NIL (Figure 2). Using this simulation method, we expect to be able to explore a set of design-correction strategies with the aim of reducing parasitic stamp deflections. We are currently seeking to calibrate the method for a range of nanoimprint resist materials and to this end are keen to work with any interested industrial NIL users.

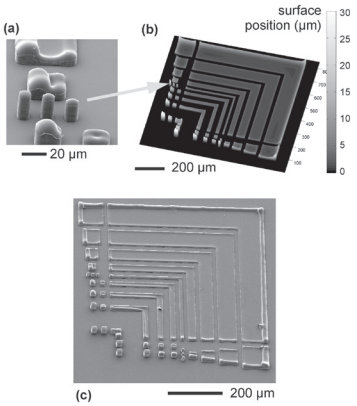

FIGURE 1: Comparison of experiment with simulation in the micron-scale embossing of a 2.2-μm polysulfone layer, spun onto silicon. Embossing was performed at 205 °C under 30 MPa for 2 minutes. Scanning electron micrographs of the sample (a, c) and a 3-D plot of the simulated topography (b) show close agreement.

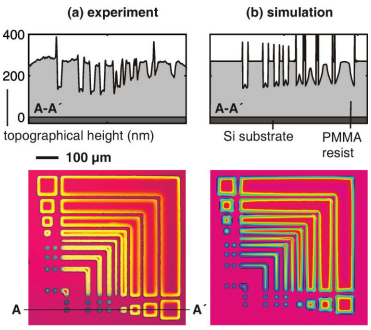

FIGURE 2: Comparison of experiment (a) with simulation (b) in the micron-scale embossing of a 270-nm-thick PMMA layer, spun onto silicon. Embossing was performed at 165 °C under 40 MPa for 2 minutes. Optical interferograms (lower) and cross-sections (upper) are shown. The experimental cross-section was obtained, using white-light interferometry, from an elastomeric casting of the imprinted layer. The simulation incorporates elastic deflections of the silicon stamp and shear-thinning of the PMMA resist.

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Carbon Nano-switches for Low-leakage Circuit Applications

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Sponsorship: SRC/FCRP IFC, DARPA

Nanoelectromechanical switches (NEMS) exhibit minimal leakage current in the off state. Consequently, they may find application in low-power electronics. This work focuses on the fabrication of a vertically oriented nano-switch using a carbon fiber or nanotube as the active component. Figure 1 shows the device schematic, and Figure 2 shows an SEM image of a fabricated nano-switch. The device consists of a line of carbon nanofibers grown directly on a highly doped silicon substrate between two contacts that are electrically isolated from the substrate by an insulator. The device is actuated when a voltage is applied between the substrate and one of the contacts. This voltage causes the nanofibers to be pulled into and eventually make physical contact with one of the contacts, which allows current to flow between the substrate and the contact.

One of the primary benefits of the nano-switch is that it has extremely low leakage current because a physical gap separates the nanotube from the contact during the off state. One possible application that takes advantage of the reduced leakage is power-gating idle circuit blocks. The nano-switch is connected as a header switch between the power supply and the load circuit. During normal operation, the nano-switch acts as a short circuit and power is supplied to the load circuit. When the circuit is not in use, the nano-switch is opened and the supply voltage is disconnected to reduce power consumption. This technique is similar to power-gating with a high threshold CMOS device, but the nano-switch provides extra power savings because it has even less leakage current.

A CMOS test chip has been designed to quantify the power savings of the nano-switch for this power-gating application. The chip also implements proof-of-concept SRAM and reconfigurable interconnect circuits that explore other potential benefits of the nano-switch. The basic device fabrication process has been developed, and the nano-switches are currently being optimized for performance.

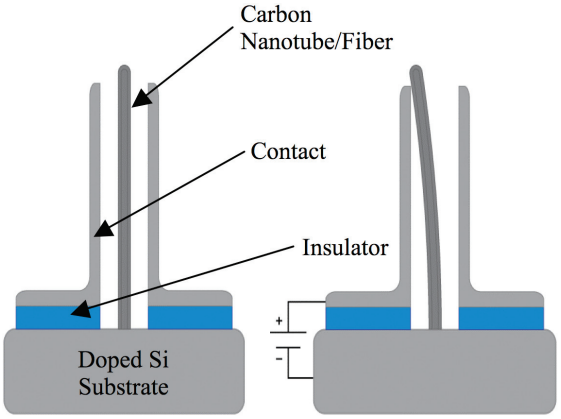

FIGURE 1: Left) Schematic of a vertically oriented carbon nano-switch. Right) Carbon nano-switch upon actuation using an applied voltage between the substrate (i.e., tube) and a contact.

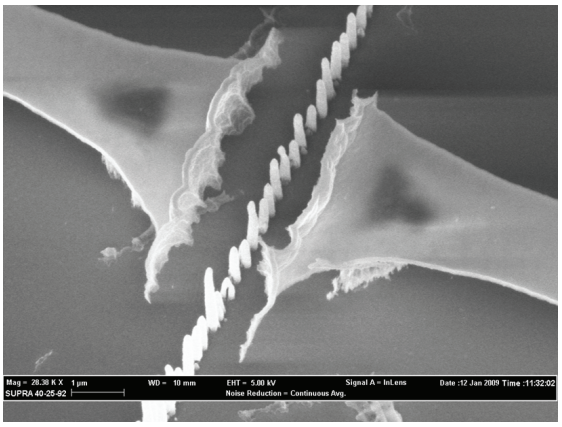

FIGURE 2: An SEM image of a fabricated carbon nanofiber-based nano-switch.

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Control of Carbon Nanotube Geometry via Tunable Process Parameters

M. A. Cullinan, M. L. Culpepper
Sponsorship: Chang Innovation Grant, Pappalardo Fellowship

Carbon nanotubes (CNTs) are well–suited for use in flexure-based nanomechanical devices because CNTs possess both a high elastic modulus (~1 TPa) and failure strains of up to 40%. These properties, combined with CNTs' low mass-per-unit volume, make it possible for CNT–based devices to exhibit three characteristics that are useful in nano–scale devices: (1) vibration frequencies in lateral bending that may exceed of 10s of GHz, (2) high energy storage per unit mass, and (3) large ranges of motion relative to their size. In this research we created a growth model that was generated via statistical and experimental analysis. Using this growth model, a method was created for selecting fabrication process parameters that may be used to grow carbon nanotubes with a specified outside diameter and number of walls. The diameter and number of walls are controlled by adjusting several growth parameters: temperature, catalyst film thickness, and hydrocarbon concentration. Figure 1 shows the results of the CNT growth for one set of process parameters; Figure 2 shows the relationship between CNT diameter and wall thickness for a variety of process parameters. The capability to control diameter and number of walls enables the control of rigidity, which in turn makes it possible to control a CNT's lateral vibration behavior and bending stiffness. The growth model was therefore used to design growth process for specific applications. Experimental results showed that the models predicted average outside diameter and number of walls within the growth with less than 6% and 7% error, respectively. Based on the measured geometries, it was estimated that the stiffness and natural frequency can be accurately controlled to within 1.5% of the desired values.

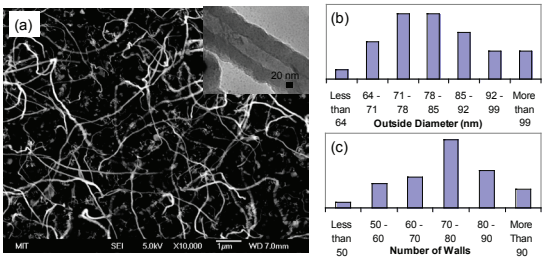

FIGURE 1: (A) SEM image with inset TEM image of sample from run 15 with F = 3nm, T = 800°C, and Cm = 68.5%. (B) Histogram of CNT outside diameter for run 15. (C) Histogram of number of walls in CNT for run 15.

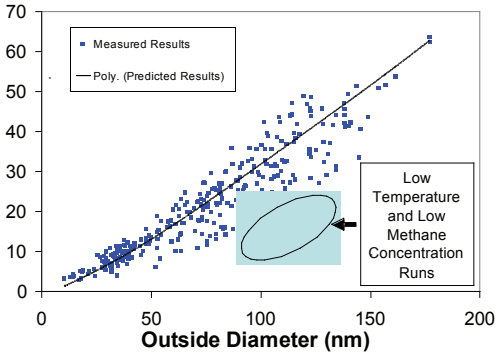

FIGURE 2: Model predictions vs. measured values for CNT growth.

Towards Controlled Doping in III-V Semiconductor Nanowires

M J. Tambe, M. J. Smith, S. Gradečak
Sponsorship: NSF, MITEI, MTL

Nanowires are quasi-one-dimensional single crystals with lateral dimensions that can be scaled-down to only a few nanometers. They can simultaneously act as active components and interconnects and therefore fulfill the two basic functions of any active device. However, controlled doping of III-V nanowires is challenging due to strong Fermi-level pinning as well as the kinetic and thermodynamic requirements for dopant incorporation through the metal catalyst. To enable flexible and controllable doping of nanowires we are studying two doping approaches: doping through the deposition of a doped epitaxial shell around the nanowire [1] and *ex-situ* post-growth diffusion doping. Here we concentrate on GaAs nanowires as a model system, although our approaches are applicable to other III-V nanowires.

Shell doping is proposed as a simple *in-situ* doping method. After GaAs nanowires are grown at 420°C, the reactor temperature is increased to 750°C and silane is introduced during the growth of a conformal GaAs shell, as shown in Figure 1a. Experiments have shown that uniform shells can be achieved, as shown in Figure 1b. To overcome Fermi-level pinning, the shells must be thick and/or heavily doped. Schrödinger-Poisson models predict that at $N_D = 10^{18} cm^{-3}$, the minimum shell thickness to achieve doping is 48nm. Experimental studies to validate this prediction and determine the dependence of carrier concentration on shell thickness are currently in progress. We have optimized the design and fabrication of robust, Ohmic electrical contacts onto GaAs nanowires with sufficiently low contact resistance. The contacts are patterned using e-beam lithography followed by e-beam evaporation of Ni(20 nm), Ge (20 nm), and then Au (120 nm). The contacts are then annealed at 420°C for 30 seconds.

To achieve precise control over diffusion doping at the nanoscale, we propose a platform for finely tunable dopant dosages via the creation of a monolayer of dopant-containing molecules [2] on GaAs. First, the GaAs surface is hydrolyzed [3] to create reactive sites for monolayer formation. A controlled dose of silicon is introduced by reacting (3-Mercapto-propyl) trimethoxysiloxane (MPTMS) with the hydroxyl groups on the surface (Figure 2). Silicon atoms are then driven in by a rapid thermal anneal. X-ray Photoelectron Spectroscopy analysis supports the proposed surface functionalization. Preliminary sheet resistance measurements suggest that this platform can be used to dope GaAs. An investigation of dopant dosage control is underway.

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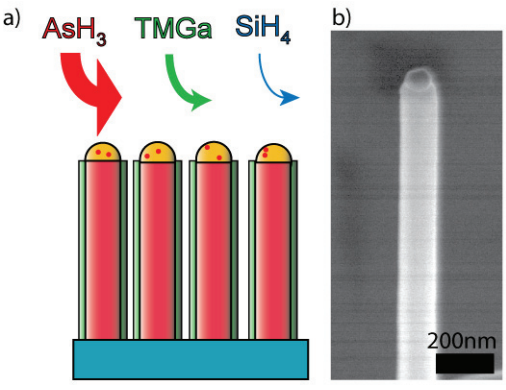

FIGURE 1: a) Schematic of shell doping via co-introduction of silence during epitaxial shell deposition. b) An SEM image of shell-doped GaAs NW. The dark object on the top of the nanowire is the Au catalyst nanoparticle.

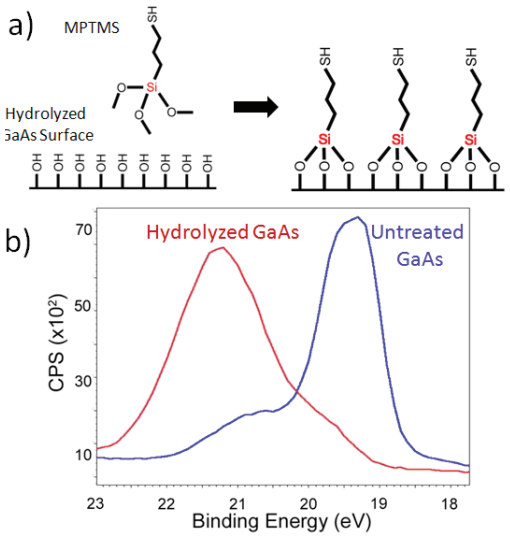

FIGURE 2: a) Idealized reaction between MPTMS and hydrolyzed GaAs. Silicon, the n-type dopant, is highlighted in red. b) X-ray Photoelectron Spectroscopy peak shifts suggest a hydrolyzed GaAs surface.

Supercritical Microfluidic Synthesis of Nanomaterials

S. Basak, S. Marre, J. Bake, M. Bawendi, K. F. Jensen
Sponsorship: NSF, ARO – ISN

Nano-sized materials are of interest for modern technological applications such as reinforced lightweight materials, catalysts, sensors, fuel cells, and medical diagnosis and treatments due to improved chemical, mechanical, optical and functional properties compared to bulk materials. Significant effort has been focused on the ability to control the nanoscale structures via innovative synthetic approaches. Synthesis of nano-sized specialty materials using a multistep batch process suffers from problems in reproducibility of size, size distribution, and purity. Under such situations, the challenge is to find alternate methods or make improvements in the existing processes.

Continuous laminar flow reactors based on microfluidics, integrated with fluid flow, heat, and pressure control elements offer a solution to these problems as well as additional advantages, including feedback control of temperature and feed streams, reproducibility, potential for *in situ* detection for reaction monitoring, rapid screening of parameters, and low reagent consumption during optimization. We have demonstrated a continuous supercritical microfluidic method for synthesis of nanosized oxide materials (Figure 1). Decomposition of iron pentacarbonyl in hexane to produce iron oxide under 70 bar pressure and between 220 – 300°C temperature is studied as a model system. Oleic acid and lauric acid are used as surfactant to reduce the agglomeration of nanoparticles inside the reactor channels. At operating pressure, the solvent hexane turns supercritical above 234°C. The supercritical hexane provides a better control over the particle size distribution and morphology, which makes this technology advantageous compared with conventional techniques.

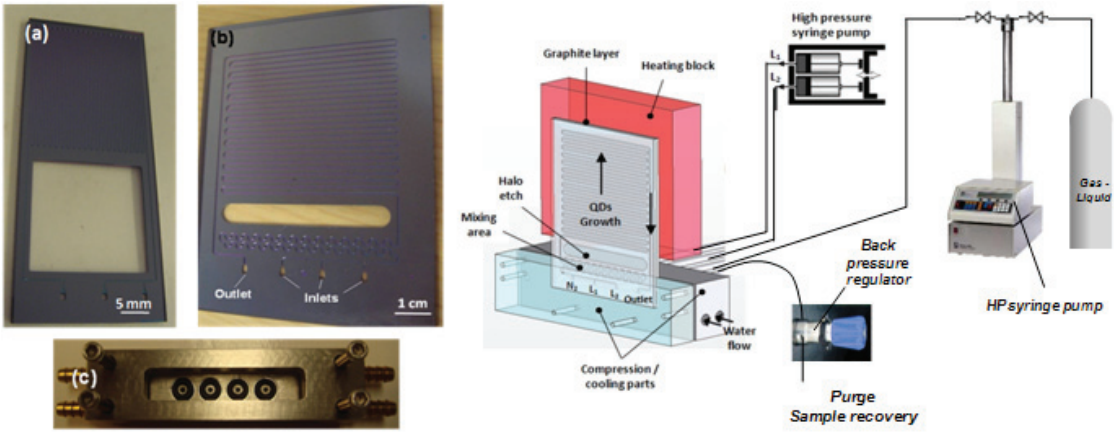

FIGURE 1: Left: High-pressure microreactors for nanomaterials synthesis: (a) 45-µL microreactor, (b) 100-µL microreactor and (c) modular high-pressure fluidic connections. Right: High-pressure experimental set-up including a high-pressure, high-temperature microreactor, a compression-cooling aluminum part, two high-pressure syringe pumps, and a back-pressure regulator.

Synthesis of Single-walled Carbon Nanotube Thin Films via Electrostatic-spray-assisted Chemical Vapor-deposition

M. Hofmann, Y. P. Hsieh, J. Kong
Sponsorship: SRC/FCRP IFC, Intel Corporation

In our work, electrostatic-spray-assisted chemical vapor-deposition is used to grow floating single-walled carbon nanotubes and directly deposit nanotube thin films on a substrate.

The catalyst solution was finely dispersed by a strong electrical field and injected into the heated reaction zone during the growth. The size of the aerosol was found to be affected by electrospraying parameters. Carbon nanotubes are nucleating from these aerosols and grow as they travel through the reaction zone. This process offers a versatile test bed for fundamental studies of nanotube growth since the aerosol is found to be unperturbed from substrate interaction and individual carbon nanotubes are produced.

The nanotubes can be efficiently deposited on a cooled sample holder that is reaching into the reaction zone. This result is promising for thin-film application since nanotubes can be deposited on a variety of cooled substrates that are otherwise not compatible with the CVD environment. Finally, the fabrication of free-standing suspended nanotube films was demonstrated.

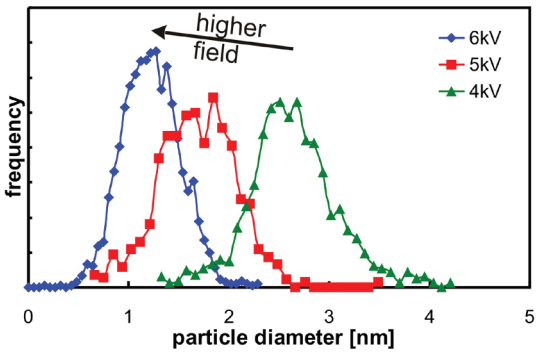

FIGURE 1: Diameter distributions of aerosol generated with different acceleration voltages.

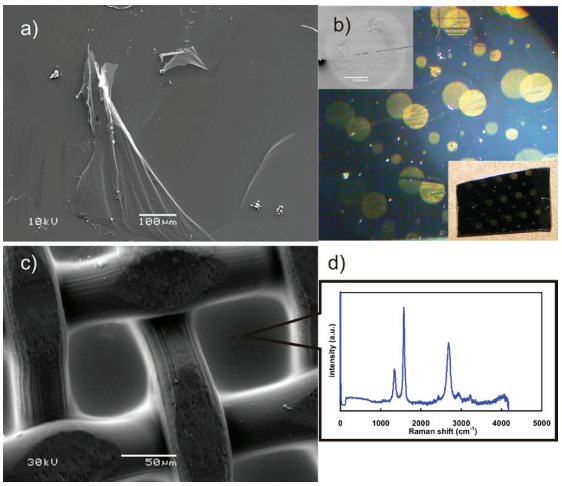

FIGURE 2: a) An SEM image of damage in the continuous CNT film, b) CNT patterns generated by shadow-masking technique, c) SEM image of a suspended nanotube film on stainless steel mesh, and d) Raman spectrum and indication of position obtained.

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Integrated Graphene Interconnects

K.-J. Lee, A. P. Chandrakasan, J. Kong
Sponsorship: SRC/FCRP IFC

As process technology scales, the importance of material and architectural innovation on interconnect performance will continue to increase. Graphene has gathered much interest as a possible replacement for copper interconnects due to its large carrier mobility and current carrying capacity. Graphene sheets are also an attractive alternative to carbon nanotube-based interconnects as they are more compatible with conventional lithography methods. This project proposes to integrate high-density graphene ribbons and characterize their properties as global interconnects. The main objectives of this project are to achieve high density integration of graphene with CMOS, reduce overall power consumption by low-swing signaling, and characterize the performance (delay, energy, noise, etc.) of graphene interconnects.

This project will focus on low-swing signaling, primarily as a power-reduction technique for on-chip communication. During the design phase, low-swing drivers/receivers will be benchmarked using existing graphene circuit models [1]. Similar to work in [2], graphene sheets are grown on a separate substrate by chemical vapor deposition, and then they are transferred on top of the completed CMOS chip using an adhesion layer. Unlike the integration process of carbon nanotubes [3], the use of graphene enables lithographic patterning, which allows the large graphene sheet to be patterned and etched into mm-length interconnect wires. Bare SiO_2/Si chips have been used as prototypes to fabricate graphene wires up to 1 mm in length, with an effective sheet resistance of 700 – 900 Ohms/sq.

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Fabrication of Graphene Nanostructures Using Thermally-activated Nickel Nanoparticles

L. C. Campos, V. R. Manfrinato, J. D. Sanchez-Yamagishi, J. Kong, P. Jarillo-Herrero
Sponsorship: Department of Physics, MIT; Department of Electrical Engineering and Computer Science, MIT; Departamento de Física, Universidade Federal de Minas Gerais; Departamento de Engenharia de Sistemas Eletrônicos, Escola Politécnica, Universidade de São Paulo

Graphene, a single atomic layer of graphite, holds many exciting possibilities for demonstrating new physics as well as novel electronic applications [1], many of which can be realized only by confining graphene into nanoribbons and other nanostructures. When confined on the nanometer scale, the edges of a graphene device play an important role in determining its electronic and magnetic properties. For example, it is predicted that graphene nanoribbons with crystallographically-defined edges could be key to realizing fast ballistic field-effect transistors [2] or room-temperature spintronic devices [3]. To date, though, no effective method to produce single-layer graphene structures with well-defined crystallographic edges has been found.

Our research has focused on this problem, and we have successfully developed the first anisotropic etching process in isolated single-layer graphene. This etching process produces nanoribbons and other continuously connected nanostructures with edges aligned along a single crystallographic-direction. The nanoribbons are obtained in sub-10nm geometries, with edges smooth on the nanometer scale, and they should provide a wealth of interesting new experiments from its unique crystallographic orientation. For example, previous graphene nanoribbon field effect transistors were limited by having disordered edges; since our nanoribbons are aligned along crystallographic directions with smooth edges, they should feature much better FET operation. Moreover, we often obtain nanoribbons and other nanostructures connected in continuous graphene circuits, one example being a nanometer-scale equilateral triangle connected to a series of nanoribbons and other more complicated geometries. Previous studies have worked on tailoring graphene into nanocircuits, but these are the first graphene nanocircuits that can exploit the potential of graphene's edge-physics.

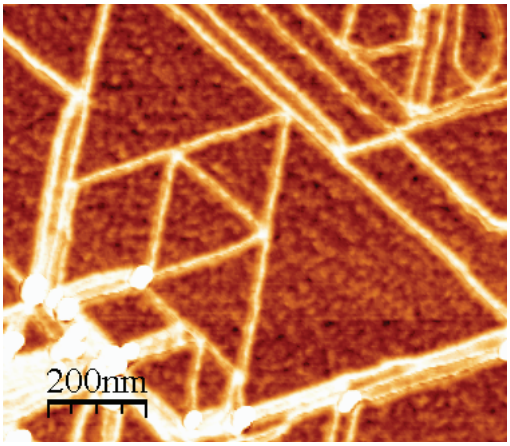

FIGURE 1: An AFM image of the trenches produced by thermally-activated nickel nanoparticles etching across single-layer graphene. The trenches run along straight lines, following a single crystallographic orientation.

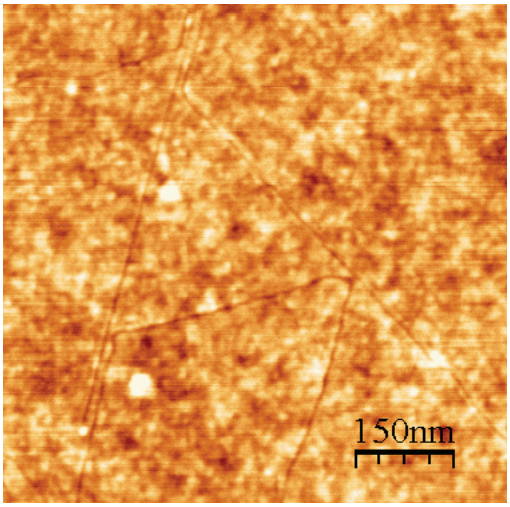

FIGURE 2: Nickel nanoparticles avoid crossing previously etched trenches, producing graphene nanostructures such as equilateral triangles and nanoribbons that should feature interesting electronic properties.

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Templated Self-assembly of Block Copolymers for Nanolithography

C. A. Ross, H. I. Smith, E. L. Thomas, V. Chuang, Y. S. Jung

Sponsorship: NSF, Singapore-MIT Alliance, SRC

Self-organized macromolecular materials can provide an alternative pathway to conventional lithography for the fabrication of devices on the nanometer scale. In particular, the self-assembly of the microdomains of diblock copolymers within lithographically-defined templates to create patterns with long range-order has attracted considerable attention, with the advantages of cost-effectiveness, large-area coverage, and compatibility with pre-established top-down patterning technologies. Block copolymers consist of two covalently bound polymer chains of chemically distinct polymer materials. The chains can self-assemble to form small-scale domains whose size and geometry depend on the molecular weights of the two types of polymer and their interaction [1]. With the purpose of fabricating arrays of magnetic nanosized dots, which are a potential candidate for magnetic hard-drive media, we are templating the block copolymers in a removable template. Previously, sphere-forming poly(styrene-b-ferrocenyldimethylsilane) (PS-PFS) diblock copolymers were successfully aligned in 2-D [2] or 3-D [3] templates. In addition, the spherical morphology of poly(styrene-b-dimethylsiloxane) (PS-PDMS) block copolymers can be templated using an array of nanoscale topographical elements that act as surrogates for the minority domains of the block copolymer, as demonstrated in Figure 1[4]. The PS-PDMS diblock copolymers have a large interaction parameter and a high etch-contrast between two blocks, which are desirable for long-range ordering and pattern-transfer into functional materials. Concentric ring patterns can also be obtained by using circular templates [5]. Beyond rather limited morphologies of diblock copolymers, an appropriate combination of block sequence, interaction parameter of the adjacent blocks, volume fraction, and molecular weights of ABC triblock polymer thin films provides a diversity of new structures. For example, core-shell structured triblock terpolymer can be obtained by designing the block sequence and volume fraction of the blocks. Figure 2a presents vertically oriented high-density nanorings from PS-PFS-P2VP polymers after the selective removal of PS and P2VP [6]. Square arrays of dots can also be achieved from a PI-PS-PFS self-assembled triblock terpolymer, as shown in Figure 2c.

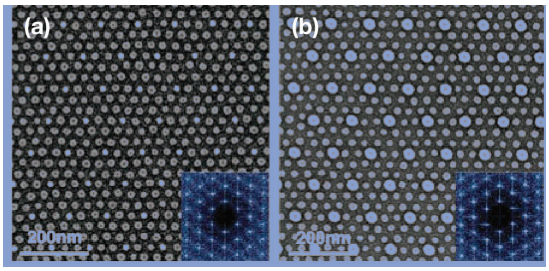

FIGURE 1: SEM images of ordered BCP spheres formed within a sparse 2D lattice of HSQ posts (brighter dots). The substrate and post surfaces were functionalized with a PDMS brush layer in (a), which corresponds to the schematic in (A), and with a PS brush layer in (b). The insets show the 2D Fourier transforms.

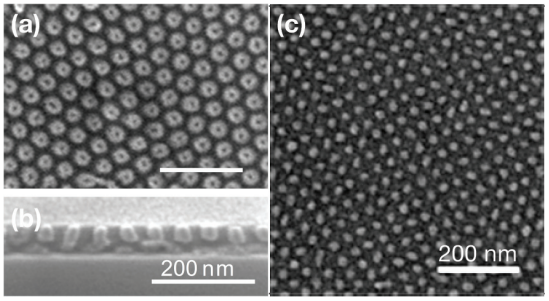

FIGURE 2: Ring arrays of PFS from a thin film of a core-shell cylindrical-morphology PS-b-PFS-b-P2VP triblock terpolymer. (a) top view (b) side view. (c) Square array of PFS dots from a thin film of PI-b-PS-b-PFS triblock terpolymer. PI and PS have been removed by O2 RIE.

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Nanofabricated Reflection and Transmission Gratings

M. Ahn, S. K. Slater, P. Mukherjee, R. K. Heilmann, M. L. Schattenburg
Sponsorship: NASA, NSF

Diffraction gratings and other periodic patterns have long been important tools in research and manufacturing. Diffraction is due to the coherent superposition of waves—a phenomena with many useful properties and applications. Waves of many types can be diffracted, including visible and ultraviolet light, x-rays, electrons, and even atom beams. Periodic patterns have many useful applications in fields such as optics and spectroscopy; filtering of beams and media; metrology; high-power lasers; optical communications; semiconductor manufacturing; and nanotechnology research in nanophotonics, nanomagnetics, and nanobiology.

A long-standing problem with transmission gratings in the extreme ultraviolet (EUV) and soft x-ray bands has been the strong absorption of photons upon transmission, and thus a low diffraction efficiency in this important wavelength band. We have recently solved this problem with the invention and fabrication of critical-angle transmission (CAT) gratings. This new design for the first time combines the high broadband efficiency of blazed grazing-incidence reflection gratings with the superior alignment and figure tolerances and the low weight of transmission gratings [1], [2]. The CAT gratings consist of ultrahigh-aspect-ratio, nm-thin freestanding grating bars with sub-nm smooth sidewalls that serve as efficient mirrors for photons incident at graze angles below the angle for total external reflection (see Figures 1 and 2). Blazing can concentrate diffracted power into a single or a few desired diffraction orders and has been confirmed through x-ray tests. Blazing also enables the use of higher diffraction orders and leads to manifold increases in spectral [3] and spatial resolution in spectrometer or focusing applications, respectively. We have achieved grating bar aspect ratios of ~ 150 in 200-nm-period CAT gratings and are currently focusing on optimizing internal support structures.

Work is also ongoing in the area of high-precision pattering of silicon-immersion echelle gratings for high-resolution (R ~ 100,000) applications in infrared telescopes for astronomy [4].

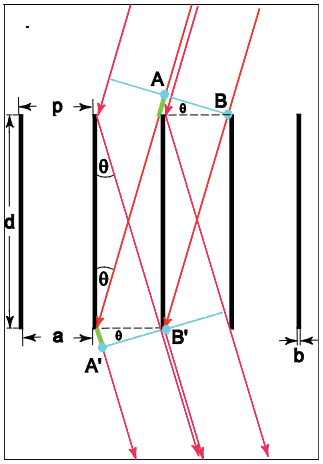

FIGURE 1: Schematic of the CAT grating principle. Diffraction peaks appear where the path length difference AA'-BB' equals an integer multiple of the wavelength.

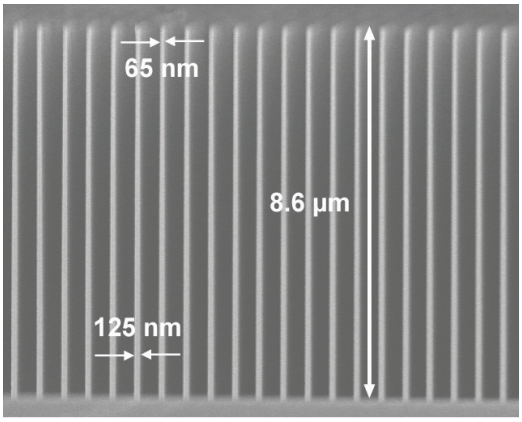

FIGURE 2: Scanning electron micrograph of a cleaved cross-section through a 574 nm-period silicon CAT grating that was (intentionally) not etched all the way through. The grating bar aspect ratio is close to 100 and is increased to ~ 150 for the final grating.

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Nanometrology

R. Heilmann, Y. Zhao, D. Trumper, M. L. Schattenburg
Sponsorship: NSF

Manufacturing of future nanodevices and systems will require accurate means to pattern, assemble, image, and measure nanostructures. Unfortunately, the current state-of-the-art of dimensional metrology, based on the laser interferometer, is grossly inadequate for these tasks. While it is true that when used in carefully-controlled conditions interferometers can be very precise, they typically have an accuracy measured in microns rather than nanometers. Achieving high accuracy requires extraordinarily tight control of the environment and thus high cost. Manufacturing at the nanoscale will require new technology for dimensional metrology that enables sub-1-nm precision and accuracy in realistic factory environments.

A recently formed MIT-UNC–Charlotte team is developing new metrology technology based on large-area grating patterns that have long-range spatial-phase coherence and ultra-high accuracy. Our goal is to reduce errors in gratings by 10-100 times over the best available today. These improved gratings can be used to replace interferometers with positional encoders to measure stage motion in new nanomanufacturing tools and to calibrate the dimensional scales of existing nanofabrication tools. This increased precision and accuracy will enable the manufacturing of nanodevices and systems that are impossible to produce today. Improved dimensional accuracy at the nano-to-picometer scale will have a large impact in many nanotechnology disciplines including semiconductor manufacturing, integrated optics, precision machine tools, and space research.

As part of this effort, we will utilize a unique and powerful tool recently developed at MIT called the Nanoruler that can rapidly pattern large gratings with a precision well beyond other methods. Another unique high-precision tool, the UNCC-MIT-built Sub-Atomic Measuring Machine (SAMM), is being brought to bear to research new ways to quantify and reduce errors in the gratings. Recent work at MIT has focused on improving the thermal controls in the Nanoruler lithography enclosure and developing an improved interferometer system to reduce errors in the stage metrology frame. At UNCC, the SAMM is undergoing extensive refurbishment and improvements designed to boost interferometer accuracy.

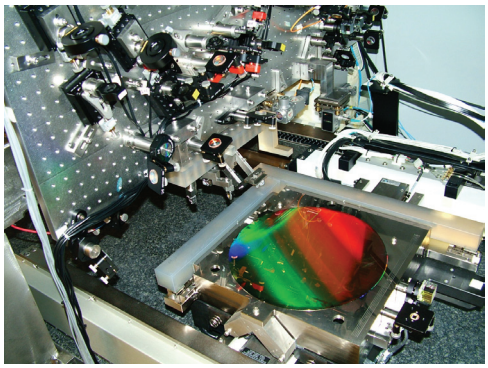

FIGURE 1: Photograph of the Nanoruler lithography and metrology system built by MIT students. This unique tool is the most precise grating patterning and metrology system in the world.

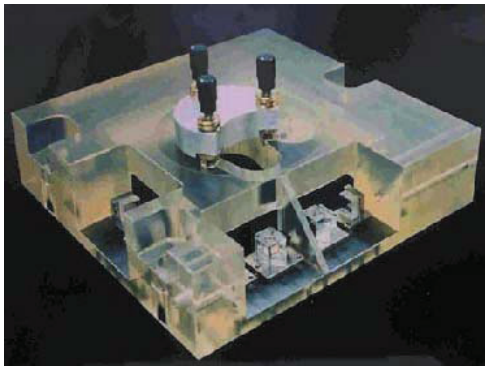

FIGURE 2: Photograph of reference block/sample holder for the Sub-Atomic Measuring Machine at the University of North Carolina – Charlotte.

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Sub-Wavelength Interference Lithography with Absorbance Modulation

T. B. O'Reilly, R. Menon, H. I. Smith
Sponsorship: Lincoln Laboratory Integrated Photonics Initiative

The minimum period of the pattern that can be produced in interference lithography is generally restricted to half the wavelength of the light being used. While shorter wavelength sources are available, the properties of short wavelength lasers are not always suitable for use in interference lithography. As a result, there is great interest in finding ways to write patterns with periods below the diffraction limit, so that very fine pitch patterns can be written with sources that are easy to work with. We are pursuing an approach to patterning below the diffraction limit by combining a dual-wavelength IL (DWIL) system and absorbance-modulation technology [1]. In absorbance-modulation optical lithography (AMOL), an absorbance-modulation layer (AML), is placed on top of the photoresist layer. The absorbance-modulation layer is a polymer film containing reversible photochromic molecules that can be switched between two isomeric states using different wavelengths of light. An example of such a material is bis(bithienylethene) (BTE) which has two forms, as shown in Figure 1. If an AML containing BTE is simultaneously exposed to standing waves in both UV and red wavelengths, as shown in Figure 2, it is possible to set up dynamic competition between the open and closed states, forming regions in the AML, with sizes much smaller than the wavelength, that are transparent to UV light. These regions effectively serve as subwavelength apertures in the AML through which the photoresist is exposed by the UV wavelength.

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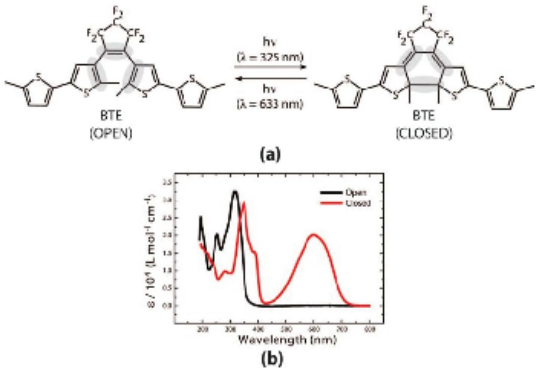

FIGURE 1: Molecular structure of the open and closed states of BTE. Exposure to UV wavelengths cause BTE to switch to the closed state, while exposure to longer wavelengths, red light for example) causes BTE to switch to the open state.

Since the states of the photochromic molecules are reversible, it is possible to shift the sets of fringes on the substrate, forming a new set of subwavelength apertures, and exposing a new set of lines in the resist. In effect, each exposure divides the spatial period of the original fringes, reducing the pitch of the final pattern. For example, if the initial spatial period were 400 nm, four exposures could be performed, shifting the fringes by 90 degrees between the exposures, to reduce the final period of the pattern to 100 nm. Ultimately, the extent to which the period can be divided will be limited by the performance of both the absorbance modulation layer and the photoresist, making a system to test and characterize AMOL materials an important tool. We are presently developing a DWIL system to be used both to test materials for use with AMOL and to provide a means of achieving sub-100nm period interference lithography with a relatively simple system and relatively long wavelengths. The planned system will form two standing waves, one using 351 nm light from an argon ion laser and a second from a longer wavelength red laser. In essence, the system consists of two independent Mach-Zehnder style IL systems, simultaneously forming standing waves of the same period that are 180 degrees out of phase with each other.

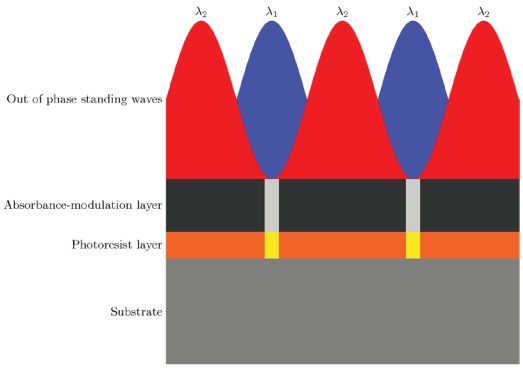

FIGURE 2: Schematic of the interaction of red and UV (shown in blue) wavelengths with an absorbance modulation layer. Out-of-phase standing waves formed by the two wavelengths result in the formation of narrow regions at the null of the red standing wave that are transparent to the UV light which serves to expose the photoresist. The AML narrows the width of the exposed regions compared to what would be possible with conventional IL exposures.

Interference Lithography

T. B. O'Reilly, H. I. Smith
Sponsorship: Lincoln Laboratory Integrated Photonics Initiative

Interference lithography (IL) is a means of rapidly writing periodic and quasi-periodic patterns , such as gratings and grids, over large areas using the coherent interference of light. The NanoStructures Laboratory has conducted research in this field for many years, developing IL systems capable of making patterns with a wide range of spatial periods, and helping to develop some of the applications of those patterns.

The lab currently operates three IL systems. Two of them, the Lloyd's mirror and Mach-Zehnder IL systems use 325 nm light from Helium-Cadmium lasers. The Lloyd's mirror IL system is a flexible and robust system that can be easily configured to write gratings with periods as small as 165 nm or as large as many microns. The ability to quickly change the period pf the pattern produced, coupled with the ease of use of this system, has made it possible for a large number of researchers to use the Lloyd's mirror system to produce patterns required for their research without having be become IL experts. Applications of these structures have included patterned magnetic media, patterned surfaces for templated self-assembly processes, and photonic crystals.

The Mach-Zehnder IL system, while less flexible than the Lloyd's mirror, produces higher quality patterns that are suitable for metrological applications. The third system, the Achromatic IL system (AIL) is a grating-based interferometer that writes 100 nm period gratings using 193 nm light from an ArF excimer laser. In addition, the NSL has close ties to the Space Nanotechnology Lab at MIT which operates the NanoRuler, which is among the most precise IL systems in the world.

We have recently developed a method to characterize photoresist performance by double-exposing a sample on an IL system; the sample is rotated slightly between the two exposures [1]. By analyzing the resulting pattern it is possible to determine how linewidth varies with exposure dose and dose modulation in fewer exposures than are required by previously described methods. The data collected from this method can be applied to models of specific IL systems to predict the variation of linewidth across the exposure area [2], which makes it possible to select IL system design and exposure parameters to improve exposure uniformity.

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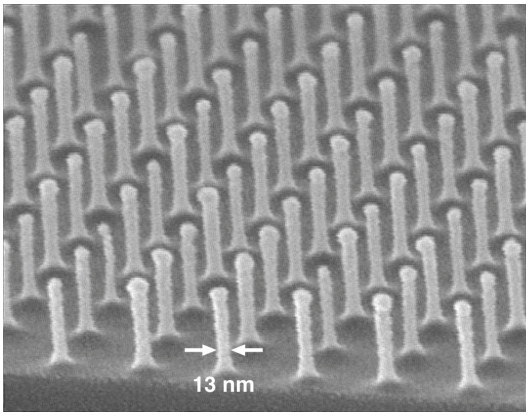

FIGURE 1: Scanning electron micrograph of a 100 nm-period grid produced with the AIL system. PMMA was exposed on top of an antireflection coating and the pattern was transferred into Si by reactive ion etching.

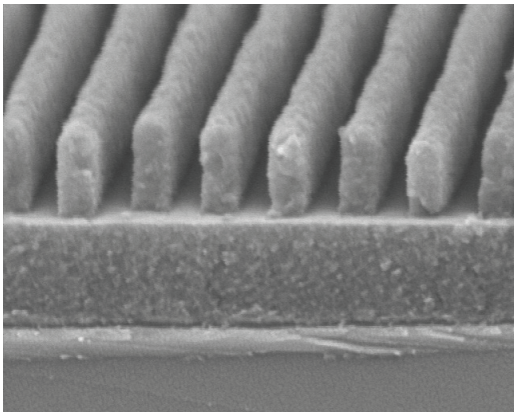

FIGURE 2: Micrograph of 165 nm period grating produced with the Lloyd's mirror. This system can be used to write patterns with periods ranging from 165 nm up to several microns.

Catalyst Engineering and Growth Mechanisms of Si and III-V Nanowires

S. T. Boles, E. A. Fitzgerald, C. V. Thompson
Sponsorship: Singapore-MIT Alliance

The vapor-liquid-solid mechanism for growth of single-crystal whiskers and wires was originally discovered in the 1960s, but it has gained new interest in the last decade as a way to fabricate high-performance nanoscale electronic devices below the limits of photolithography. Although a great deal of attention has been focused on the electronic properties of Si and III-V nanowires, many of the physical mechanisms involved in growing these single-crystal wires remain unclear. We have been investigating the importance of catalyst size and shape in growth morphology by using evaporated island catalysts, catalysts derived from dewetted thin films, and commercially available nanoparticles. Optimizing catalyst processing conditions and combining them with specific topographies or templates, such as inverted pyramid arrays or silicon dioxide gratings achieves precise control over catalyst placement and subsequent nanowire placement. This study also examines the role of growth conditions by controlling temperature, partial pressures of reactants and pre-growth annealing. These parameters have been determined to be critical not only to stable and repeatable growth of Si and III-V nanowires, but also to controlling the relative orientation and defect generation at the substrate-wire interface [1].

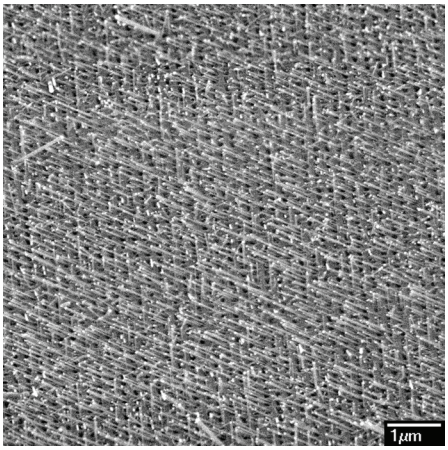

FIGURE 1: The Si nanowires grown on a Si <100> substrate with an inverted pyramid array and e-beam-evaporated Au-catalyst particles.

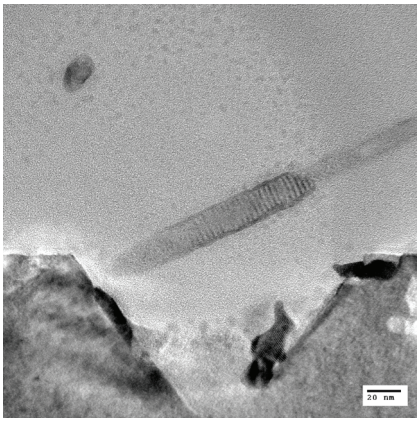

FIGURE 2: The InP/GaP core/shell nanowire heterostructures grown on a Si <100> substrate with an inverted pyramid array and e-beam- evaporated Au-catalyst particles.

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Ultra-high-density Silicon Nanowire Arrays Fabricated by Metal-assisted Etching and Block Copolymer Lithography

S.-W. Chang, V. P. Chuang, S. T. Boles, C. A. Ross, C. V. Thompson
Sponsorship: Singapore-MIT Alliance

Semiconductor nanowires have attracted considerable attention due to potential applications arising from their quasi-one-dimensional structure. In particular, silicon nanowires (SiNWs) are potential candidates for applications in nanoscale electronics, sensors, and other devices. The most commonly used method for the fabrication of SiNWs is the vapor-liquid-solid (VLS) technique, in which metal nanoparticles are used as catalysts for growth by chemical vapor deposition. One major concern for VLS-grown wires is the diffusion of catalyst metal, typically gold, into the wires at the high temperatures usually required for growth. Another challenge is getting vertical epitaxial growth on Si(100) wafers. This problem limits the integration of VLS nanowires with current CMOS technology. To circumvent these problems, an electrochemical etching method, known as metal-assisted etching (MAE), has recently received significant attention. In this approach metal catalysts are used to enhance local Si etching at the metal-silicon interface in a mixture of hydrofluoric acid and an oxidant. The process can be used to fabricate high-aspect-ratio Si structures through patterned etching of silicon wafers. For example, we have used metal-assisted etching in conjunction with block copolymer lithography and post-etching critical-point-drying to create silicon nanowire arrays with very high density and aspect ratio.

In this approach, a diblock copolymer, polystyrene (PS)-block-polyferrocenyldimethysilane (PFS) is spun onto a silicon substrate coated with an oxide layer, followed by vacuum annealing to allow for phase separation. The PFS block forms spherical microdomains surrounded by a PS matrix, which is removed by oxygen-reaction ion-etching (RIE). The PFS spheres are then used as a dry etching mask to pattern-transfer into the underlying oxide layer. Using the resulting oxide nanopillars as a metal-deposition mask, a metal catalyst antidot array is obtained after film deposition and lift-off. Finally, ordered arrays of SiNWs with good fidelity to the original block copolymer pattern are obtained by etching the silicon under the gold in a mixed solution of hydrofluoric acid and hydrogen peroxide. Post-etching drying is done in a critical-point drier to reduce capillary-force-induced clustering at wire tips. We are currently exploring application of these structures in electrochemical devices.

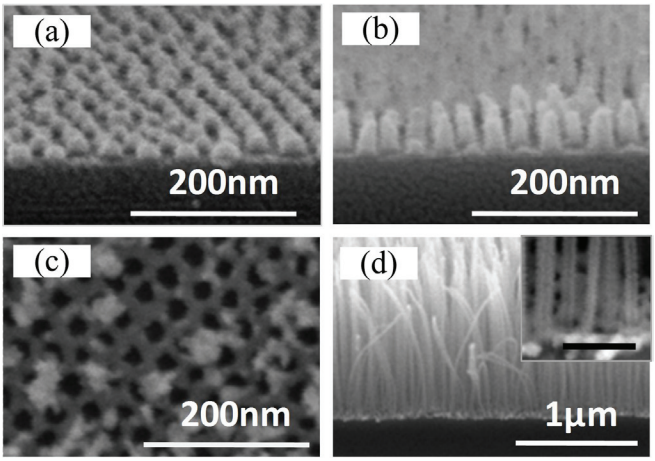

FIGURE 1: Scanning electron microscope images showing steps in SiNW fabrication: (a) *PS-b-PFS* on a silicon substrate coated with silicon oxide after PS matrix has been removed by oxygen RIE; (b) Oxide pillars after CF4 RIE; (c) Au anti-dot array after liftoff of the pillars; and (d) Silicon nanowire array after metal-assisted etching.

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Growth and Characterization of Carbon Nanotubes for Integrated Circuit Interconnects

R. R. Mitchell, G. D. Nessim, A. F. Al-Obeidi, C. V. Thompson
Sponsorship: SRC/FCRP IFC, Intel Corporation

As integrated circuit technology is developed at dimensions below 32 nm, carbon nanotubes (CNTs) represent an ideal replacement for copper interconnects as they can carry higher current densities, do not need liners, and do not suffer from electromigration. However, fabrication issues such as growing the desired type of CNTs, using CMOS-compatible processes (e.g., ideally at temperature below 400°C), and making electrical contacts and interconnections remain major technical challenges.

For electrical applications, it is important to grow CNTs on conductive substrate [1], [2]. Using appropriate catalyst/substrate metallic thin films, we have grown vertically-aligned, crystalline CNTs using thermal chemical vapor deposition at 475°C (Figure 1). Preliminary electrical measurements show ohmic contact of the CNTs with the metallic substrate. Additionally, our group hopes to decrease the processing temperature further using plasma enhanced chemical vapor deposition.

We have also grown CNTs on conductive substrates into an insulating alumina scaffold with regularly spaced pores (Figure 2). The insulating scaffold is fabricated using interference lithography and anodization of aluminum. This structure simulates an array of nanometer-scale vias filled with CNTs. In order to have CNTs with uniform height (length) and to make electrical contact with all the walls in the multi-wall tubes, we ion-milled the top after CNT growth. The electrical properties of these CNTs can be collectively characterized through deposition of a conducting overlayer on all the CNTs or individually characterized using an AFM on uncapped CNTs. We plan to characterize electrical properties as a function of CNT diameter and length and as a function of contact metallurgy.

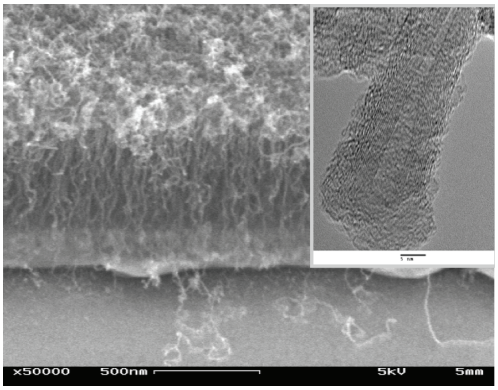

FIGURE 1: Carpet of vertically-aligned CNTs on conductive substrate grown at 475°C. The catalyst/underlayer system is Fe/Ta. The HRTEM image on the inset shows the crystalline nature of the CNTs (scale bar 5 nm).

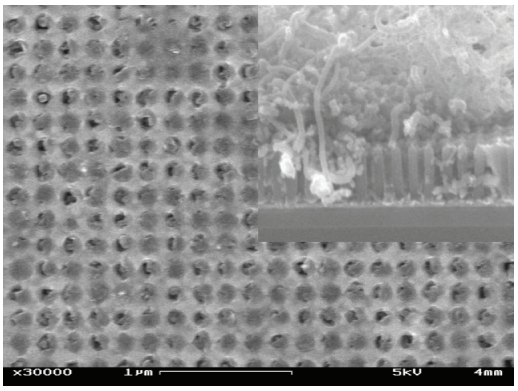

FIGURE 2: CNTs grown into alumina scaffold with pores regularly spaced. The CNTs are flush with the top surface after ion milling. The inset shows the CNTs prior to ion milling.

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Nano-particle Formation via Solid-state Dewetting

J. Ye, A. L. Giermann, D. Kim, W.-K. Choi, Y. J. Oh, H. I. Smith, C. A. Ross, C. V. Thompson
Sponsorship: Singapore-MIT Alliance

We are investigating solid-state dewetting of thin films as a technique for producing ordered arrays of metal nano-particles over large areas. Such arrays are used as catalysts for nanowire and nanotube growth and may also be of interest in memory or plasmon device applications. In order to obtain ordered dewetting with polycrystalline films, we employ physical templates. One technique is to physically constrain the area of film that dewets by pre-patterning a polycrystalline gold film on silicon dioxide. By pre-patterning a film into various geometries and observing the morphological evolution of each pattern, we found that certain geometries lead to self-ordering and alignment of the dewetted nano-particles (Figure 1). Further characterization of the effects of film thickness and pattern dimensions on self-alignment is underway.

Another technique for ordered dewetting of polycrystalline films is the use of topographic templates to modulate the curvature of as-deposited films. Topographic templates regularly modulate the curvature of as-deposited polycrystalline thin films, leading to an ordered dewetting process. Gold films dewetted on di-periodic arrays of oxidized pyramidal pits in silicon result in one-to-one self-assembly of ordered arrays of gold particles over large areas. Compared to dewetting on flat substrates, the templates impose a significant decrease in average particle size and ensure a narrow size and spatial distribution (Figure 2). In this case, this technique results in crystallographic ordering of the particles, imposing an in-plane texture and changing the out-of-plane texture [1]. We have demonstrated similar morphological and crystallographic results for gold dewetting on mono-periodic saw-tooth gratings. Similar results ordering results (but without crystallographic alignment) have been obtained for Co [2]. In addition, we have developed a combination of patterned deposition on topography and controlled dewetting, to produce ordered arrays of particle arrays with dimensions of a few ten's of nanometers [3].

In the case of a single crystalline film, the dewetted islands show regular patterns. We observe a strong dependence of the morphological evolution of single crystalline nickel thin films on the thickness of the film and on the crystallographic orientation of the film. The latter is determined by an epitaxial relationship with a magnesium oxide substrate. The resulting nano-particles remain epitaxial and thus share both in- and out-of-plane crystallographic alignment. Therefore, we believe that this work could give us an opportunity to study the effect of crystallographic orientation of catalysts on the growth of nanotubes and nanowires.

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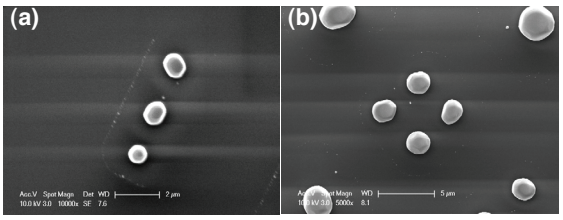

FIGURE 1: The SEM images of self-aligned Au dots through solid-state dewetting process. Solid-state dewetting process changes a rectangular Au pattern to self-aligned dots during thermal annealing. (a) Self-aligned 3 dots with single row from the pattern dimension of 3 μm x 7 μm x 30 nm. (b) Self-aligned 4 dots with double row from the pattern dimension of 9.3 μm x 9.3 μm x 120 nm. All scale bars represent 5 μm.

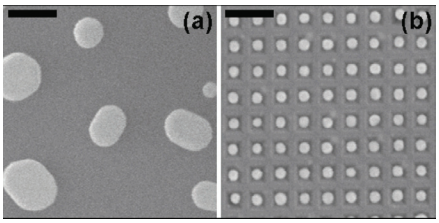

FIGURE 2: The effect of topography on particle morphology. The results of dewetting a 10-nm-thick Au film on (a) a flat substrate and (b) a topographic substrate. Micrographs are displayed at the same magnification to emphasize the effect of topography on particle size. Scale bars are 200 nm in length.

Nanostructured Resistor- and Transistor-based Gas Sensors

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Sponsorship: KIST, NSF, US-Israel Binational Science Foundation

Gas sensors play a vital role in public health and safety, industrial process control, and the reduction of toxic emissions into the environment [1]. Conductometric gas sensors based on semiconducting metal-oxide thin films are of high interest in many applications due to their high sensitivity, small size, and simplicity of measurement. Reproducibility, however, often suffers due to generally uncontrolled electronic properties of the film-substrate interface. Several approaches are being taken to overcome this limitation including the use of microsphere templating [2], or meshes of interconnected nanofibers [3]. In the case of dense films, thin-film transistor (TFT) configurations are being investigated to achieve improved control [4].

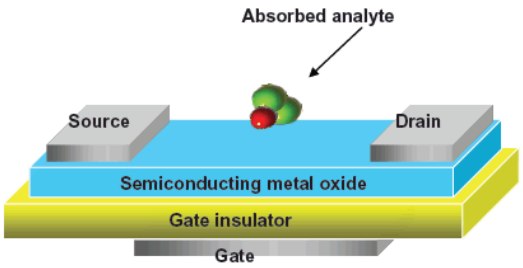

FIGURE 1: Schematic of gas sensor.

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Directional Liquid Spreading on Asymmetric Nanostructured Surfaces

K. Chu, R. Xiao, E. N. Wang

The controllability of liquid-spreading and droplet wettability on surfaces have been of significant interest for a broad range of applications, including inkjet printing, biological microfluidics, and fluidic-based thermal management devices [1-5]. In this research, we investigated the ability to manipulate the directionality of liquid-spreading by using asymmetric nanostructured surfaces. The nanostructures were composed of silicon pillars with diameters of 250 nm with one side coated with a gold film of thicknesses ranging from 250 nm to 400 nm. Due to the thermal expansion mismatch of the materials, the pillars deflected to angles ranging from 7 to 52 degrees, where the deflection angle was dependent on the thickness of the gold layer. Figure 1 shows an example of asymmetric nanopillar array with a 12-degree deflection angle. We demonstrated that such asymmetrical structures allow the advancing side (+X side) of the droplet to spread, while pinning the receding side (-X side) of the droplet, as shown in Figure 2 (a) and (b). Detailed experiments were performed to characterize the effect of material properties and nanostructure deflection angle on spreading dynamics. The surface tension of the liquid was also varied to examine the effect on spreading velocity. In sum, the directional propagation of the liquid film in the nanopillars allows control of the droplet spreading process. This work offers new opportunities to develop tunable nanostructures to control directional liquid droplet spreading and film propagation for microfluidic systems.

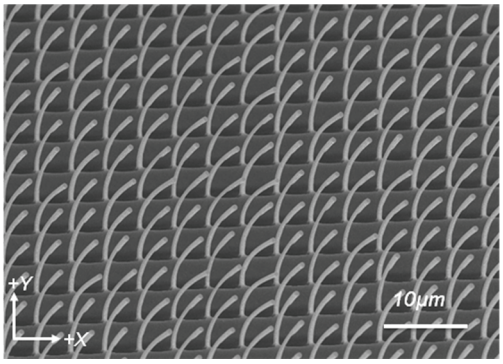

FIGURE 1: Scanning electron micrograph of a surface with uniform array of asymmetric nanopillars of 12° deflection angle. The diameter and spacing of pillars are ~500nm and 3.5μm, respectively.

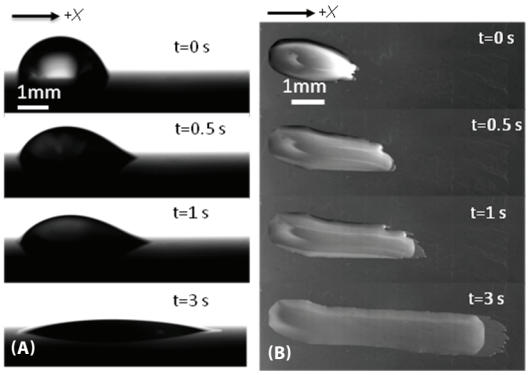

FIGURE 2: (a) Side view and (b) top view of time-lapse images of directional spreading phenomenon of a liquid droplet. The images show that the initial (t=0 s) position with the final (t=3 s) position of contact line of a liquid droplet on the -X side was pinned while the liquid spreads only in the +X direction.

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High-lux Cooling on Nanoengineered Surfaces

R. Xiao, E. N. Wang

The demand for increased performance of integrated circuits has introduced a growing demand for new thermal management solutions [1], [2]. Various thermal management schemes have been studied, among which thin-film evaporation has received recent attention due to its potential in achieving high heat dissipation rates (~1000 W/cm^2) with low thermal resistance. Traditional methods of forming thin liquid films, including jet-impingement or spray, usually consume considerable power or require significant space, which limit their applications [3], [4]. In this work, we investigated microstructures consisting of micro-pillar arrays as a new method to achieve thin-film evaporation. The microstructures have diameters ranging from 5 μm to 10 μm, separated by spacings ranging from 5 μm to 10 μm (Figure 2a). Liquid is driven by capillarity to form a thin film whose thickness is the same as the height of the pillars (Figure 1). A semi-analytical model was developed to predict the propagation rate of the liquid film and the model was validated with experiments. Heaters were fabricated on the backside of the chips with micro-fabrication technology to simulate the non-uniform heat flux on integrated chips. The temperature distribution over the chip was measured by distributed thermoresistors (Figure 2b). Experiments show that with same super-heat, the heat dissipation rates on microstructured surfaces are higher than on smooth surfaces. The heat dissipation rate is positively related to the propagation rate of the liquid film. Optimizing pillar geometries according to the model in this work achieves an optimized heat dissipation rate of several hundreds of Watts per cm^2 at local heat spots. This work provides opportunities to meet the high heat- dissipation demand for future high-performance integrated circuits.

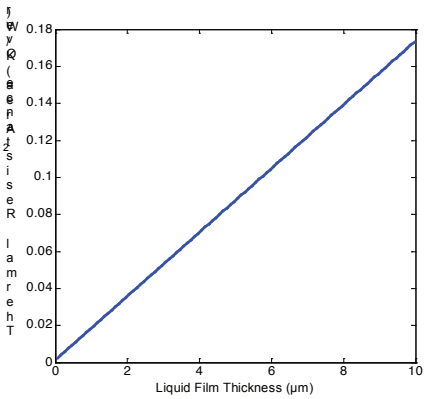

FIGURE 1: Thermal resistance of water film as a function of the film's thickness. To achieve a thermal resistance below 0.1 K/W, the film's thickness should be below 6 μm.

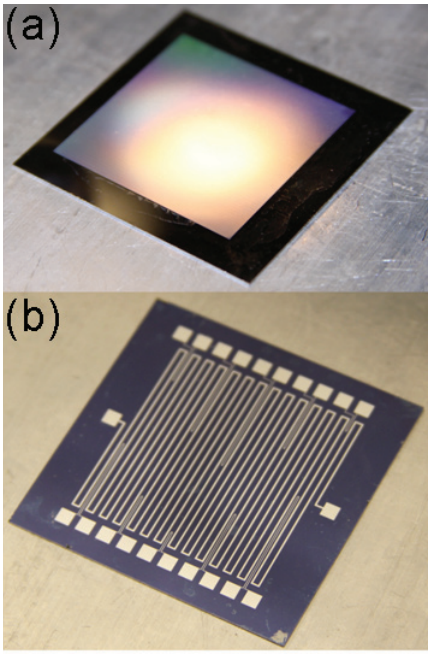

FIGURE 2: a) Image of front-side device with the micropillar array with diameters of 10 μm and spacings of 5 μm. b) Image of back-side devices with ten temperature sensors and one heater.

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Aligned CNT-based Microstructures and Nano-engineered Composite Macrostructures

B. L. Wardle, R. Guzman de Villoria, N. Yamamoto, H. Cebeci, J. Blanco, H. M. Duong, F. Fachin, S. L. Figueredo, K. Ishiguro, W. Kim, L. Megalini, S. P. Pont, S. A. Steiner III, S. Vaddiraju, S. Wicks

Sponsorship: Nano-Engineered Composite aerospace STructures (NECST) Consortium, NSF, Fulbright IS&T Fellowship

Carbon nanotube (CNT) composites are promising new materials for structural applications thanks to their mechanical and multifunctional properties. We have undertaken a significant experimentally-based program to understand both microstructures of aligned-CNT nanocomposites and nano-engineered advanced composite macrostructures hybridized with aligned CNTs.

Aligned nanocomposites are fabricated by mechanical densification and polymer wetting of aligned CNT forests [1]. Polymer wetting is driven by capillary forces that arise upon contact of the polymer with the nanostructured CNT forest [2], [3], the rate of which depends on properties of the CNT forest (e.g., volume fraction) and the polymer (viscosity, contact angle, etc.). Here the polymer is unmodified aerospace-grade epoxy. CNT forests are grown to mm-heights on 1-cm^2 Si substrates using a modified chemical vapor deposition process. Following growth, the forests are released from the substrate and can be handled and infiltrated. The volume fraction of the as-grown CNT forests is about 1%; however, the distance between the CNTs (and thus the volume fraction of the forest) can be varied by applying a compressive force along the two axes of the plane of the forest to give volume fractions of CNTs exceeding 20%.

Variable-volume fraction-aligned CNT nanocomposites were characterized using optical, scanning electron (SEM) and transmission electron (TEM) microscopy to analyze dispersion and alignment of CNTs as well as overall morphology. Physical property testing is underway.

Nano-engineered composite macrostructures hybridized with aligned CNTs are prepared by placing long (>20 μm) aligned CNTs at the interface of advanced composite plies as reinforcement in the through-thickness axis of the laminate. Three fabrication routes were developed: transplantation of CNT forests onto pre-impregnated plies [4] (the "nano-stitch" method), placement of detached CNT forests between two fabrics followed by subsequent infusion of matrix, and *in situ* growth of aligned CNTs onto the surface of ceramic fibers followed by infusion or hand-layup [5]. Aligned CNTs are observed at the composite ply interfaces and give rise to significant improvement in interlaminar strength, toughness, and electrical properties. Interestingly, toughness improvement has demonstrated a favorable nano-scale size effect [6]. Analysis of the multifunctional properties and nanoscale interactions between the constituents in both the nanocomposites and hybrid macrostructures is underway. A new route to fabricate these materials in a continuous way is being developed.

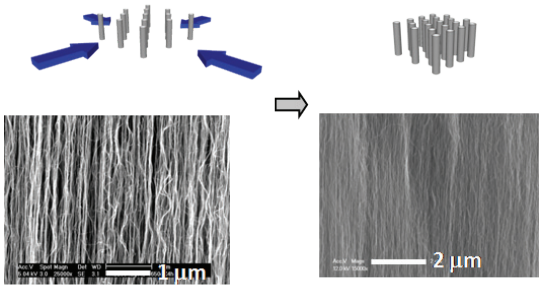

FIGURE 1: Aligned-CNT nanocomposites via biaxial mechanical densification of CNT forests.

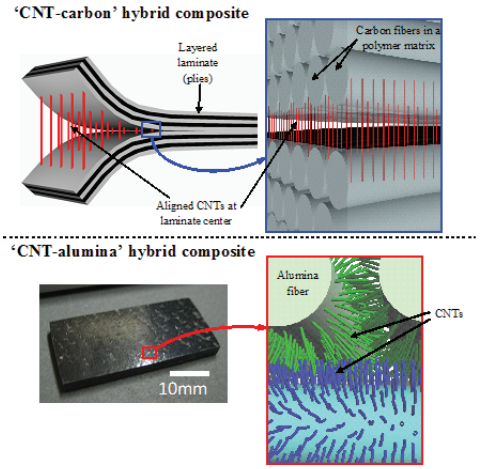

FIGURE 2: Aligned-CNT nano-engineered composite macro-scale architectures.

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