Materials

Molecules as Segmented Storage Elements in Floating Gate Memories

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Sponsorship: SRC/FCRP MSD

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Conventional flash memories may reach fundamental scaling limits [1] because of the minimum tunnel oxide thickness and poor charge retention due to defects in the tunneling oxide, necessitating new approaches to meet the scaling requirements while simultaneously meeting the reliability and performance requirements of future products. In this study we demonstrate alternative nano-segmented floating gate memories using organic molecules as programmable charge-storage and charge-retention elements in capacitive structures. These organic thin films consist of inherently well-ordered planner molecules that are on the order of 1nm in size, representing a uniform set of identical nanostructured charge-storage centers. We investigated and compared the memory behavior of a variety of molecular thin films for identifying the molecular thin-film characteristics best suited for design of floating gate memory. The initial results show device durability over 10^5 program-erase cycles, with a hysteresis window of up to 3.3 V for program/erase conditions of +8V/-8V, corresponding to the charge storage density of 5×10^{12} cm^{-2}. These results signify the potential of using molecular organic thin films as a floating gate of flash memory devices.
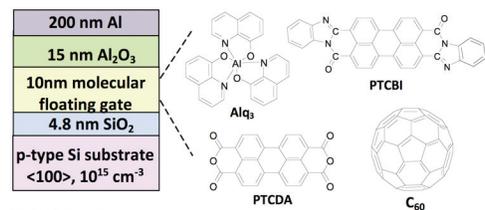

FIGURE 1: The schematic cross-section of the device structure with chemical structures of tested molecular organic thin films.
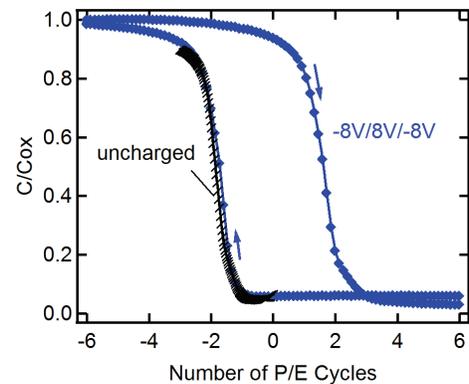

FIGURE 2: The C-*V* plot of a device with a10-nm thick PTCBI layer showing a 3.3±0.1 V hysteresis window.

In-situ Deposition of High-k Dielectrics on a III-V Compound Semiconductor

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Sponsorship: SRC/FCRP MSD

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[2]   C.W. Cheng,J. Hennessy, D. Antoniadis, E.A. Fitzgerald ,"The Discrepancy of C-V Characteristics of *In* and *Ex Situ* Atomic-layer-deposition Al_2O_3 on n- and p- GaAs with Arsine Treatment," submitted to *IEEE Electron Device Letters.*

We developed an *in-situ* manufacturable method to passivate the III-V compound semiconductor (especially the GaAs) in an MOCVD system. The trimethyaluminum (TMA) and isopropanol (IPA) were chosen as the precursors of the Atomic Layer Deposition (ALD) of Al_2O_3. The III-V channel and buffer layer were grown by the CVD mode and then the passivation Al_2O_3 was deposited by the ALD mode by applying appropriate procedures and growth parameters in an MOCVD system. This design made our CVD machine the first *in-situ* passivation CVD machine in the world, and it achieved low interfacial defect density at the oxide/III-V semiconductor. Beside the *in-situ* method, the *ex-situ* method was also investigated to compare the results with the *in-situ* method. The self-cleaning effect was also explored in the *ex-situ* process by applying TMA/IPA as ALD precursors. Both depletion- and enhanced-mode MOSFET were fabricated to evaluate the real performance of the device with *in-situ* passivation oxide.
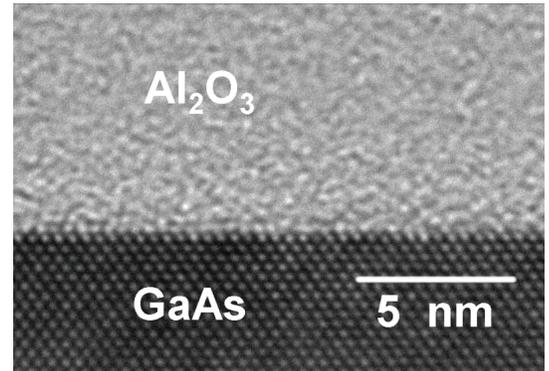

FIGURE 1: An HRTEM image of the interface between GaAs substrate and Al_2O_3 film grown at 370 °C. The TMA and IPA pulse times were both 5 s.
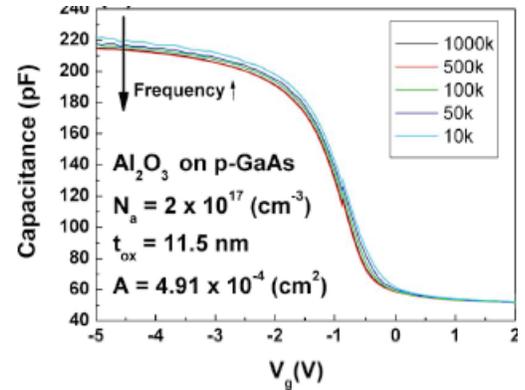

FIGURE 2: The C-V characteristics of in-situ Al_2O_3 / p-GaAs MOS capacitor measured at different frequencies from 10 kHz to 1 MHz.

A CMOS-compatible Substrate and Contact Technology for Monolithic Integration of III-V Devices with Silicon

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Sponsorship: DARPA COSMOS program

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This work explores a method of planar integration of III-V HEMTs with silicon CMOS technology, which will allow for true monolithic integration of III-V RF components with digital logic. The substrate platform and contact technology of the III-V devices are studied. Our group previously developed the substrate platform on which these devices will be built, which is shown in Figure 1 [1], [2]. It has been termed a silicon-on-lattice-engineered-silicon (SOLES) substrate. The buried germanium in this substrate provides a template for the growth of III-V materials, whereas the top silicon-on-insulator allows for the processing of traditional CMOS devices. This substrate platform offers flexible integration of III-V and Si devices [3], [4] as well as the capability to be processed in a Si fabrication facility. We are currently exploring the thermal stability of the SOLES substrate, both in terms of the mechanical stability and the diffusion or interdiffusion of the various layers. Methods to increase the thermal budget of this substrate are sought. These methods include the incorporation of additional buried layers in the substrate. Both the ease of integration of these new materials as well as the ease of subsequent device processing on the SOLES substrate are considered in the materials choices.

For true monolithic integration, both the substrate platform and device processing must be compatible with Si CMOS. Thus, we seek a device process that will eliminate or minimize exposure of the III-V materials. In addition, using only materials that are traditional to the silicon fabrication will be advantageous in allowing for simultaneous processing of both the Si and III-V devices. The III-V contact technology traditionally makes use of gold, a deep-level trap in silicon. Because the use of gold is detrimental to silicon devices and because of the simultaneous goal of process integration, we seek to create silicide contacts to GaAs through a silicon cap. Nickel silicide is currently being explored for this application due to its low thermal budget, as compared to TiSi2 and CoSi2.
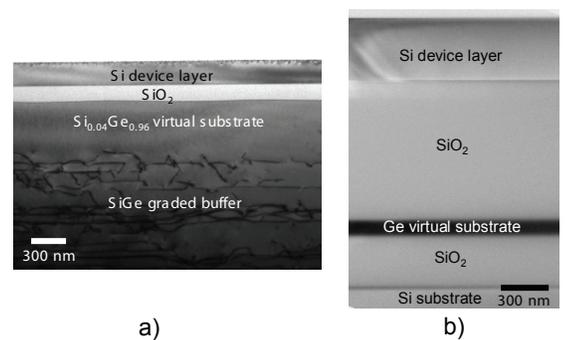

a)   b)

FIGURE 1: TEM micrographs of two variations of the SOLES structure. The buried Ge layer is incorporated into the substrate either through a) a SiGe graded buffer [1], or b) by the SmartCutTM process [2].

Selective Epitaxial Growth of Ultrathin SiGe-on-Si for CMOS Applications

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Sponsorship: DARPA

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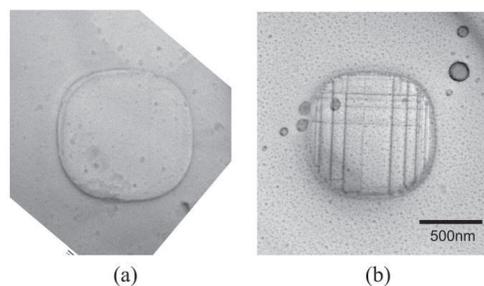
The selective epitaxial growth of ultrathin SiGe-on-Si for structures suitable for CMOS devices has been studied. Very thin $Si_{0.3}Ge_{0.7}$ (thickness less than 12nm) was grown in exposed Si regions on oxide-patterned Si wafers. The SiGe growth and misfit dislocation density were studied and analyzed as a function of film thickness and window orientation. Intensive TEM techniques were used for this study.

Strained SiGe and Ge channel PMOS have large hole mobility enhancement over traditional Si channels, and it has been shown that the hole mobility can be enhanced up to 10X relative to unstrained Si [1], [2]. Hole mobility in strained SiGe channel MOSFET is increased with increasing Ge composition. However, growing Ge or SiGe with high Ge composition on bulk Si increases the lattice mismatch in the heteroepitaxy. Increasing the Ge composition above 70% does not bring increased mobility enhancement because the channel thickness is limited due to critical thickness constraints [3]. Increasing the critical thickness for strained SiGe grown in small areas will enable thicker SiGe channels and a pathway to avoid the mobility degradation associated with ultra-thin films. In addition, this area of study is of interest for epitaxial growth in small-area SiGe source/drains as a means of increasing compressive strain in Si PMOSFETs.

Past studies showed that growing low-Ge-content (<30%) SiGe in small areas (~10 x 10 um) increases the critical thickness [4]. In this study, we have grown $Si_{0.3}Ge_{0.7}$ on exposed Si regions on oxide-patterned Si wafers, with pattern size spanning sub-microns to a few tens of microns. With this limited area growth, the critical thickness of $Si_{0.3}Ge_{0.7}$ was ~8nm, which is a 3X increase from the equilibrium thickness of 2.5nm (Figure 1). The misfit dislocation for SEG growth is strongly influenced by the processing conditions such as prebake temperature, as well as the shape of the growth area. Figure 2 shows 10-nm-thick $Si_{0.3}Ge_{0.7}$ film, one grown in <110> square oxide opening, the other in 45°rotated feature. Dislocation density is much higher in Figure 2(b), and further study is in progress to understand the effect of window shape on the misfit dislocation density.

(a)   (b)

FIGURE 1: Plan-view TEM images of $Si_{0.3}Ge_{0.7}$ films illustrating the critical thickness in small areas. The field region is SiO_2. (a) No misfit dislocation is detected for a 6-nm-thick film. (b) For an11-nm film, dislocations are clearly visible. Scale bar applies to both (a) and (b).
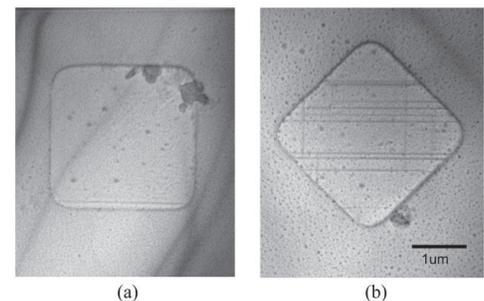

(a)   (b)

FIGURE 2: Plan-view TEM mages of $Si_{0.3}Ge_{0.7}$ that was grown (a) in <110> square oxide opening, and (b) in 45° rotated feature, which shows higher dislocation density. Both SiGe films are ~10nm thick.

Graphene by Ambient-pressure CVD

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Sponsorship: NSF CAREER (DMR-0845358), Intel Higher Education Program, SRC/FCRP MSD, Lincoln Lab Advanced Concept Committee.

We present an approach to grow graphene films consisting of 1 to 10 graphene layers in ambient pressure on thin metal films [1]. The graphene so produced is transferable to non-specific substrates. The growth of graphene occurs by segregation of carbon from the bulk of the metal film. Such segregation takes place in a CVD process in which the metal thin film is cooled down as it is being doped by carbon from a hydrocarbon source. We find that such graphene precipitation can be controlled in ambient pressure conditions in order to obtain coverage of up to 87% of no more than 2 graphene layers.

The size of such films is limited only by the size of the catalytic metal film. Here, we demonstrate sizes of around 1in². Transferring of single- and multi-layer graphene to other substrates enables their characterization in isolation from its growth surface. The ambipolar transfer characteristics of the graphene synthesized is demonstrated and electron and holes mobilities of 200-2200 cm²/Vs were measured. The graphene films also show optical transmittance of 90% in the wavelength range of 400-1000 nm and average sheet resistances of 1 kΩ/sq.

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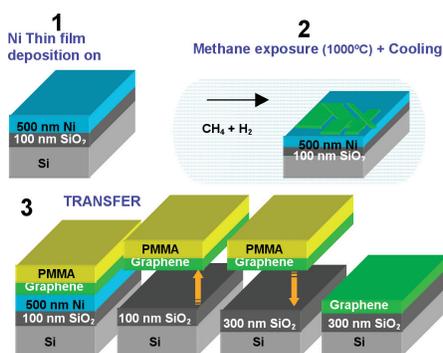
FIGURE 1: Graphene growth and transfer process. 1. Thin films of Ni are deposited on SiO₂/Si by ebeam evaporation and sputtering. 2. The films are annealed and exposed to methane at 1000˚C. Carbon decomposed on the surface of Ni diffuses into the bulk of the Ni film. During cooling, graphene precipitation is generated by carbon segregation from the bulk of the film. 3. Transferring of the graphene film synthesized is enabled by wet etching of the Ni film. A PMMA layer is used as support.
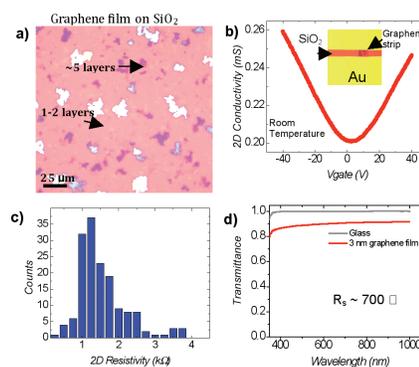

FIGURE 2: a) Optical image of a graphene film transferred to a SiO₂/Si substrate. Most of the area (shown in pink) is covered by no more than 2 graphene layers. Recognition of the number of layers is done by measuring the optical contrast created by the film, which depends on the number of layers. b) Electron transport of a graphene strip on SiO₂/Si and modulated by a back gate. c) 2D resistivities measured by several device geometries such as that shown in the inset of b). d) Optical transmittance of a graphene film fabricated by this method showing a transmittance close to 90% over the wavelength range of 400-1000 nm.

Fabrication of Large-area Graphene-based Electronic Devices

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Sponsorship: ISN, SRC/FCRP IFC

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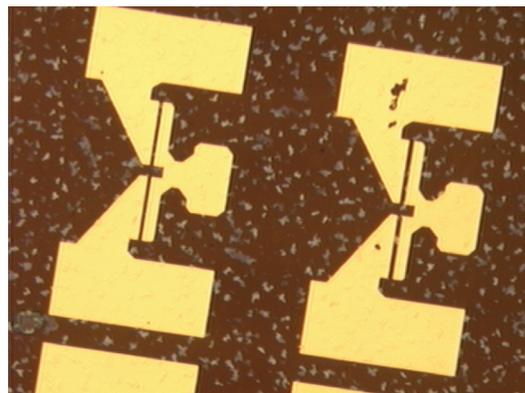
Since the discovery of graphene in 2004 [1], there has been a tremendous amount of interest in this material for its unique electronic properties. Graphene is a stable two-dimensional material composed of a monolayer of carbon atoms with extremely high electron mobility up to 200,000 cm^2/Vs [2]. Therefore, in nanostructured devices, electrons may undergo ballistic rather than ohmic transport. Additionally, graphene is a zero-band-gap semiconductor with the conduction and valence bands meeting at the Dirac point. However, there has been much interest in using 1-D graphene nanoribbons (GNR) as a method for inducing a band gap at the Dirac point [3]. These exciting properties coupled with the benefits of already mature planar processing technology have fueled the excitement about graphene-based electronics.

Initially, most measurements have been done on isolated graphene flakes through mechanical exfoliation or "the scotch tape method." However, recent developments using chemical vapor deposition (CVD) have demonstrated growth of large areas of single-layer graphene and transfer to arbitrary substrates. [4]. Other work on producing large-area devices has focused mainly on growth of graphene on fixed SiC substrates [5]. Although these growth methods have shown promising results, currently, the best device performances reported have been measured on suspended exfoliated graphene.

Our work focuses on improving the material quality and device processing technology of CVD graphene devices. Work in progress includes utilizing high-k dielectric substrates and self-aligned transistor structures to maximize the frequency performance of graphene transistors and exploring nanoribbon graphene devices fabricated through conventional dry etching and patterned-growth modalities. This project also aims to explore future electronic and optoelectronic applications of graphene devices beyond transistors. We have, for example, recently demonstrated the use of graphene's ambipolar transport for high efficiency frequency doubling [6].

FIGURE 1: Patterned Ohmic Contacts of graphene transferred onto hafnium oxide substrate.
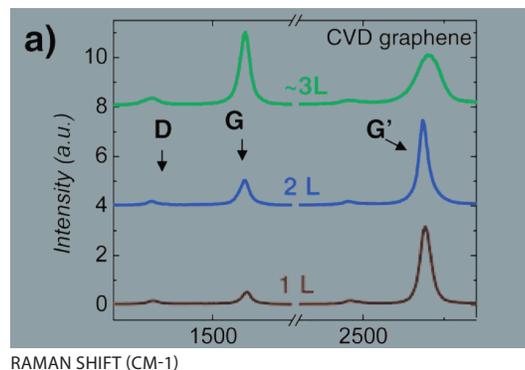

RAMAN SHIFT (CM-1)

FIGURE 2: Raman spectra for CVD graphene on SiO$_2$ substrates. The strength of the D band represents defect levels. The ratio of the G' to G provides a rough metric to qualify the number of monolayers of grapheme [6].

Magnetic Oxides for Optical Isolators and Magnetoelectronic Devices

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Sponsorship: Lincoln Laboratory, ISN, NSF

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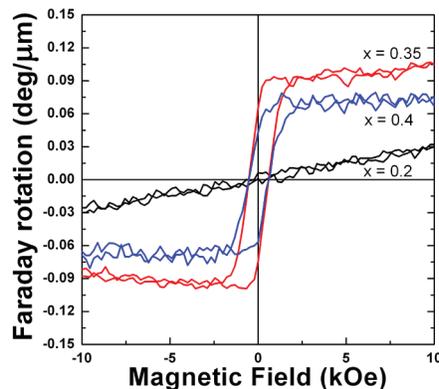
We have established a thin-film laboratory that includes a pulsed-laser deposition (PLD) system and an ultra-high vacuum sputter/analysis system. In PLD, a high-energy excimer laser is used to ablate a target, releasing a plume of material that deposits on a substrate to form a thin film. The PLD is particularly useful for making complex materials such as oxides because it can preserve the stoichiometry of the target material.

We have been using PLD to deposit a variety of oxide films for magneto-optical devices such as isolators. These materials include iron oxide, which can adopt one of four different ferrimagnetic or antiferromagnetic structures depending on deposition conditions, and bismuth iron garnet (BIG, Bi$_3$Fe$_5$O$_{12}$), which is useful for magneto-optical isolators in conventional photonic devices. The ideal material for an isolator combines high Faraday rotation with high optical transparency. Garnets have excellent properties but do not grow well on silicon substrates, making it difficult to integrate these materials. In contrast, iron oxide (maghemite) grows very well on MgO or Si, with high Faraday rotation, but its optical absorption is high. One way to solve this problem is to develop new magneto-optical active materials, which can grow epitaxially on Si by using buffer layers. Through doping with transitional metal ions, these materials can exhibit strong Faraday rotation as well as low optical loss. Recently, we have examined Fe and Co-doped SrTiO$_3$ thin film (Figure 1) [1], which shows strong magneto-optical properties and lower optical absorption compared with iron oxide. The best figure of merits of 1.1 deg/dB and 0.57 deg/dB, which are defined as Faraday rotation divided by optical absorption loss at 1550-nm wavelength, have been achieved in Sr(Ti$_{0.6}$Fe$_{0.4}$)O$_3$ and Sr(Ti$_{0.7}$Co$_{0.3}$)O$_3$, respectively. These films could be useful for waveguide isolators and other magnetoelectronic devices in which optical absorption losses are critical. Additionally, As$_2$S$_3$/Sr(Ti$_{0.6}$Fe$_{0.4}$)O$_3$ strip-loaded waveguides were fabricated on epitaxial Sr(Ti$_{0.6}$Fe$_{0.4}$)O$_3$ on LSAT (001) substrates (Figure 2) [2]. Optical transmission measurements at 1550-nm wavelength confirmed the relatively high transparency of the magneto-optical film. A second project involves the use of electrochemical methods to control the magnetization of iron oxide spinel structure films (magnetite or maghemite) grown on conducting substrates, making a chemically-switchable material. The insertion of Li ions by electrochemical discharge changes the oxidation state of the Fe(III) to Fe(II) and can reduce the magnetization of the film by about 30%, in a reversible process. Recent experiments on nanoparticles of iron oxide show much greater changes in magnetization, up to ~80%, indicating that the process is kinetically limited. Lithiation of CrO$_2$ also successfully changed the magnetization with an initial change of $10\mu_B$ per Li$^+$ ion insertion.

FIGURE 1: Faraday rotation at 1550-nm wavelength vs. applied field for Sr(Ti$_{1-x}$Fe$_x$)O$_3$ films grown on LaAlO$_3$ (001) substrates.
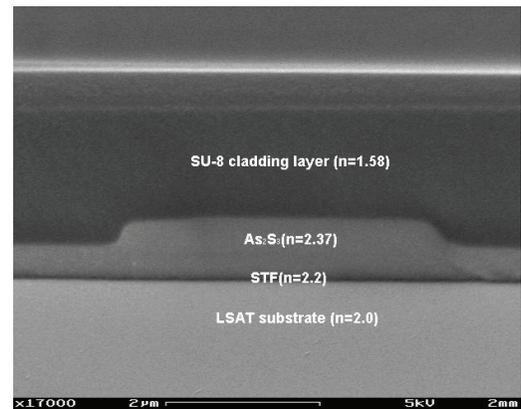

FIGURE 2: Cross-sectional SEM image of an As$_2$S$_3$/Sr(Ti$_{0.6}$Fe$_{0.4}$)O$_3$ strip-loaded waveguide with an SU-8 top-cladding layer fabricated on an LSAT(001) substrate.

Scanning Beam Interference Lithography

M. Ahn, C.-H. Chang, R. Heilmann, Y. Zhao, M.L. Schattenburg
Sponsorship: NASA

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Traditional methods of fabricating gratings, such as diamond tip ruling, electron- and laser-beam scanning, or holography, are generally very slow and expensive and result in gratings with poor control of phase and period. More complex periodic patterns, such as gratings with chirped or curved lines, or 2D and 3D photonic patterns, are even more difficult to pattern. This research program seeks to develop advanced interference lithography tools and techniques to enable the rapid patterning of general periodic patterns with much lower cost and higher fidelity than current technology.
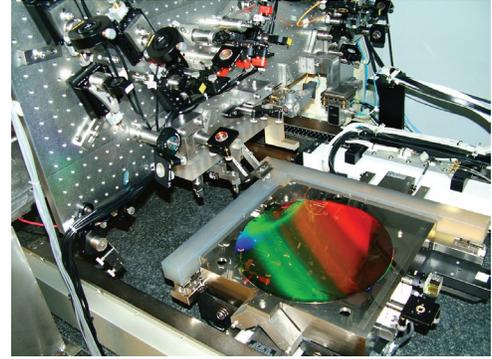
Interference lithography (IL) is a maskless lithography technique based on the interference of coherent beams. Interfering beams from an ultra-violet laser generates interference fringes, which are captured in a photo-sensitive polymer resist. Much of the technology used in modern IL practice is borrowed from technology used to fabricate computer chips. Traditional IL methods result in gratings with large phase and period errors. We are developing new technology based on interference of phase-locked scanning beams, called scanning beam interference lithography (SBIL). The SBIL technique has been realized in a tool called the MIT Nanoruler, which recently won an R&D 100 award (Figure 1). Large gratings can be patterned in a matter of minutes with a grating-phase precision of only a few nanometers and a period error in the ppb range.

Current research efforts seek to generalize the SBIL concept to pattern more complex periodic patterns, such as variable period (chirped) gratings, 2D metrology grids, and photonic patterns [1]. Important applications of large, high-fidelity gratings are for high-resolution x-ray spectroscopes on NASA x-ray astronomy missions, high energy laser pulse compression optics, and length metrology standards. We have recently developed a new grating patterning technique called aligned multiple overlay SBIL, which uses multiple (up to four) precisely overlaid IL images to divide the fundamental grating pattern down to very short periods, in this case 50-nm pitch, over large areas (Figure 2). This type of pattern has many applications including nanomagnetics, semiconductor, and nanobio manufacturing.
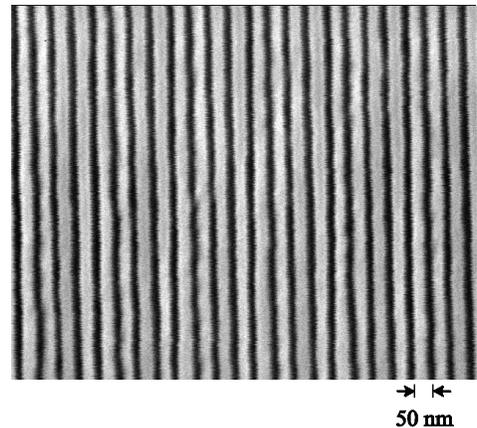

FIGURE 1: Photograph of the Nanoruler lithography and metrology system built by MIT students. This unique tool is the most precise grating patterning and metrology system in the world.

50 nm

FIGURE 2: A 50-nm pitch (25-nm line/space) grating pattern fabricated by 4X overlaid interference lithography.

Spatial-phase-locked Electron-beam Lithography

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Sponsorship: NSF

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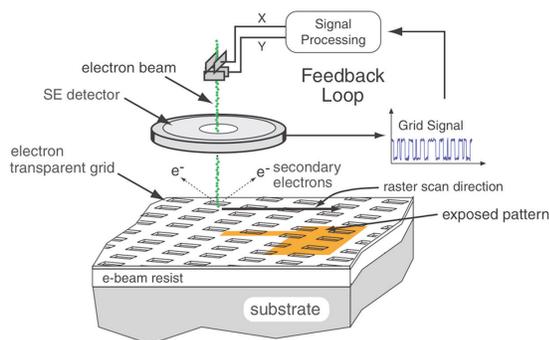
Our research in spatial-phase-locked electron-beam lithography (SPLEBL) is conducted in collaboration with the University of Kentucky. It is aimed at reducing pattern-placement errors in scanning electron-beam-lithography systems to the sub-1 nm level. Such high precision is essential for certain applications in photonics and nanoscale science and engineering. SPLEBL is currently the only approach capable of achieving such pattern-placement accuracy. As shown in Figure 1, SPLEBL uses a periodic signal, derived from the interaction of the scanning e-beam with a fiducial grid placed directly on the substrate, to continuously track the position of the beam while patterns are being written. Any deviation of the beam from its intended location on the substrate is sensed, and corrections are fed back to the beam-control electronics to cancel beam-position errors. In this manner, the locations of patterns are directly registered to the fiducial grid on the substrate. The research effort at MIT is now focused on developing the materials and processes for producing the fiducial grid, with the objectives of: maximizing the signal-to-noise of the secondary-electron signal derived from the grid; minimizing electron scattering from the grid, which would be deleterious to precision lithography; maximizing the area and absolute accuracy of the grid; and minimizing the cost and inconvenience of producing the grid on substrates of interest.

The current approach derives the modulation of the secondary-electron signal purely from the topography of the grid. The fabrication is exceedingly simple: the electron beam resist is covered with a grid in a G-line resist, and a few-nanometer coating of metal. Since most e-beam resists are not sensitive in the visible and near-UV, and since most e-beam resists are dissolved in different solvents than are G-line resists, we are able to use the two resists independently. We expose the G-line resist to interference lithography (using a Mach-Zender interferometer or coherent-diffraction lithography) and develop it to form the fiducial pattern. We then uniformly coat the grid with a metal such as Al, providing an enhancement of secondary-electron yield at the vertical sidewalls. When an electron beam scans across such a pattern there are spikes in the secondary electron emission from the sides of the vertical walls, due to enhanced electron escape probability along the sidewalls, as illustrated in the data in Figure 2. The metal and photoresist are stripped before the e-beam resist is developed. Further research will include selection of the grid thickness, metal thickness, and metal type to optimize the signal-to-noise ratio. In addition, if there is incompatibility of solvents between the G-line resist and the e-beam resist we can add a thin film of water-soluble poly-vinyl alcohol between the electron-beam resist and the G-line resist. Finally, the shape of the grid sidewalls can be tailored to optimize the secondary-electron signal in the fundamental grid frequency, and minimize the higher spatial frequency lobes observed in Figure 2.

FIGURE 1: Schematic of the global-fiducial-grid mode of spatial-phase-locked electron-beam lithography. The periodic signal detected from the fiducial grid, which includes both X and Y components, is used to measure placement error, and a correction signal is fed back to the beam-deflection system.
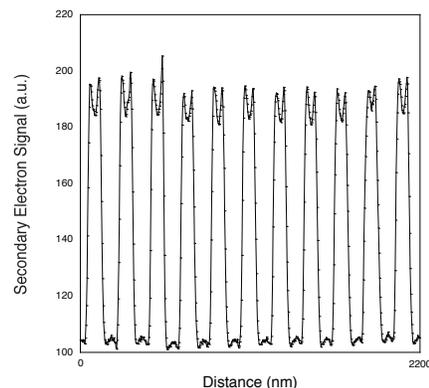

FIGURE 2: Plot of the secondary-electron yield in a fiducial pattern composed of PFI-88 photoresist covered with 3 nm of Au/Pd, averaged along one direction.

Fabrication of Free-standing Silicon-Nitride Zoneplates for Neutral-helium Microscopy using Segmented-grid-spatial-phase-locked Electron-beam Lithography

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Sponsorship: Bergen Research Foundation

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Neutral-helium microscopy is a relatively new technique that employs a focussed supersonic-expansion helium beam (~50meV) to image a sample in scanning mode. It potentially offers significant advantages. Firstly, the atoms are neutral, which means that insulating surfaces can be imaged without prior coating. Furthermore, the energy of the beam (a few tens of meV for a wavelength of about 1 Å) is very low, a factor of 1000 less than electrons for a similar wavelength. This means that fragile samples can be investigated without any damage. Helium atoms can be focussed in a number of ways, but Fresnel zoneplates have achieved the smallest beam focus so far (1μm). The first transmission-mode images created using this technique was published early 2008 [1].

In order to further improve the technique, we have developed a new fabrication process for free-standing Fresnel zoneplates to be used as focusing elements in a scaled-down and stabilised setup designed to improve resolution to about 300 nm (full width half maximum) and create the first reflection mode images. The quality of the images obtained using this technique will strongly depend on the diffraction efficiency of the fabricated zoneplates, which is determined by how closely the zoneplate resembles the ideal. Scanning electron-beam lithography (we used the RAITH 150 system available at RLE's SEBL facility) provides the necessary resolution, but pattern fidelity is limited by intra- and inter-writefield distortion. We have developed a fabrication process for the free-standing zoneplates and are currently working on minimizing both mentioned distortion errors using interference lithography gratings as a reference (see Figures 1 and 2) [2].
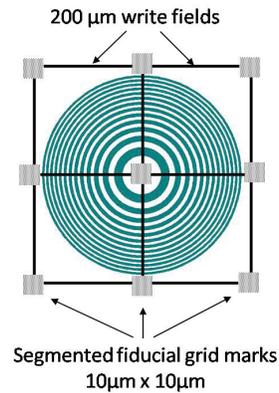

FIGURE 1: Schematic of spatial-phase locking approach for a zoneplate pattern using a segmented fiducial grid. The marks at the corner of the 200-μm writefields are dot-grids with a period of 200 nm, which were created by segmenting a Mach-Zehnder interference-lithography grid. They are used to align the writefield to the substrate as well as relative to each other, by scanning the write-field at the corners which are not relevant to the zoneplate pattern. The result will be a zoneplate with higher diffraction efficiencies.
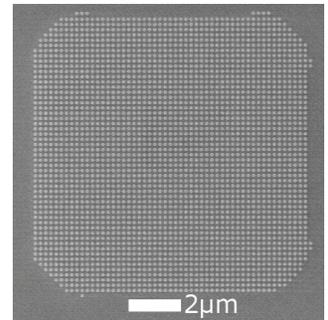

FIGURE 2: SEM micrograph of the segmented-grid alignment-mark. The titanium-gold dots are arranged in a 200-nm grid, where the two grid-axes subtend an angle of 90° to an accuracy of better than 1 arc minute. The segmentation was achieved using standard contact-ultraviolet-lithography. The spatial phase of these marks is measured for each write field by two orthogonal line scans and the writefield alignment is updated based on that spatial phase at three writefield corners.

Design and Fabrication of Sampled Bragg Gratings in SOI

J. Sun, C. W. Holzwarth, H. I. Smith
Sponsorship: DARPA

Waveguide Bragg gratings are used in optical communication systems for many applications. However, in order to achieve more advanced grating properties, such as phase shift and chirp, Scanning-Electron-Beam-Lithography (SEBL) with special precision-control techniques (e.g. Spatial-Phase-Locked EBL) represents one approach. We propose a novel sampled-Bragg grating (SBG) structure to realize various grating responses using optical lithography only. In this scheme, interference lithography is used to fabricate the background grating with excellent coherence, and then the background grating is amplitude-modulated to achieve various grating responses. In SBG, various grating responses are realized by reallocating the sampling positions and by varying the duty cycle of each sampling. For example, the phase shift grating is achieved by phase shifting the sampling instead of the grating itself. Figure 1(a) shows the simulated transmission spectrum of a phase shift grating using SBG, where the desired filter response appears in the -1st channel. Similarly, the chirp grating is achieved by chirping the sampling period, as shown in Figure 1(b).
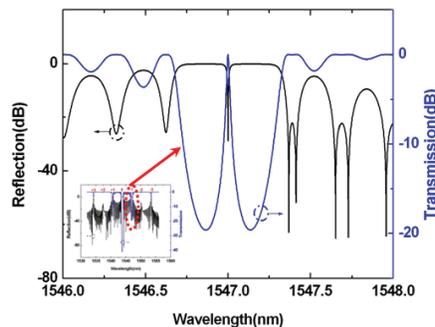
The sampling period is usually of the order of ~10mm, which is much larger than the grating period and enables to use optical-contact lithography. A processing flow for SBG fabrication was developed. A thin layer of SiO_2 was first evaporated on top of an SOI wafer. The background grating was formed on this layer through interference lithography. This SiO2 grating layer will serve as a hard mask to etch grating into silicon later. Then the sampling pattern was transferred onto the grating layer by optical-contact lithography and etching away excess background grating. After this, a second contact lithography was performed to pattern the waveguides and HBr etching was used to transfer the waveguide pattern into silicon to form a ridge waveguide. Finally, the grating pattern was etched into the top of the silicon ridge waveguide to a certain depth to form the SBG. Figure 2(a) shows the micrograph of a fabricated SBG, and Figure 2(b) shows the cross-sectional view of the SBG under Scanning-Electron-Microscope.

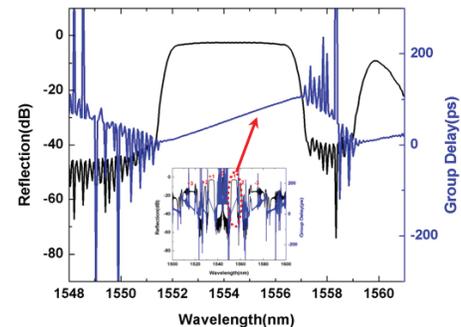**FIGURE 1(A):** Simulated response of a phase-shift grating using SBG.

FIGURE 1(B) Simulated response of a chirp grating using SBG

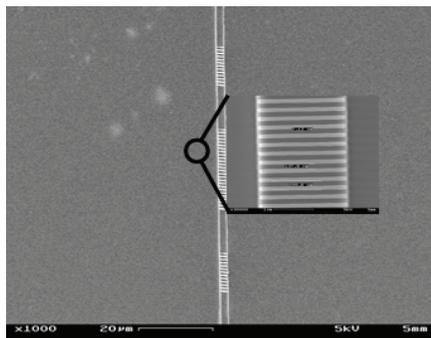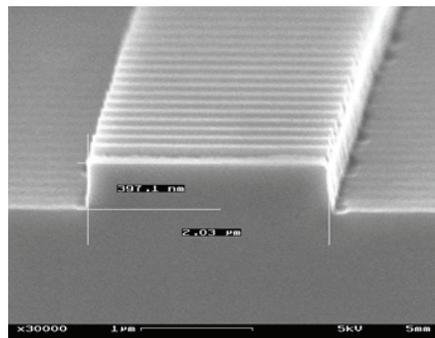
FIGURE 2(A): SEM of a fabricated SBG

FIGURE 2(B): Cross-sectional view of the SBG

Anodic Aluminum Oxide Scaffolds for IC Interconnect and Energy-storage Applications

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Sponsorship: NSF

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Metallic nanowires and nanotubes are promising candidates for advanced electrode arrays for sensor arrays and energy storage applications such as micro-batteries [1], [2]. To integrate synthesized nanowires into the devices, it is desirable to fabricate them with controlled size and location on the device-applicable substrates.. As a strategy, we are developing templated self-assembly methods that combine top-down (lithography) and bottom-up (self-assembly) approaches for fabricating and assembling various metallic nanowires and nanotubes for sensor and energy-storage applications [3].

Ordered porous alumina (OPA) is a nano-structured material that self-orders with domains and has been widely used as a template for growth of metallic nanowires and nanotubes [3]. However, the nanowires grown in the OPA are electrically blocked from the substrate due to a thin insulating barrier oxide at the base of the pores. While it is desirable to remove the thin barrier oxide, this removal is normally done using chemical etching, a barrier-thinning technique, or a reverse-bias technique [4]. These methods lead to pore widening and are difficult to implement for OPA on substrates, with difficulties increasing for small-diameter pores and pores with small spacings.

A new method for perforation of the OPA barrier layer has been developed, based on anodization of Al/W multilayer films on substrates [5]. When Al/W multilayer films are anodized and pores approach the Al/W interface, tungsten oxide forms and penetrates the alumina barrier oxide. After selective etching of the tungsten oxide, the base of the pores opened, without etching of the OPA (Figure 1). With this technique, we have demonstrated that it is possible to perforate OPA barrier layers for porous structures with small-diameter pores at small spacings and fabricated free-standing metallic nanowires, such as Ni, Au, and Pt, and carbon nanotubes on metallic layers on Si substrates (Figure 2) by selectively removing the OPA template. Using these NWs and NTs with or without the AAO as a platform, we are testing electronic characteristics for future IC interconnects and developing a micro-battery.
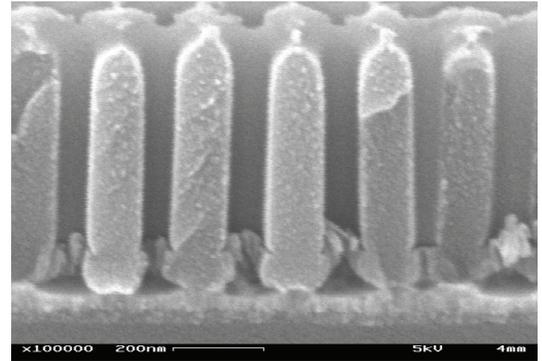

FIGURE 1: Cross-sectional SEM image of ordered porous alumina (OPA) after removal of thin barrier oxide.
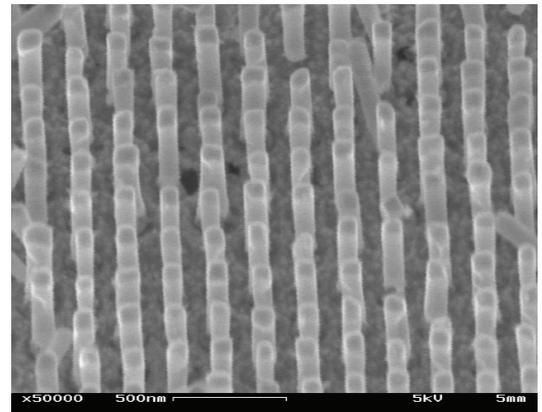

FIGURE 2: An SEM image of free-standing Ni nanowires on a conducting layer on Si substrates.