Electronic Devices

Si Current-limiters based on Si Pillar Ungated FET for Field-emission Applications

Y. Niu, L. F. Velasquez-Garcia, A. I. Akinwande
Sponsorship: DARPA

We used vertical silicon ungated field-effect transistors (FETs) as current limiters to individually ballast field-emitter arrays of density. The device structure, shown in Figure 1, consists of silicon or carbon nanofiber (CNF) emission tips that are individually connected in series with high-aspect-ratio silicon pillars (1μm x 1μm x 100μm). The device structure provides a simple solution to three problems that have plagued field emission arrays: emission current uniformity, emission current stability, and reliability.

The ungated FETs are designed as high-aspect-ratio silicon pillars to achieve velocity saturation of carriers and obtain current source-like characteristics. The Si pillar ungated FETs are connected in series with field emitter tips to limit current in each field emitter in spite of tip radii variation/distribution. To provide rigorous characterization of the ungated FET behavior, we made a test structure that exposed selected numbers of columns. Also to achieve optimal dynamic output resistance of a current limiter, silicon pillar ungated FETs were fabricated on n-type substrates with 150-200 Ω-cm, 20-40 Ω-cm and 4-6 Ω-cm resistivity. Figure 2 is an example of current-voltage characteristics obtained on silicon pillar ungated FETs fabricated on a 20-40 cm resistivity. Process and device simulations were also conducted to solidify our experimental results.

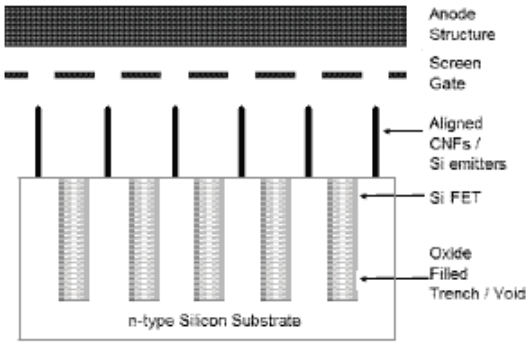

FIGURE 1: Device structure FEAs are formed on top of Si columns (FETs). Each column holds one emitter. The drain of the FET is connected to the emitter of the FE, i.e., node floating. Voltage is distributed between FEA and FET.

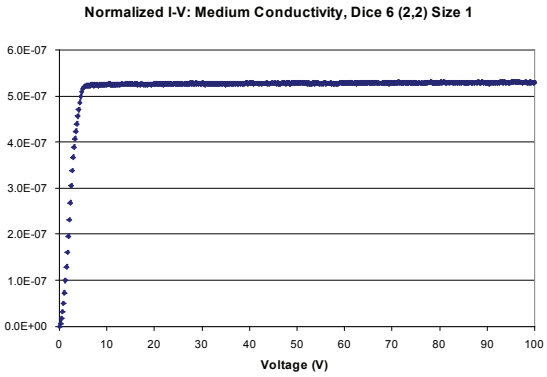

FIGURE 2: The FET characterization data show current saturation is achieved. The columns have dopant concentrations of 1x1015 cm-3, 2x1014 cm-3, and 2x1013 cm-3.

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Semiconductor and Insulator Engineering for the Improvement of Organic Thin-Film Transistors

M. A. Smith, A. I. Akinwande
Sponsorship: GEM Ph.D. Engineering Fellowship, Office of the Dean for Graduate Students

The potential uses for electronic solid state devices are endless. As organic semiconductor-based devices can easily be scaled to large areas and fabricated on mechanically compliant and non-planar surfaces at low temperatures, they can lead to a more profound realization of the possibilities that solid state technologies offer [1].

To realize organic semiconductor-based devices as a pervasive complement to Si CMOS devices, the electrical performance of organic semiconductor devices must be improved. In particular, the operating voltage must reduce while the current and the on-current to off-current ratio increase. The device of interest is a pentacene-based organic thin-film transistor (OTFT). Delocalized ð-bonded electrons enable semiconducting behavior in pentacene [1]. To make useful circuits, key device parameters such as threshold voltage, subthreshold slope, and on-current to off-current ratio have to be reproducible. Ultimately, these device parameters are related to pentacene thin-film quality (grain size, growth modes, and material phases), which affects carrier mobility.

Conventional methods of device fabrication have been used to address performance issues with limited success. This work will address these issues through insulator and semiconductor engineering. Initial efforts will concentrate on engineering the gate insulator by using a high dielectric constant material. Specifically, BZN ($Bi_{1.5}Zn_{0.8+x}Nb_{1.3-x}O_7$) is a paraelectric pyrochlore system that boasts a high dielectric constant, low dielectric loss, and low co-firing temperature, making it a viable insulator for improving OTFT performance and enabling advanced circuit design [2]. Later phases of this work will focus on engineering the semiconductor deposition. Enhancements to standard evaporative deposition techniques will be explored by in situ coupling of new forms of energy to control pentacene thin-film morphology and defects.

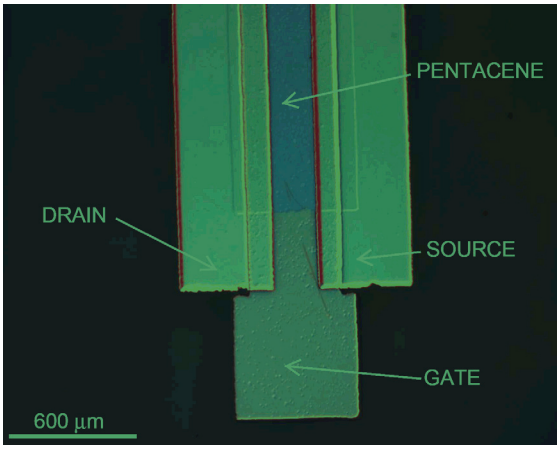

FIGURE 1: Pentacene OTFT top view micrograph

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High-performance Cold Cathodes for Sub-mm-wave Compact Sources

L. F. Velásquez-García, Y. Niu, S. Guerrera, A. I. Akinwande
Sponsorship: DARPA

The continued demand for very wideband communications and increased need for wireless channel capacity have led to the exploration of new regions of operation that will exploit the upper millimeter-wave spectral range. The broad minimum that occurs in atmospheric absorption between 200GHz and 300 GHz is largely under-utilized because of a lack of high-bandwidth and high-power amplifiers in this frequency range that are compact and efficient. The core of proposed vacuum amplifier technology is a field-emitter-array (FEA) cathode. Due to the exponential dependence of the emitted current on the emitter tip radius [1], emission currents are extremely sensitive to tip radii variation. In addition, research has shown that nm-sized emitter tips have a distribution with long tails [2]. Therefore, spatial variation of tip radius results in the spatial variation of the emission currents and hence the current density. The variation also results in non-uniform turn-on voltages even when the tips are located next to each other. Moreover, at a given voltage only a small fraction of the tips in an FEA emit because the sharper tips burn out early, before the duller tips emit, resulting in under-utilization of the FEA (Figure 1). Attempts to increase the emission current by increasing the voltage often result in burnout and shifting of the operating voltage to higher voltages. Spatial non-uniformity can be substantially reduced if arrays of emitters are ballasted [3]. Ungated FETs are ideal to individually ballast each emitter because they behave like current sources and can be fabricated with high emitter density FEAs [4]. Limiting the current from each emitter makes it possible to prevent destructive emission from the sharper tips while allowing higher overall current emission because of the emission of the duller tips. Using the ungated FET individual ballasting technology, we have demonstrated more than 600 mA of emission with no damage to the cathode (Figure 2).

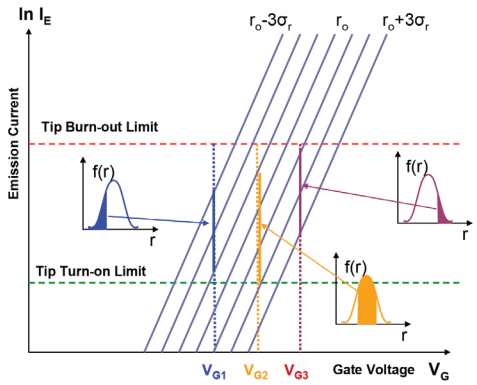

FIGURE 1: Emission current I_E versus gate voltage V_G for varying tip radii r. The tip radius has a distribution with variation σ and mean r_o. The emitter current falls within the turn-on limit (controlled by the noise floor) and the burn-out limit (due to ohmic heating). For a constant gate bias, only a small percentage of the tips contributes to the total emission current.

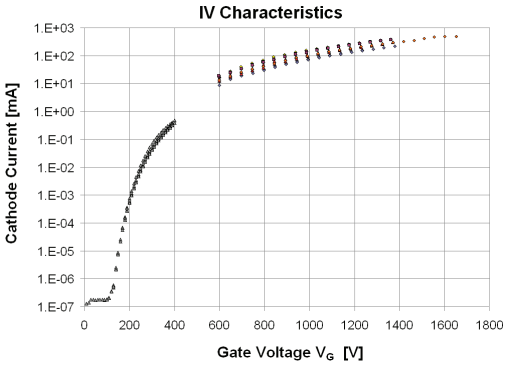

FIGURE 2: The DC (low-current) and pulsed (high current) IV characteristics of a 1-million field emitter array. More than 600 mA of current were measured with no damage to the cathode.

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Reproducible Lithographically Patterned Metal-oxide Transistors for Large-area Electronics

A. Wang, B. Yaglioglu, C. G. Sodini, V. Bulović, A. I. Akinwande
Sponsorship: SRC/FCRP C2S2

Metal-oxide-based field-effect transistors (FETs) have been demonstrated with higher charge-carrier mobilities, higher current densities, and faster response performance than amorphous silicon FETs, which are the dominant technology used in display backplanes [1], [2]. Because the optically transparent semiconducting oxide films can be deposited at near-room temperatures, these materials are compatible with future generations of large-area electronics technologies that require flexible substrates [3]. Our project aims to develop a low-temperature, scalable lithographic process for metal oxide-based FETs that can be integrated into large-area electronic circuits.

While any single demonstrated transistor may have excellent characteristics, circuit design using these FETs is impossible without the capability to reproducibly fabricate FETs with uniform characteristics. Previously, we demonstrated top-gate, fully lithographic FETs of varying channel lengths on 100-mm glass wafers with a sputtered ZnO:In_2O_3 channel layer, using an organic polymer, parylene, as the gate dielectric and indium-tin-oxide (ITO) for source/drain contacts. Because of process non-uniformities, however, FET turn-off voltages (V_{OFF}) across a wafer and between wafer lots varied by as much as ±10V. By modifying the process to deposit semiconductor and protective dielectric together without breaking vacuum, the FET uniformity across wafers was improved; the standard deviation of V_{OFF} decreased to <1V across three subsequently-processed wafer lots. Figure 1 shows a photograph of a 100-mm glass after fabrication was completed; current-voltage characteristics for a device fabricated in the improved process are shown in Figure 2. This baseline process can provide a platform for the design of oxide FET-based circuits, as well as for studying the underlying device physics of metal-oxide FETs.

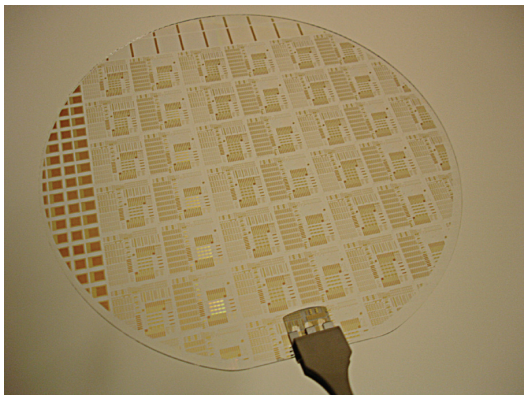

FIGURE 1: A 100-mm glass wafer with lithographically patterned metal-oxide field-effect transistors. Device uniformity can be examined by comparing transistors of the same geometry from different die across the wafer.

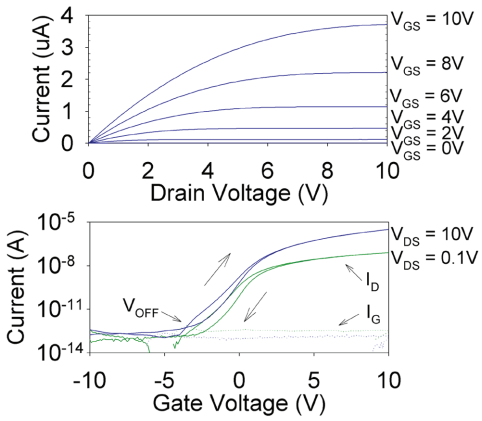

FIGURE 2: Current-voltage characteristics of lithographically patterned FET (W/L = 100mm / 100mm). Output curves are plotted in the top graph; double-swept transfer curves taken in saturation and triode regions are plotted on the bottom. The turn-off voltage, V_{OFF}, is -4V.

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High-electron-mobility Germanium MOSFETs: The Effect of n-type Channel Implants and Ozone Surface Passivation

J. Hennessy, D. A. Antoniadis
Sponsorship: SRC/FCRP MSD

Germanium n-channel devices have historically shown poor performance due to an asymmetric distribution of interface states that degrade electrostatic behavior and carrier mobility. In this work, we demonstrate two methods for improving the performance of Ge n-MOSFETs: ozone surface passivation and n-type ion-implantation. Figure 1 shows the interface state density (D_{it}) extracted near the middle of the bandgap by the conductance method for germanium samples receiving *in-situ* exposure to a high concentration of ozone immediately prior to Al_2O_3 gate deposition. Both n-type and p-type samples that received ozone treatment show a significant reduction in D_{it} compared to samples that received a standard wet clean only. This technique has also been shown to result in D_{it} reduction near both band edges and enhanced electron and hole mobility [1]. Previous work has demonstrated enhanced electron mobility for phosphorus-implanted Ge n-MOSFETs [2]. Figure 2 shows the effective electron mobility of Ge n-MOSFETs that received channel implants of arsenic or antimony in addition to ozone surface passivation prior to gate deposition. Devices receiving a 4×10^{12} cm^{-2} dose show a significant increase in electron mobility, particularly at low inversion densities, but also a degraded subthreshold slope and increased off-state current, indicating some buried-channel-like behavior. Devices receiving a 1×10^{12} cm^{-2} implant dose show little degradation in subthreshold slope but maintain a significant enhancement in mobility compared to un-implanted devices [1].

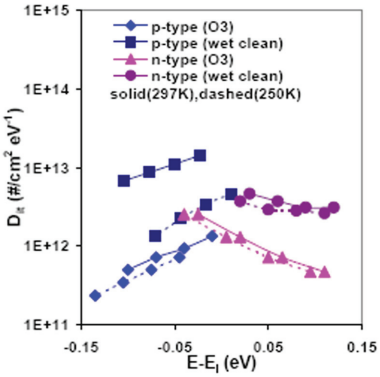

FIGURE 1: The D_{it} near the middle of the bandgap for ALD Al_2O_3 on O3-treated germanium substrates

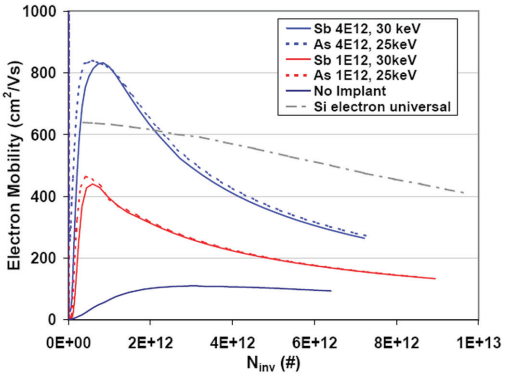

FIGURE 2: Effective electron mobility (split-CV) for As and Sb implanted germanium n-MOSFETs.

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Si/SiGe Tunneling Transistors

H. Lee, O. Nayfeh, L. Gomez, J. L. Hoyt, D. A. Antoniadis
Sponsorship: DARPA

The tunneling field-effect transistor (TFET) is interesting as a promising candidate for future complementary metal-oxide-semiconductor (CMOS) technology due to its potential for low-voltage operation. To successfully compete with conventional MOSFETs, it is important to decrease the sub-threshold swing (SS) and improve the drive current to reduce the power requirements. Theoretically the sub-threshold swing of TFETs could be scaled down to below 60 mV/dec at room temperature due to the band-to-band tunneling (BTBT) mechanism of operation. Optimization of tunneling current is complex since it depends on several parameters such as doping concentration and profile abruptness of the source, gate oxide thickness, and low band-gap material [1]. In this work, planar-heterojunction TFETs with Si/strained SiGe have been fabricated with two different nominal Ge concentrations (40 % and 70 %) and with gate oxide thicknesses of 2.5 and 3.5nm. Biasing conditions have been utilized in order to observe the different tunneling injection mechanism such as N-channel TFET (NTFET) and P-channel TFET (PTFET). The measurement has been done in NTFET mode by using an N+ bias (V_{N+} > 0) condition and a negative gate bias (see inset of Figure 1). The comparison of NTFET I-V characteristics between 70 % Ge and 40 % Ge content structures is shown in Figure 1. A device with 70 % Ge content displays an improved drive current and SS compared to a 40% Ge NTFET due to the reduction in tunneling barrier width and high mobility. Work is in progress with laser spike annealing (LSA) in order to improve performance by reducing Ge out-diffusion during implant activation. Figure 2 shows the comparison of NTFETs with varying oxide thickness. The device with the thinner gate oxide has improved drive current. This trait is due to the improved coupling of the gate potential to the channel [2].

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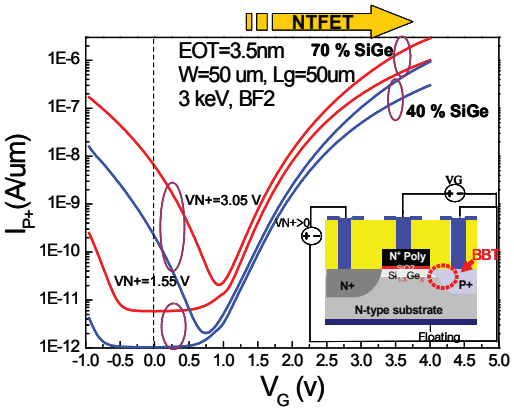

FIGURE 1: Measured transfer characteristics (drain current, I_{P+} versus V_G) for NTFETs with 40 % SiGe and 70 % SiGe. Increasing Ge content improves the drive current and sub-threshold swing. The inset shows a cross-sectional view of the fabricated TFET and an experimental bias setup condition for creating the NTFET operation mode.

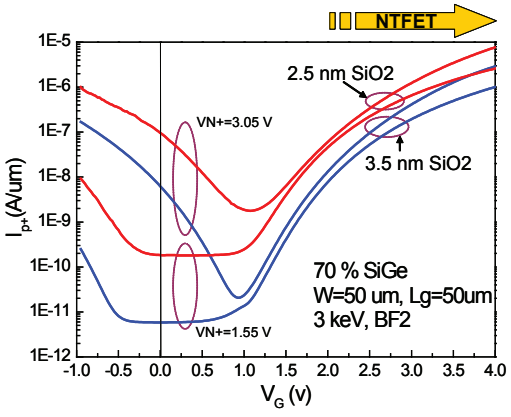

FIGURE 2: Measured transfer characteristics (drain current, I_{P+} versus V_G) for NTFETs with 2.5- and 3.5-nm-thick gate oxides.

Impact of Uniaxial Strain and Channel Orientation on Band-to-band Tunneling in Si/SiGe Heterostructures

O. M. Nayfeh, L. Xie, J. A. del Alamo, J. L. Hoyt, D. A. Antoniadis
Sponsorship: SRC/FCRP MSD, DARPA

Heterostructure tunneling field effect transistors (HTFETs) have potential for extremely low voltage operation (<0.3 V) [1]. These devices make use of the large gate-controlled band-to-band tunneling (BTBT) efficiency in Si/SiGe heterostructures due to the reduced energy gap of the material [2]. It is important to understand the physics of BTBT with varying channel orientations and applied additional mechanical uniaxial stress so as to design and engineer more optimal future devices that may encounter these conditions intentionally or unintentionally. Figures 1 and 2 show select measurements (I-V) of a Si/SiGe BTBT device with varying channel orientation and applied mechanical uniaxial compressive strain.

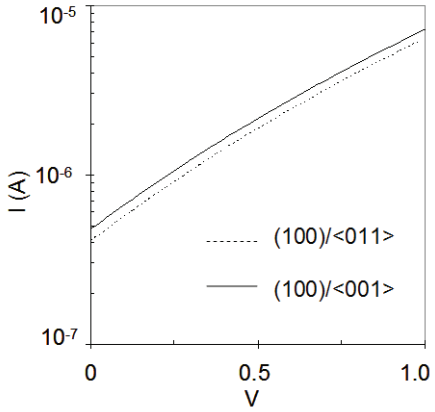

FIGURE 1: The Si/SiGe BTBT current for <001> and <001> channel orientations on (100) wafer.

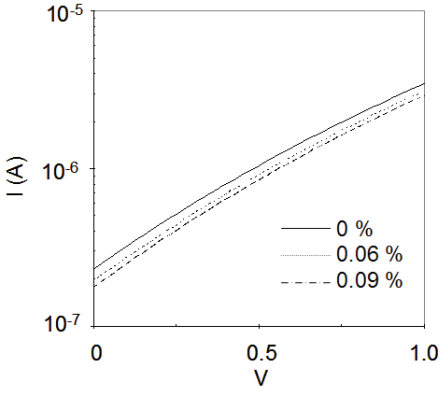

FIGURE 2: The Si/SiGe BTBT current for varying levels of applied mechanical uniaxial compressive strain.

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Nonvolatile Memory Devices with Nanoparticle/High-k Dielectric Tunnel-barrier Engineering

O. M. Nayfeh, J. Hennessy, D. A. Antoniadis, K. Mantey, M. H. Nayfeh
Sponsorship: SRC/FCRP MSD

Silicon-nanoparticle-based nonvolatile memory devices using uniformly delivered colloidal nanoparticles [1] are candidate replacement candidates for traditional polysilicon flash memory [2], [3]. Future devices are envisioned to require the use of high-k dielectrics for achieving suitable nonvolatile memory characteristics [2]. In this work we make use of novel heterojunctions formed between silicon nanoparticles and high-k dielectrics to design and construct more optimal nonvolatile memory devices using tunnel barrier engineering. Figure 1 shows a cross-sectional TEM of silicon nanoparticles embedded in an atomic-layer-deposited high-k dielectric (Al_2O_3). Figure 2 shows a select capacitance-voltage (C-V) hysteresis measurement of the device.

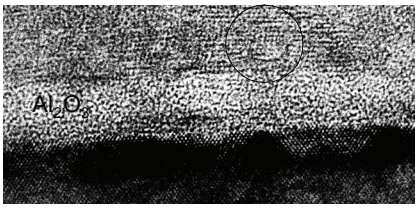

FIGURE 1: Example XTEM, a constructed device showing silicon nanoparticles (2.9 nm, circled) embedded in ALD-deposited Al_2O_3.

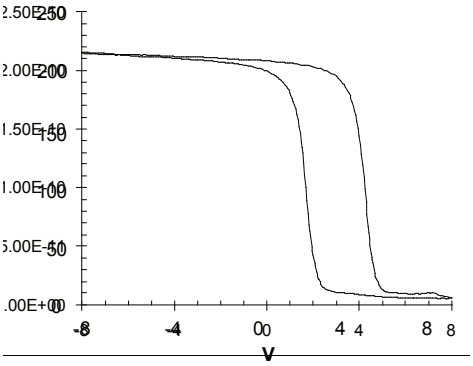

FIGURE 2: Capacitance-voltage (C-V) hysteresis characteristics of the device.

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Exciplex Transistors

J. Lee, C. L. Mulder, M. A. Baldo
Sponsorship: NRI/INDEX

Excitons, bound pairs of electrons and holes, mediate the interconversion of charges and photons and thus can be used for an efficient interconnect between electronic circuits and optical communication. The ability to guide excitons in space can lead to an excitonic switch that directly routes an optical signal. Recently, High et al. demonstrated an excitonic transistor using indirect excitons formed in AlGaAs/GaAs coupled quantum wells at a temperature of 1.4K [1]. The much larger binding energy of excitons in organic semiconductors could enable excitonic transistors at room temperature. Furthermore, by exploiting spin-disallowed transitions in organic materials, room temperature excitons can last up to milliseconds, more than sufficient to enable exciton propagation over large distances and the operation of sample circuits.

In this work we aim to demonstrate an exciton transistor based on organic semiconductors that can operate at room temperature. Exciplexes, indirect electron-hole pairs situated on adjacent molecules, are interesting because they are spatially oriented with a defined electron-hole spacing. The exciplex energy can be controlled by applying electric fields. We propose to guide exciplexes using the energy gradient determined by external electric fields (See Figure 1). In Figure 2, we show that by changing the voltage bias over a 4,4',4"-tris-(3-methylphenylphenylamino)triphenylamine (m-MTDATA)/bathocuproine (BCP) heterojunction, the energy of the exciplexes can be changed over 40meV, well above thermal energy at room temperature. We also observe that long-lived exciplexes can be created with a lifetime of several microseconds at room temperature in the phosphorescent system of N,N'-diphenyl-N,N'-bis(3-methyl-phenyl)-l,l'biphenyl-4,4'diamine (TPD)/iridium(III) bis(4,6-difluorophenylpyridinato-N,C2')-picolinate (Firpic). These results open a promising route toward the spatial manipulation of exciplexes in organic semiconductors.

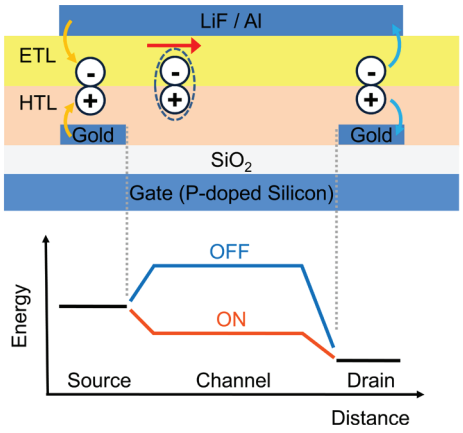

FIGURE 1: The device structure of the organic exciplex transistor and its energy profile under the operating condition. We control exciplex fluxes by modulating the gate bias and, thus, the potential barrier. The source creates exciplexes by injecting electrons and holes. The drain detects the exciplex fluxes by separating and extracting them with high reverse biases.

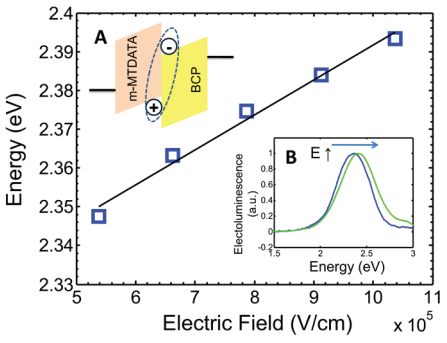

FIGURE 2: The control of the exciplex energy by an external electric field. The exciplex energy is changed over 40meV in an organic heterojunction of m-MTDATA and BCP. Inset (A): the organic heterojunction diode that exhibits exciplex emission. Inset (B): the electroluminescence spectra with low and high electric fields.

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Modeling of Deep-reactive Ion-etch Variation

J. O. Diaz, H. K. Taylor, D. S. Boning
Sponsorship: Sandia National Laboratories

Our modeling work with deep-reactive ion-etching (DRIE) has provided effective models to account for wafer-, die-, and feature-level non-uniformities [1]-[3]. The variation observed has been explained by spatial and temporal differences in the amount of F radical species at the wafer surface and their limited flux into features [4]. Despite our previous success integrating wafer- and die-level models, fundamental incompatibilities between these and most feature-level models had prevented us from integrating them together. We have revised our modeling methods to eliminate model compatibility issues. On the wafer- and die-levels, our new approach uses a simple electrical network analogue (Figure 1) to predict the time-evolving concentration of the etchant species available to the features. This prediction is used to provide estimates of the average etch rate in different regions within the wafer. The direct compatibility with the existing feature-level semi-physical models provides the flexibility to easily incorporate future effect-modeling enhancements such as sidewall etching and tapering. The model can also be tuned to specific tool-dependent etching characteristics and etch "recipes" by the fitting of parameters extracted from etch-depth measurements of wafers with pre-determined patterns. We are currently interested in unifying this model into a CAD tool capable of optimizing MEMS fabrication by accurately depicting the tradeoff between etching speed and uniformity in DRIE, which requires selecting and using the best feature-level model available. Additionally, we would like to expand current feature-level models to correctly account for the main sidewall effects relevant to the reliability of MEMS devices.

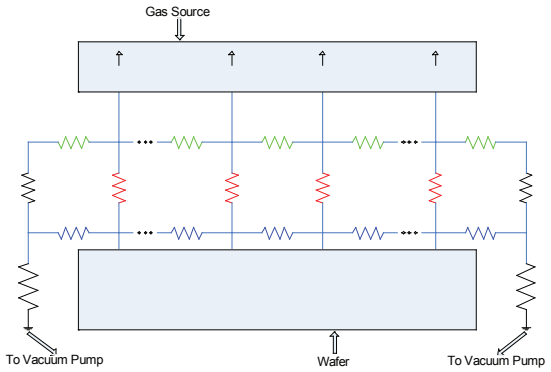

FIGURE 1: The electrical equivalent network used for DRIE wafer- and die-level modeling. In it, voltage corresponds to F radical concentration while current corresponds to radical flux in a given direction.

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Modeling of Electrochemical-mechanical Polishing (ECMP)

W. Fan, J. Johnson, D. S. Boning
Sponsorship: SRC/SEMATECH Engineering Research Center for Environmentally Benign Semiconductor Manufacturing

Electrochemical mechanical polishing (ECMP) is an emerging technology in semiconductor processes, used for Cu interconnecting layer planarization. In previous work, our group proposed a non-ohmic ECMP model to understand the exponential dependence of current on overpotential at the electrode/electrolyte interface and to calculate the Cu removal rate [1]. Based on electrochemical theory and process physics, the model has been well improved and extended to 3D accounting for lateral voltage/current distribution and Cu-layer resistance change during the process. The calculation is simplified by using equivalent circuit elements to simulate the electrochemical reaction.

As Figure 1(a) shows, the model captures the electrochemical reactions occurring at surfaces of both the wafer and the polishing pad using equivalent diode elements, and the lateral coupling distribution in the electrolyte is modeled using resistive elements.. Assuming that single-wafer rotation time is much shorter than total polishing time, radial time-averaged current density distributions on the wafer surface are calculated due to multiple voltage zones (Figure 1(b)). From the simulation result, we conclude that the model computes the current density of the chemical reaction in the water surface effectively (Figure 2(a)). Figure 2(b) shows the radial averaged current density, which is proportional to the instantaneous removal rate. Current work is seeking to calculate the Cu thickness evolution during the process and extract model parameters to fit experiment data.

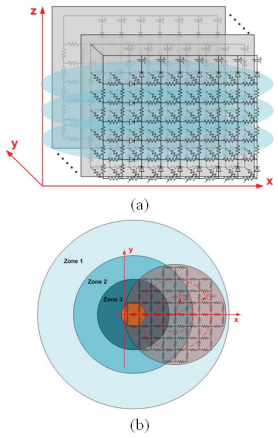

FIGURE 1: (a) Framework of the 3D ECMP model. The top voltage source level is a pad and the bottom variable resistors level is a Cu wafer. The electrolyte in the middle is simulated by pure resistors. The overpotential at electrolyte and wafer/pad surface is characterized by diodes. (b) Top view of pad showing multiple voltage zones and Cu wafer position. The wafer is connected to the ground via the contact point in the pad's center. From the wafer's center to its edge, the radial average current density is calculated along the red dashed circles.

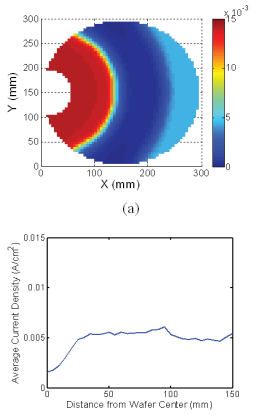

FIGURE 2: (a) The distribution of the current density of the chemical reaction on the wafer surface (A/cm^2) in the beginning of the process. The pad voltage zone settings are V_1=2V, V_2=1V, and V_3=3V. The blank area in the wafer image is the part under the contact point where no chemical reaction occurs. (b) The instantaneous current density along the wafer radius at the beginning of process. The removal rate and removal amount in each time step can be calculated with the current density.

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Stability of Metal Oxide-based Field-effect Transistors

B. Yaglioglu, A. Wang, K. Ryu, C. Sodini, A. I. Akinwande, V. Bulović
Sponsorship: Hewlett-Packard, DARPA

The main goal of this research is to combine a low-temperature budget fabrication method with scalable processes such as sputter deposition to realize oxide channel field-effect transistors (FETs) on glass or flexible plastic substrates. Oxide-based transistors offer an attractive alternative to commercially used amorphous Si transistors due to their high mobility values (~10-20cm²/Vs vs ~1cm²/Vs) [1-3]. Field-effect mobility, sub-threshold slope, and threshold voltage of FETs are the main parameters that are characterized for circuits. However, reliability of properties needs to be also addressed before these devices take their place in large-area electronic applications.

In this study we test the stability of FETs that have a polymer dielectric, parylene, and an amorphous oxide semiconductor, zinc indium oxide. The devices are processed lithographically at low temperatures (T ≤ 100 ºC). Figure 1 shows a typical transfer characteristics curve representing device performance. The inset gives the distribution of the threshold voltage across a 4-inch wafer. In Figure 2, the change in I-V characteristics is shown under a prolonged gate bias stress. The gate bias is interrupted at fixed times to record the transfer characteristics of the transistor at a drain bias of V_D=1V. Preliminary results of I-V tests show a positive shift in the threshold voltage. Two possible mechanisms that are originally proposed for similar shifts in amorphous Si FET's are metastable state generation in the semiconductor and charge trapping in the dielectric [4]. Stability experiments at different temperatures and bias gate voltages are conducted to understand the instability mechanisms in these hybrid (inorganic/organic) devices.

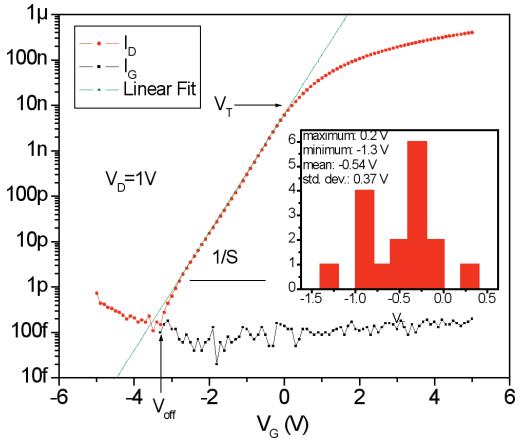

FIGURE 1: Transfer characteristics of a W/L=100µ/100µ transistor. Data are taken from -5V to 5V with 0.1V steps while V_D= 1V. The distribution of threshold voltage collected from 17 devices on different dies across the wafer is given in the inset.

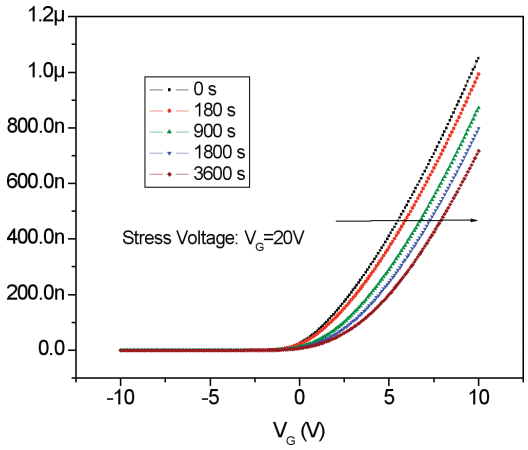

FIGURE 2: The V_G-I_D curve of a transistor as a function of stress time. The stress measurement is interrupted every 180s to measure the transfer characteristics. Measurements after 3min, 15min, 30min, and 1h are included to show the shift in the characteristics.

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Electrical Reliability of GaN HEMTs on Si Substrates

S. Demirtas, J. A. del Alamo
Sponsorship: ARL MURI

GaN High Electron Mobility Transistors (HEMT) are very promising devices for high power, high frequency applications due to the unique properties of the GaN system. However, their reliability is limited even when grown on traditional substrates such as SiC, which has a relatively good match with the GaN lattice. Recently, Si has emerged as a very attractive alternative to SiC substrates due to its low cost, availability and well-known characteristics. The disadvantage of using a Si substrate is the increased lattice and thermal mismatch with GaN. This brings new reliability concerns. In our work, we have carried out systematic reliability experiments on industrial devices from our collaborators Nitronex Corporation and Triquint Semiconductor to understand the mechanisms of electrical degradation of GaN HEMTs on Si.

One of the consequences of growing GaN-on-Si is an increased number of traps and other electrical defects. This is observable in fresh HEMTs. Figure 1 compares current transients observed in virgin GaN-on-Si and GaN-on-SiC devices after a 1 second pulse of -10V at the gate. The purpose of such a short pulse is to "pump" electrons into the traps which get negatively charged and hence suppress the 2DEG in the channel, causing a sudden decrease in drain current. As time goes on, these electrons will be detrapped from these states allowing the current to "recover" to its original value before the pulse. As the number of traps increase, more electrons will be trapped in these states and the initial current collapse is larger. In our experiments we monitor I_{Dlin}, which is the drain current at V_{DS}=0.5 V and V_{GS}=1 V. Our experiments show a higher current collapse and a slower recovery in devices on a Si substrate when compared to devices on a SiC substrate. Clearly this shows that the higher mismatch between the GaN heterostructure and the Si substrate causes more traps than on a SiC substrate.

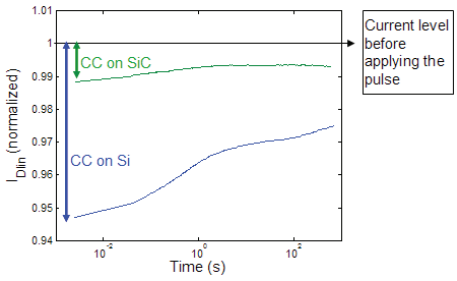

FIGURE 1: Comparison of current transients in fresh GaN-on-Si and GaN-on-SiC HEMTs after the application of 1 second pulse of value -10V at the gate. The current transient curves are normalized to the uncollapsed values of I_{Dlin}. Note the larger current collapse in GaN-on-Si HEMT due to increased number of traps caused by the larger substrate mismatch.

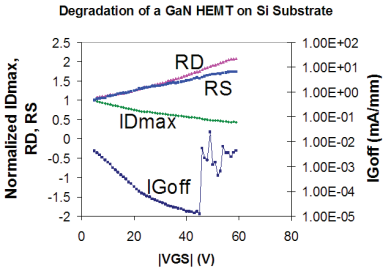

FIGURE 2: Output of the characterization suite utilized in our research for a typical electrical stress experiment. In this stress test, V_{DS}=0V and constant whereas V_{GS} is stepped from -5V to -60V by 1V every 10 seconds. R_D and R_S increase whereas I_{DMAX} decreases with increased stress. I_{GOFF} exhibits a decrease first until the critical voltage for degradation is reached where it increases by almost three orders of magnitude.

Our approach to the reliability testing of GaN-on-Si HEMTs is similar to that followed in [1] and [2]. We perform electrical stress experiments under a variety of conditions. An automated benign characterization suite monitors important figures of merit (FOM) of the devices such as maximum drain current (I_{DMAX}), gate leakage current (I_{GOFF}), drain and source resistances (R_D, R_S) throughout the experiment. Measurements of FOM take place at predefined intervals and the stress is interrupted during these measurements. Figure 2 shows the output of the characterization suite for I_{DMAX}, I_{GOFF}, R_D and R_S for a GaN-on-Si HEMT. In this test, V_{DS}=0 V and constant whereas V_{GS} is stepped from -5 V to -60 V by 1 V steps every 10 seconds. This is a typical case where R_D and R_S increase and I_{DMAX} decreases with increased stress. I_{GOFF} first decreases due to increased trapping with stress until it experiences an almost three orders of magnitude increase around a stress voltage of 45 V. This increase is permanent and the voltage that this occurs is referred to the critical voltage for I_{GOFF} degradation, V_{CRIT}. This is the key signature of degradation due to the inverse piezoelectric effect.

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RF Power CMOS for Millimeter-wave Applications

U. Gogineni, J. A. del Alamo
Sponsorship: SRC, Intel PhD Fellowship, IBM

Radio frequency (RF) power amplifiers are core components of almost all wireless systems. Traditionally III-V, SiC, or SiGe devices have been used in power amplifiers because of their ability to deliver high power and operate at high frequencies. Recently there has been an increased interest in using Si CMOS for designing single-chip integrated systems for operation in the millimeter-wave regime. Specific applications in this regime include wireless LAN and collision-avoidance radar. A key concern in using CMOS for these applications is the inability of CMOS to yield high-efficiency power amplifiers with power levels over 10 mW in the 60-80 GHz regime. In our work, we are investigating the fundamental limitations of using Si CMOS in power amplifiers and exploring options for device optimization with the goal of enhancing the millimeter-wave power-handling ability of Si CMOS.

Previous research in our group at MIT into the RF power performance of 65-nm and 90-nm Si CMOS devices [1], [2] has shown that the optimum device width that delivers the maximum power at any frequency (shown as open diamonds in Figure 1) scales down with increasing frequency. The effective cut-off frequency for power (frequency at which the output power drops below 10 mW) can be extrapolated to be around 20 GHz for 65-nm CMOS. Peak PAE and output power are strongly correlated to the maximum oscillation frequency (f_{max}) [1] and hence the decrease in output power for wide devices can be attributed mainly to a decrease in f_{max}.

To explain the f_{max} degradation in wide devices, small-signal equivalent circuits were extracted from the s-parameters measured on devices with different widths. The results show that the intrinsic parameters such as the transconductance (g_m) and intrinsic capacitances (C_{gs} and C_{gd}) are constant across width, but the extrinsic parasitic resistances (R_D and R_G) increase with increasing width. In this work, device width is increased by wiring multiple unit cells (each containing 24 fingers of 2 mm width) in parallel. The additional wiring between the cells results in higher parasitic resistances for the wider devices. Hence, the key to enabling CMOS for millimeter-wave power applications is a parasitic-aware approach to designing wide devices.

Several test structures with optimized parasitics have been designed and implemented on IBM's 65-nm and 45-nm CMOS technologies. Some of the design ideas being explored include (a) alternate ways of connecting elemental devices in parallel, and (b) use of multiple levels and thicker levels of metal to reduce interconnect resistance.

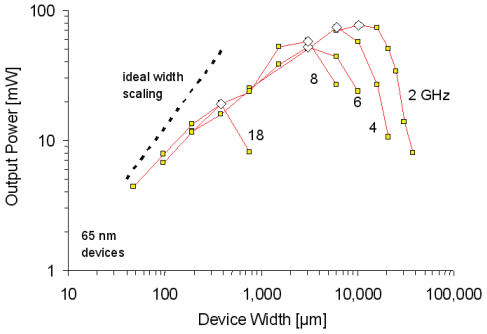

FIGURE 1: Maximum power (at peak PAE) vs. MOSFET width at different frequencies for 65-nm devices (V_{dd} =1 V) [1].

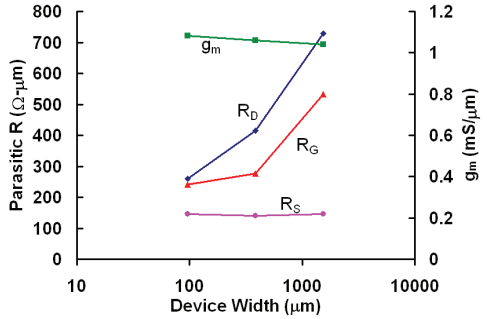

FIGURE 2: Normalized transconductance and parasitic resistances vs. device width for 65-nm devices (V_{dd}=1V, I_D=100mA/mm).

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Quantum Capacitance in Scaled-Down III-V HEMTs

D. Jin, J. A. del Alamo
Sponsorship: SRC/FCRP MSD, Intel Corporation

As Si CMOS fast approaches the end of the roadmap, finding a new transistor technology that would allow the extension of Moore's law has become a technical problem of great significance. Among the various candidates that are being contemplated, III-V-based Field-Effect Transistors represent a very promising technology due to the outstanding electron-transport properties of III-V compound semiconductors. In particular, InGaAs-based High-Electron-Mobility Transistors (HEMTs) fabricated at MIT exhibit great logic performance and constitute an excellent test bed to explore a future III-V CMOS technology [1].

In order to improve the logic performance of HEMTs, the barrier thickness needs to continue to scale down so as to maintain electrostatic integrity and enhance gate capacitance. However, as the barrier thickness approaches a few nanometers in thickness, the gate capacitance does not increase as much as expected as a result of the finite inversion-layer capacitance. This limit comes from two main contributions: finite quantum capacitance [2] and the centroid capacitance. The first one originates in the extra energy required to create a two-dimensional electron gas (2DEG) in a quantum well due to the finite density of states. The second one is related to the shape of the charge distribution in the inversion layer [3]. In scaled-down III-V HEMTs, due to the small effective mass of electrons in the channel, these two effects conspire to seriously limit the overall gate capacitance of the device and limit its current driving capability. Correct understanding of these effects and accurate modeling are essential to predicting the logic performance characteristics of future scaled III-V FETs.

In this research, we model the gate capacitance of HEMTs (Figure 1) and compare it with experimental measurements on devices fabricated at MIT (Figure 2). Using a one-dimensional Poisson-Schrodinger solver (Nextnano), we show that the overall gate capacitance of HEMTs can be modeled precisely as the series combination of an insulator capacitance and the inversion-layer capacitance. This one consists of a parallel combination of the contributions of each occupied electron subband. For each sub-band, the inversion-layer capacitance consists of the quantum capacitance (C_{Q_i}) and the centroid capacitance (C_{cent_i}), which are connected in series (Figure 1). We have performed S-parameter measurements and extracted the gate-capacitance characteristics of InGaAs HEMT structures with 4-nm barrier thickness in the linear regime [4]. The measurements agree very well with the modeled capacitance (Figure 2).

Our model suggests that in the operational range of these devices, the quantum capacitance significantly lowers the overall gate capacitance of the device. This research suggests that it is important to explore new ways to increase the quantum capacitance in order to develop scaled down III-V FETs with superior logic characteristics.

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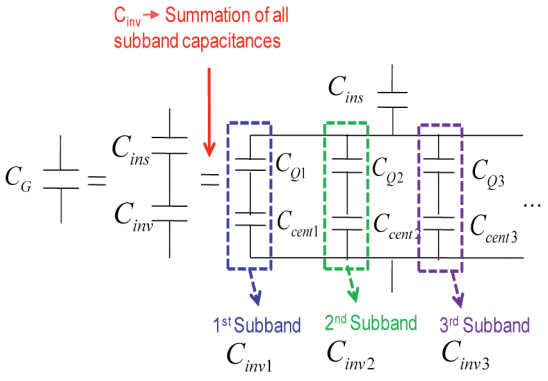

FIGURE 1: The gate-capacitance model used in this work. For each subband, the inversion-layer capacitance is the series of the quantum capacitance and the centroid capacitance.

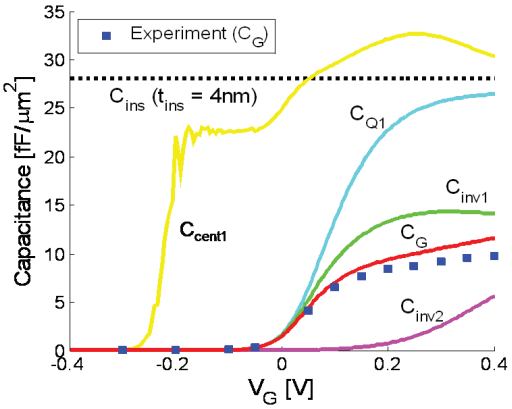

FIGURE 2: Experimental and modeled gate capacitance of 4-nm barrier thickness InGaAs HEMTs in the linear regime as a function of applied gate voltage. The 1st electron subband dominates in the HEMTs' operational range. The quantum capacitance severely brings down the overall gate capacitance.

RF Reliability of GaN High-electron-mobility Transistor

J. Joh, J. A. del Alamo in collaboration with TriQuint Semiconductor
Sponsorship: Army Research Laboratory (contract # W911QX-05-C-0087)

Thermally accelerated RF life tests (RFLT) are widely accepted as the most reliable ways to evaluate the lifetime of RF amplifiers in the field. However, RF life tests require a relatively complicated setup and an accurately determined and controlled device channel temperature, which is sometimes very difficult to achieve. The situation is particularly complex for high-power density technologies such as GaN high-electron-mobility transistors (HEMTs) or high-voltage GaAs-based devices. Also, in terms of understanding the physics of degradation, RFLT is somewhat cumbersome because a change in RF output power can result from a variety of different causes.

In order to overcome these complexities, DC life tests (DCLT) are often preferred due to their simplicity. In addition, during DCLT, better insight into failure mechanisms can be obtained by monitoring changes in various DC parameters such as the maximum drain current, I_{Dmax}, and the threshold voltage,V_T [1]. Though simple to implement, DC life tests have several limitations. First, the choice of stress bias conditions is not obvious. Second, DC life tests can at most only hope to emulate the DC conditions of the RF amplifier and not the impact of the RF waveform. Thus, they can be immune to some types of degradation (e.g., RF breakdown degradation) that could be present only under RF conditions. Third, DC life tests may not predict the lifetime under RF conditions if degradation of a wrong DC parameter that is irrelevant to RF power degradation is chosen as a failure criteria. It is then of great importance to establish a correlation between the degradation that is produced during DCLT and RFLT [2].

In this work, using TriQuint's X-Band GaN HEMT technology, we study how DC and RF figures of merit degrade during DC and RF stresses. Unlike conventional RF life tests in which only RF output power, P_{out}, and quiescent DC current, I_{DQ}, are monitored, we incorporated a characterization suite that extracts several DC parameters such as I_{DSS} (drain current at V_{GS}=0) and V_T in the RFLT. Under RF stress, it was found that I_{DSS} is a better indicator of P_{out} degradation than I_{DQ} (Figures 1 and 2). Similarly, during DCLT in which we regularly measure RF performance figures of merit, I_{DSS} degradation was found to correlate well with a drop in P_{out}. Other DC figures of merit such as I_{DQ} or V_T did not show a clear correlation with P_{out}. Also, we found that due to the larger voltage swing beyond the DC bias point, which prevails under large RF power input, RF stress can degrade GaN HEMTs much more than DC stress does even at the same V_{DS} and device channel temperature. In particular, the gate current can seriously degrade under RF stress, with a serious impact on P_{out}.

With this understanding of the correlation between DC and RF degradation, we can focus on DC figures of merit in DCLT that are more relevant to real RF output power degradation. This focus will help us understand physical degradation mechanisms of GaN HEMTs. Also, we can better design DC stress experiments that can accurately predict RF reliability.

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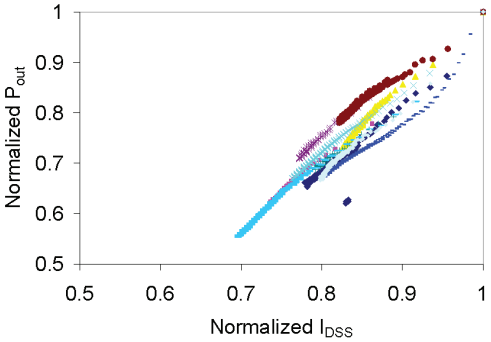

FIGURE 1: Correlation between degradation in P_{out} and I_{DSS} for 10 different devices from a single wafer.

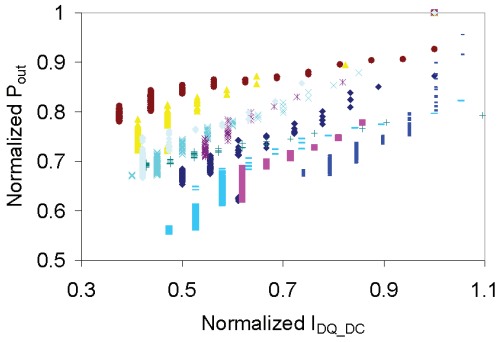

FIGURE 2: Correlation between degradation in P_{out} and I_{DQ_DC} for the same experiment in Figure 1.

Inverted-type InGaAs HEMTs for Logic Applications

T.-W. Kim, D. H. Kim, J. A. del Alamo
Sponsorship: SRC/FCRP MSD, Intel Corporation

As conventional CMOS scaling approaches the end of the roadmap, III-V-based FETs are seriously being considered as an alternative logic technology [1]. For any new device technology to take over the CMOS roadmap, electrical characteristics superior to those of Si CMOS are required in terms of performance (ON current and OFF current) and short-channel effects (evaluated through subthreshold swing and DIBL, among other figures of merit) at the required device dimensions [2]. The III-V high-electron-mobility transistor (HEMT) represents an excellent model system to study issues of relevance in future III-V MOSFETs. In order to gracefully scale into the deep sub-100-nm range, the barrier thickness (a wide bandgap semiconductor in the case of a HEMT) needs to be scaled down into the few-nm range. At MIT we are investigating InAlAs/InGaAs HEMTs with reduced InAlAs barrier thickness by three-step gate-recess process [3] and Pt-sinking-gate technology [4]. A drawback of a reduced barrier thickness is a large gate leakage current. In order to counteract this, we are currently investigating inverted-type InAlAs/InGaAs HEMTs where there are no dopants in the InAlAs barrier above the channel. The expected trapezoidal-shaped barrier should significantly reduce the gate leakage current level.

We have fabricated 30-nm gate-length inverted-type InAlAs/InGaAs HEMTs on InP substrate. The heterostructure was designed to have Si delta-doping layers both above and below the channel. In the intrinsic region of the device, the dopants are removed from the top barrier through a three-step gate recess process. In this way, a barrier thickness of 5 nm was achieved. Figure 1 shows the subthreshold characteristics of representative 30-nm inverted-type InGaAs HEMTs with typical conventional InGaAs. The inverted HEMTs exhibit a reduction in gate leakage current of around an order of magnitude when compared with conventional devices of similar dimensions. In addition, they show excellent short-channel effect characteristics with S = 66 mV/dec and DIBL = 80 mV/V. Figure 2 shows I_{ON}/I_{OFF} ratio as a function of gate length. The I_{ON}/I_{OFF} ratio of the inverted HEMTs is nearly 10^5 at V_{DD} = 0.5 V and it is fairly constant as the device scales down in size. These results reveal the benefits of the trapezoidal-shaped energy barrier under the gate. Unfortunately, there are drawbacks to this device design. These devices show a larger source resistance than conventional devices because of the high tunneling resistance associated with the higher energy barrier of the cap/barrier/channel region. The transconductance of 30-nm devices is 1.05 S/mm at V_{DS}=0.5 V and the source resistance is 0.39 Ω·mm, as extracted by the gate current injection method. For a process optimization, we hope to improve the performance of 30-nm inverted-type InAlAs/InGaAs HEMTs by reducing the parasitic resistances through a new ohmic contact scheme.

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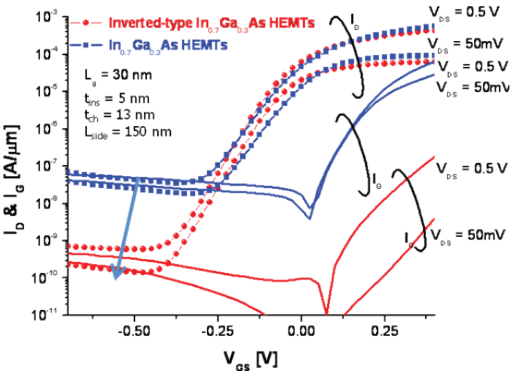

FIGURE 1: Subthreshold characteristics of inverted-type InGaAs HEMTs with conventional type InGaAs and channel normal HEMTs.

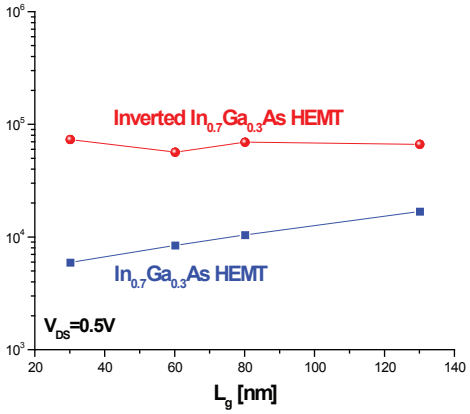

FIGURE 2: The I_{ON}/I_{OFF} ratio of inverted-type InGaAs HEMT and conventional InGaAs HEMTs as a function of gate length.

Impact of Strain on the Characteristics of InGaAs HEMTs

L. Xia, J. A. del Alamo
Sponsorship: SRC/FCRP MSD

With the incorporation of mechanical strain into the channel of Si MOSFETs, electron and hole mobilities have been improved by 2x and 3x, respectively, as compared with their unstrained counterparts [1], [2]. Just as with Si, it is of interest to study the impact of strain on the transport characteristics of InGaAs, a material that is currently receiving a great deal of attention as a post-Si CMOS logic technology. Our work studies the impact of strain on the electrostatics and transport properties of InGaAs High Electron Mobility Transistors (HEMTs).

We have fabricated a chip-bending apparatus that allows us to apply either tensile or compressive uniaxial strain to a small chip while conducting electrical measurements. Chips with size down to 2 mm x 4 mm can be accommodated. The strain level can be as high as +/-0.4%.

By applying unaxial strain to an n-channel InGaAs HEMT, we found that the threshold voltage shifts linearly with the applied strain, up to about 30 mV, as shown in Figure 1. This shift is due to the introduction of piezoelectric charge into the device due to in-plane strain and a change of the Schottky barrier height due to the hydrostatic pressure component. The linear regime transconductance also changes with strain. The underlying mechanism for this change is likely to be a combination of change in the electrostatic characteristics of the InGaAs quantum well and the mobility of 2DEG.

In parallel, we are fabricating our own p-channel III-V FETs in an effort to study the impact of mechanical strain on hole transport. We have developed a fabrication process for strain-free p-type $Al_{0.42}Ga_{0.58}As$/GaAs HEMTs. The saturation current and maximum transconductance of a 2-μm-long HEMT are 22 mA/mm and 16 mS/mm (at V_{DS}=-2 V), respectively. Figure 2 shows the output characteristics. However, the devices suffer from excessive gate leakage current that prevents them from being completely turned off. After solving this problem, we will be able to experimentally study the strain impact on p-channel III-V-based device performance.

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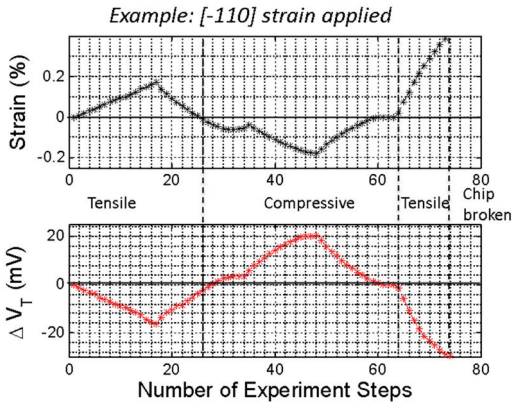

FIGURE 1: Threshold voltage (V_T) shift of n-type $Al_{0.23}Ga_{0.77}As$ / $In_{0.15}Ga_{0.85}As$ HEMT under strain. The V_T is defined as V_{GS} when I_{DS} = 1 mA/mm. Strain is applied parallel to the channel direction [-110].

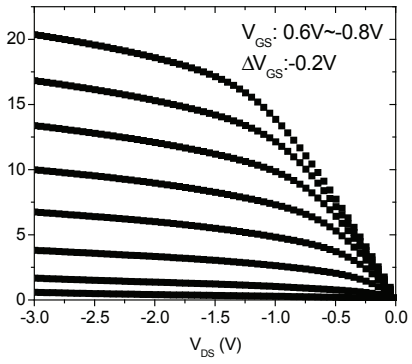

FIGURE 2: Output characteristics of p-type $Al_{0.42}Ga_{0.58}As$/GaAs HEMT. The gate length is 2 µm.

Advanced Substrate Engineering: Integration of InP Lattice Constant on Si

L. Yang, E. A. Fitzgerald
Sponsorship: SRC/FCRP MSD

Integration of the InP lattice constant with Si CMOS platforms is motivated by the monolithic interconnection of III/V optoelectronic and electronic devices with the highly integrated Si logic. However, integration of InP on Si requires a comprehensive solution that addresses lattice mismatch, thermal expansion mismatch, IV/III-V integration, and alloy engineering challenges.

We investigated III/V graded (Ñ) buffer on 6° offcut GaAs substrate in combination with 6° offcut Ge on Insulator (GOI) substrate to integrate InP on Si. First, we chose 6° offcut GOI as the substrate to accommodate the antiphase disorder in the IV/III-V integration [1] and established excellent GaAs epitaxy on the substrate with proper surface preparation. Then we investigated two paths to integrate InP on 6° offcut GaAs: GaAs/Ñ$In_xGa_{1-x}As$/Ñ$In_yGa_{1-y}P$/InP as shown in Figure 1 and GaAs/Ñ$GaAs_{1-x}Sb_x$/InP as shown in Figure 2. For the GaAs/Ñ$In_xGa_{1-x}As$/Ñ$In_yGa_{1-y}P$/InP path, we demonstrated the integration of InP on 6° offcut GaAs with a threading dislocation density (TDD) of $7.9x10^6$ /cm². The total Ñ$In_xGa_{1-x}As$/Ñ$In_yGa_{1-y}P$ buffer thickness is 4.0 um, which should be thin enough to avoid the cracking problem that can be caused by the thermal expansion mismatch between InP and Si. However, it was demonstrated that $GaAs_{1-x}Sb_x$ can be grown with compositions in the range of solid immiscibility [2]. We investigated GaAs/Ñ$GaAs_{1-x}Sb_x$/InP path to get InP lattice constant on 6° offcut GaAs. Ñ$GaAs_{1-x}Sb_x$ was gradually graded from GaAs to $GaAs_{0.51}Sb_{0.49,}$ which is lattice-matched to InP, and InP was deposited on top. The interface of $GaAs_{0.51}Sb_{0.49}$/InP still needs to be optimized to get good quality InP layer. For the next step, we will further optimize the GaAs/Ñ$GaAs_{1-x}Sb_x$/InP path and combine InP on GaAs together with GaAs on GOI to realize the integration of InP on Si.

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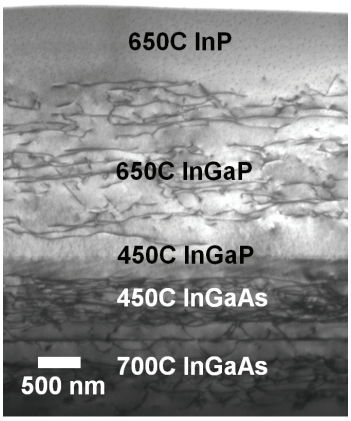

FIGURE 1: An XTEM of 6° offcut GaAs/ÑInx$Ga_{1-x}As$/Ñ$In_yGa_{1-y}P$/InP.

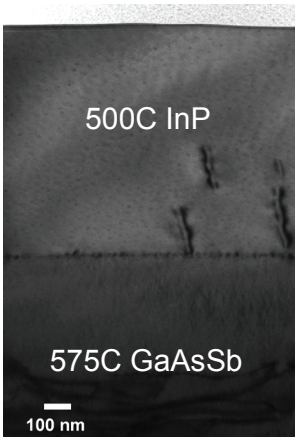

FIGURE 2: An XTEM of 6° offcut GaAs/Ñ$GaAs_{1-x}Sb_x$/InP.

Characteristics of Selectively Grown Ge-on-Si Photodiodes

N. DiLello, J. Yoon, M. Kim, J. Orcutt, J. L. Hoyt
Sponsorship: SRC student fellowship, DARPA

Germanium is a promising candidate for use in CMOS-compatible photodiodes. Its strong absorption in the 1.55-μm range and relative ease of integration on silicon substrates make it suitable for telecommunications systems and other high-speed electronic photonic integrated circuits. Important figures of merit for these photodiodes are the reverse leakage current and the responsivity. To reduce power consumption and improve the signal-to-noise ratio, the diodes must have a low leakage current in reverse bias and a high responsivity. This study has investigated the leakage current and responsivity of germanium photodiodes selectively grown by low-pressure chemical vapor deposition (LPCVD) using an Applied Materials epitaxial reactor.

To fabricate these diodes, germanium was grown selectively in oxide windows on a p+ Si substrate. The wafers then received an *in-situ* cyclic anneal to reduce the threading dislocation density. The wafers were subsequently implanted with phosphorus to create a vertical *pin* junction and contacted with metal. In this study, the Ge thickness was either 1 μm or 2 μm. The current vs. voltage characteristics for 100-μm square devices show that the dark current is ~250 nA at -1 V for both of these samples, as indicated in Figure 1. It has previously been noted that the threading dislocation density of Ge-on-Si films decreases with increasing thickness, indicating that film quality is better for thicker samples [1]. This suggests that Ge film quality is not the limiting factor in this case and more study is needed to further characterize the dark current. Figure 2 shows the responsivity vs. wavelength plot for both 1-μm- and 2-μm-thick samples. At -1 V and 1550 nm, the 1-μm sample and 2-μm sample have responsivities of 0.23 A/W and 0.46 A/W respectively. This 2x increase in responsivity is consistent with the increase in Ge thickness.

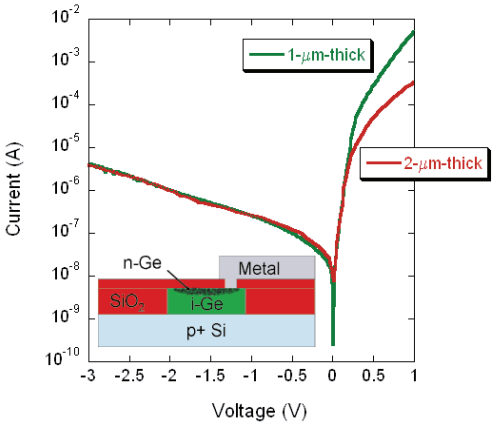

FIGURE 1: Current vs. voltage for a 1-µm-thick (green) sample and a 2-µm-thick (red) Ge sample. The dark current in reverse bias is virtually the same for both samples, suggesting that something other than material quality is limiting the leakage. Both devices are 100 µm square. Inset: Cross-sectional schematic diagram of a Ge-on-Si photodiode.

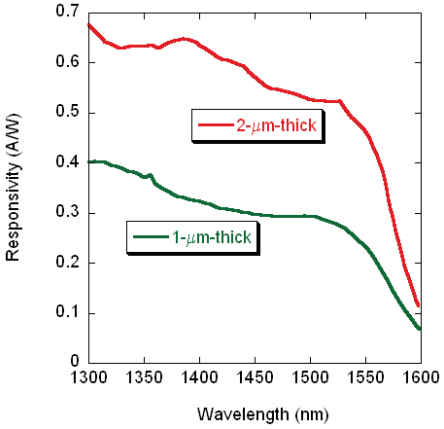

FIGURE 2: Responsivity as a function of wavelength for a 1-µm-thick (green) sample and a 2-µm-thick (red) Ge sample measured at a bias of -1 V. At 1550 nm, the responsivity of the thin sample is half of the responsivity of the thick sample. Both devices are 100 µm square.

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Scaled SiGe-channel p-MOSFETs on Insulator

L. Gomez, P. Hashemi, J. L. Hoyt
Sponsorship: SRC/FCRP MSD, MIT Lemelson Presidential Fellowship

Scaling of CMOS-device dimensions alone can no longer provide the necessary current drive enhancements required to continue historic performance gains. Strained-Si, SiGe, and Ge are under investigation as Si replacement technologies due to their enhanced carrier-transport properties [1]-[3]. Biaxial compressive strained-$Si_{0.45}Ge_{0.55}$ p-MOSFETs with gate lengths down to 65 nm have been fabricated to explore the merits of a strained-$Si_{0.45}Ge_{0.55}$ channel. Care was taken to avoid process steps that might alter or eliminate the strain in the channel. Hole mobility and velocity have been extracted and are benchmarked against a comparable Si control device. The dR/dL mobility extraction method was employed to determine the mobility of scaled p-MOSFETs with gate lengths in the range of 65-150nm [4]. Devices in this gate length range are observed to exhibit a 2.4x hole effective mobility enhancement over the Si hole universal mobility. Three velocity extraction methods were employed and the velocity characteristics of scaled strained-$Si_{0.45}Ge_{0.55}$ p-MOSFETs have been documented [5], [6]. A velocity enhancement is observed in stained-$Si_{0.45}Ge_{0.55}$ p-MOSFETs over control devices with a similar gate length and DIBL. The velocity enhancement is in the range of 1.1-1.3x. This enhancement is observed to increase with increasing proximity to the source injection point. Band structure and ballistic velocity calculations suggest that a substantial enhancement in velocity can be expected with the incorporation of Ge into the channel and the addition of uniaxial stress [7], [8]. Simulations predict that a moderate amount of Ge (e.g., $Si_{0.45}Ge_{0.55}$) coupled with -5 GPa of uniaxial stress can provide a velocity enhancement of 4.3x. This velocity is nearly two-fold larger than what Si is expected to provide with an equivalent amount of uniaxial stress.

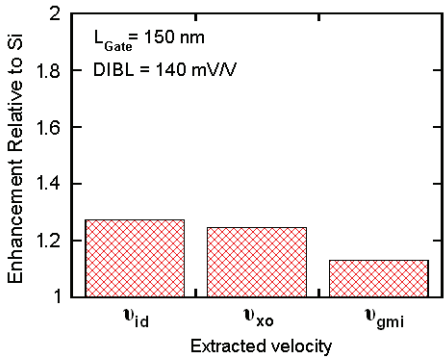

FIGURE 1: The enhancement relative to the Si control for the average υ_{id}, υ_{gmi}, and υ_{xo} extracted hole velocities. The strained-$Si_{0.45}Ge_{0.55}$ p-MOSFETs exhibit an enhancement over Si control devices ranging from 1.13-127x. All devices have an average L_{Gate} = 150 nm and DIBL = 140 mV/V.

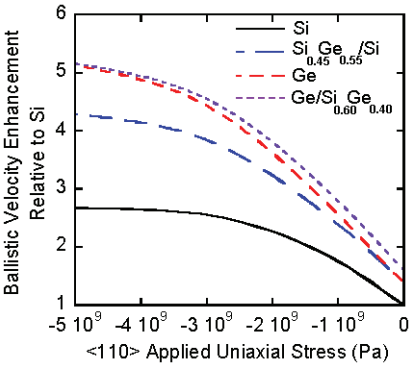

FIGURE 2: The simulated ballistic velocity enhancement relative to relaxed Si with applied compressive uniaxial stress for Si, biaxial compressive strained-$Si_{0.45}Ge_{0.55}$ pseudomorphic to relaxed-Si ($Si_{0.45}Ge_{0.55}$/Si), Ge, and biaxial compressive strained-Ge pseudomorphic to relaxed-$Si_{0.6}Ge_{0.4}$ (Ge/$Si_{0.6}Ge_{0.4}$). Simulations were performed using nextnano³ and FETtoy [7], [8].

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Uniaxial Strained-Si Gate-all-around Nanowire FETs

P. Hashemi, L. Gomez, J. L. Hoyt
Sponsorship: SRC/FCRP MSD, IBM Fellowship

Multi-gate device architectures such as tri-gate or Gate-all-around (GAA) nanowire (NW) MOSFETs are promising candidates for aggressively scaled Si-based CMOS due to their excellent electrostatics, low power consumption, and immunity to short channel effects [1], [2]. However, several effects such as quantum mechanical confinement effects and the non-ideality of the NW sidewalls play a significant role in degrading the performance of these devices. As a result, strain engineering of the Si NW channel is critical to improve device performance.

In this work, GAA strained-Si NW n-MOSFETs were fabricated using a top-down approach and their intrinsic and extrinsic performance was measured. Figure 1 shows a sample cross-section transmission electron microscopy image of a GAA strained-Si n-MOSFET, looking down the axis of the nanowires in the device channel, showing parallel nanowires with diameter ~ 8 nm, and LTO gate dielectric. Mobility of the GAA nanowires was extracted by measuring the intrinsic gate-channel capacitance using the split-CV method, after subtracting the parasitic capacitance measured on neighboring structures without NWs. The channel intrinsic conductance was corrected for series resistance. Figure 2 shows the electron effective mobility vs. average inversion charge density for ~49 nm-wide strained-Si GAA NWs, measured by both the 2-FET method and split CV, demonstrating excellent agreement between the two mobility extraction techniques. Universal (100) mobility and the mobility of planar SOI and SSDOI (t=8.7nm, close to the average thickness of strained-Si NW) and unstrained-Si NWs (W_{NW}=44nm) are also shown for comparison. The strained-Si nanowire shows mobility enhancement over universal, thin-body planar SOI and SOI NW devices (with the slightly smaller width of ~44nm).

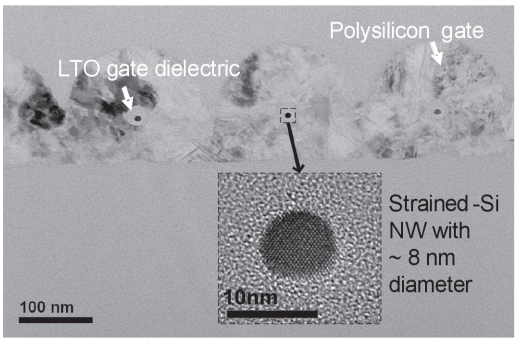

FIGURE 1: Cross-section transmission electron microscopy image of a GAA strained-Si n-MOSFET, looking down the axis of the nanowires in the device channel, showing parallel nanowires with diameter ~ 8 nm, and LTO gate dielectric [3].

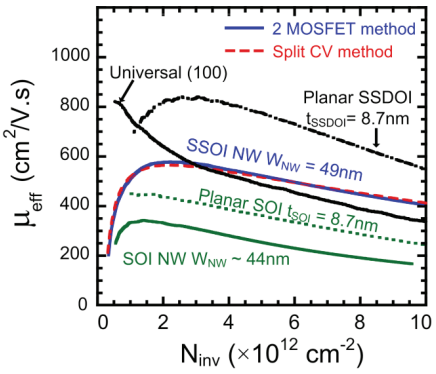

FIGURE 2: Low-field electron mobility (μ_{eff}) vs. average charge density (N_{inv}) of GAA strained-Si nanowire (W_{NW} = 49nm) measured by the split-CV and 2-FET methods. The μ_{eff} for the widest unstrained-Si nanowire (W=44nm), planar SOI, SSDOI (t=8.7nm), and universal are shown for comparison [4].

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A Superconductivity Switch Constructed in an EuS/Al/EuS Sandwich Structure

G. X. Miao, C. H. Nam, C. A. Ross, J. S. Moodera
Sponsorship: NSF, ONR

Superconductivity is known to be tunable with spin-polarized carriers as the excess spins suppress the spin singlet state of Cooper pairing [1]. In this work we attempt to use a magnetic insulator to generate net spin accumulations in a thin superconducting Al layer. It was shown that the exchange interaction between the conduction electrons and the first ferromagnetic layer can lead to large spin-dependent variation in the superconducting transition temperatures [2]. We take advantage of such properties and show that large Zeeman splitting is indeed generated inside the thin Al layer, and that the Al film can be driven back and forth between its normal state and superconducting state with an external field, leading to virtually infinite magnetoresistance (Figure 1). When the lateral dimension of the structure is reduced (for example, see structures in Figure 2), we start to see very complicated magnetic responses, as a result of the domain wall formation and propagation. Our current study focuses mainly on the effect of domain walls on superconductivity and the use of nanoconstrictions in tuning the resulted magnetoresistance.

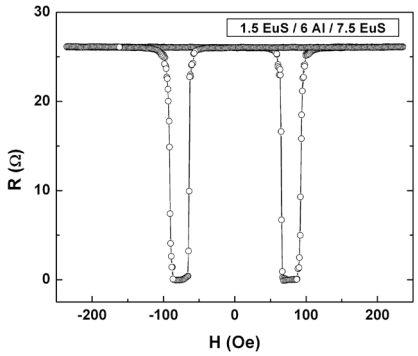

FIGURE 1: Illustration of the superconducting switch behavior in an unpatterned sandwich sample with the structure (in nm): glass/1 Cr/ 1.5 EuS/6 Al/7.5 EuS/15 Al_2O_3.

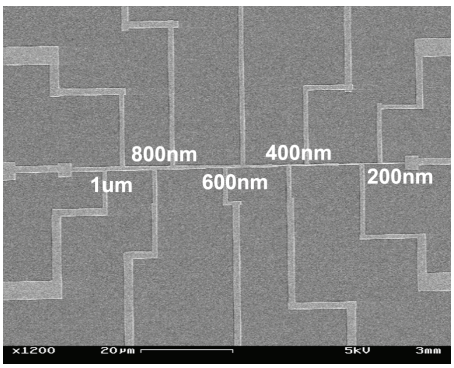

FIGURE 2: An SEM image of e-beam patterned nanostrips. A single lift-off step is used in its fabrication.

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Charge Transport Studies in Single-crystal Organic Field-effect Transistors

K. V. Raman, J. S. Moodera
Sponsorship: ONR, KIST

The research is motivated by the current development in the field of organic electronics [1]. Organic materials provide cheap, low-cost, mechanically flexible, and chemically tunable devices with performances comparable to or even better than amorphous Si. Also, these materials possess relatively good spin-transport properties [2-4], generating significant interest in these materials.

We have investigated charge transport in single crystals of organic semiconductor (OS), rubrene, with ferromagnetic electrode (FM) viz Co in addition to the conventional Au electrodes. Unlike that of gold, the surface stability of these electrodes to air is crucial and requires smart processing and fabrication steps to have clean FM-OS interfaces. A thin layer of Al (~ 6-10Å, grown at low temperature (80K)) was used to protect the Co surface and was found to give lower contact resistance. On exposure to air, an Al_2O_3 layer is formed that serves as a good tunnel barrier for charge injection. Figure 1 shows the four terminal-transfer characteristics of our FET devices. A mobility of $2cm^2/V\text{-}s$ is reported with the observation of source-drain current saturation at higher gate bias, attributed to the strong columbic interactions of the polaron charge carriers in the accumulation layer. Such effects have been reported before in high -dielectrics like Ta_2O_3 [5]. However, our results show that by considerably increasing the charge density (in our case by having large gate capacitance $C_i \sim 35nF/cm^2$), these effects show up. To further confirm the origin of such effect to the intrinsic nature of charges in rubrene, measurements were performed using Au electrodes, as shown in Figure 2, showing similar results. This work tries to gain fundamental understanding of the complex charge-transport mechanisms in organic materials and also for the proposed research goal of injection-spin information in these materials.

We would like to acknowledge Professor Marc Baldo (EECS) and his graduate student Carlijn Mulder for helping us use their organic growth facility.

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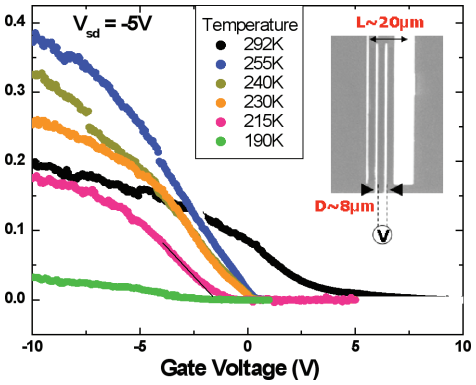

FIGURE 1: Surface conductivity vs gate voltage measured at different temperatures for Co/Al electrodes. Inset shows the 4-terminal electrode geometry (L– channel length, D- distance between the sense leads). Current saturation at high gate bias is observed and becomes stronger at lower temperatures.

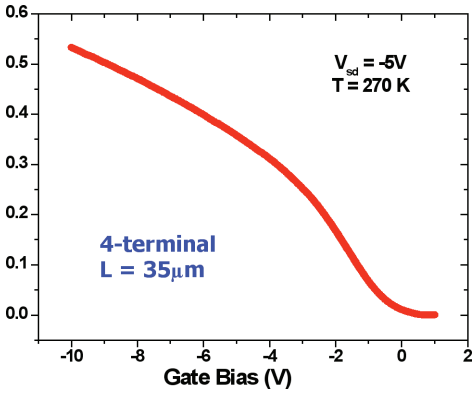

FIGURE 2: Surface conductivity vs. gate bias measured using Au electrodes. Current saturation is confirmed to originate due to the intrinsic nature of charge-carriers in rubrene.

Silicon and Silicon-Germanium Magnetic-tunneling-emitter Bipolar Transistors

M. van Veenhuizen, D. Choi, J. Chang, Y.-H. Xie, J. Moodera
Sponsorship: DARPA, KIST-MIT

We investigate a novel approach to spin-injection, based on the bipolar junction transistor, that has the potential to generate the large spin-currents inside the silicon needed to make functional spin-devices. Specifically, we employ the tunneling-emitter bipolar transistor with the emitter contact being a ferromagnet, as a spin-injection device. Tunneling-emitter bipolar transistors with a metallic emitter have been fabricated before [1], but never with the metal being a ferromagnet. We have successfully fabricated working transistors out of silicon, and Figure 1 shows an SEM micrograph of a device [1]. We find, however, that the current gain is very low, as seen in Figure 2 [2]. As we describe in [2], this can be attributed to recombination at the oxide-silicon interface due to the imperfect tunnel-barrier. Our current focus is on improving the tunnel-barrier quality. In addition, we are working on integrating this spin-injection device into a silicon-germanium heterostructure in order to inject spin into a silicon quantum well. The high-mobility quantum well has a very long spin-coherence length and the 2d confinement allows for the fabrication of functional spin-devices, as for instance the Datta-Das transistor [3].

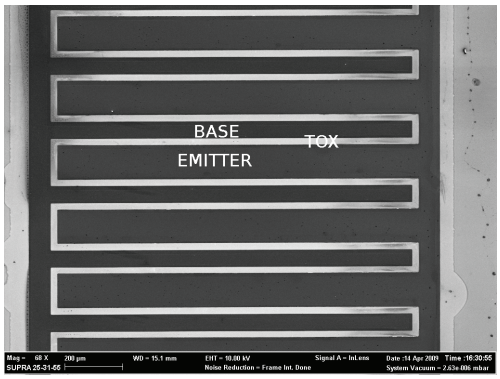

FIGURE 1: An SEM micrograph of a tunneling-emitter bipolar transistor. The base and emitter contacts consist of alternating long stripes, separated by a thermal oxide (TOX). The emitter consists of a ferromagnet/tunnel-barrier stack; for this device, iron/magnesium-oxide.

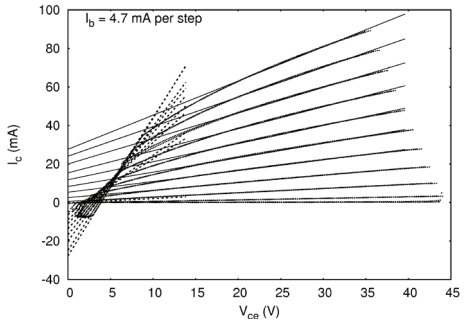

FIGURE 2: Collector current versus collector-emitter voltage for different base currents for the device shown in Figure 1 [1]. The current gain h_{FE} of the device is only slightly above 1. Also shown are fits to the initial and final slopes. The substantial final slope value is a result of the very thin base width, approximately 1000 Å.

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AlGaN/GaN Nanowire HEMTs

M. Azize, T. Palacios
Sponsorship: ONR

The high-frequency performance of $Al_xGa_{1-x}N$/GaN high-electron-mobility transistors (HEMTs) has rapidly increased in recent years. Transistors with current gain cut-off frequencies (f_T) above 160 GHz and power gain cut-off frequencies (f_{max}) of more than 200 GHz have been reported [1], [2], which enables the use of these devices in power amplifiers for mm-wave applications. In spite of these excellent results, the frequency performance of these devices is still far from its theoretically limit. Access resistances as well as short channel effects are currently limiting this performance. In this project, we are developing nanowire-based nitride HEMTs to overcome these limitations and to explore the maximum frequency of nitride devices [3].

Our work is based on the top-down fabrication of GaN nanowires on AlGaN/GaN structures grown by metallorganic chemical vapor deposition (MOCVD) on Si substrates. E-beam lithography is used to fabricate define nanowires with diameters (d) in the 30-200 nm range. After patterning of the nanowire, the sample is etched in a Cl_2-based dry-etching systems. Figure 1 shows a scanning electron micrograph of a typical device with $Al_xGa_{1-x}N$/GaN nanowires fabricated between the drain and source contacts. Preliminary measurements of these devices show an important improvement in the contact resistance as the nanowire diameter is decreased down to 50 nm (Figure 2), as well as negligible degradation in the transport properties. These low-contact resistances, in combination with the high electrostatic integrity and material quality of nanowire structures, are expected to render excellent frequency performance.

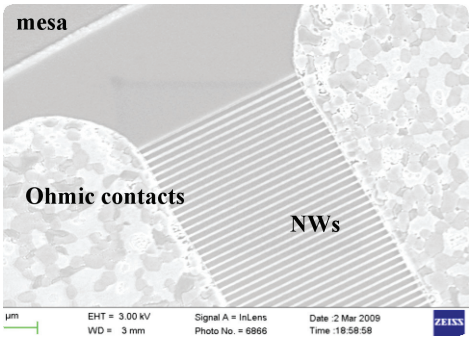

FIGURE 1: Scanning electron microscopy of AlGaN/GaN nanowires between two ohmic contacts. The diameter and the pitch of the nanowires are 60 nm and 170 nm, respectively.

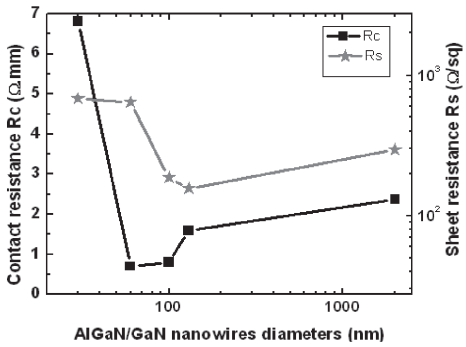

FIGURE 2: Contact and sheet resistances as function of the AlGaN/GaN nanowire diameter.

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Seamless On-wafer Integration of GaN HEMTs and Si(100) MOSFETs

J. W. Chung, J. Lee, E. L. Piner, T. Palacios
Sponsorship: DARPA YFA, SRC/FCRP IFC, KFAS

The integration of III-V compound semiconductors and silicon (100) CMOS technologies has been a long-pursued goal. A robust low-cost heterogeneous integration technology would make the outstanding analog and mixed-signal performance of compound semiconductor electronics available on an as-needed basis to realize key functions on VLSI chips that are difficult to implement in Si technology. The GaN-based devices are one of the best candidates for the integration with Si. While Si electronics has shown unsurpassed levels of scaling and circuit complexity, GaN devices offer excellent high-frequency/power performance as well as outstanding optoelectronic properties. The ability to combine these two material systems in the same chip and in very close proximity would allow unprecedented flexibility for advanced applications. In this project, we demonstrate the first on-wafer integration of AlGaN/GaN high-electron-mobility transistors (HEMTs) with Si(100) MOSFETs.

The key enabling technology is the fabrication of a *Si(100)-GaN-Si(100) virtual substrate* (Figure 1) through a wafer bonding and etch-back process described in [1]. On this substrate, a standard Si MOSFET was first fabricated. Then, the top Si layer was locally removed, exposing the AlGaN surface, and GaN HEMT devices were fabricated in those regions (Figure 2). It should be highlighted that in our technology, the Si devices are fabricated on Si(100) without any miscut and following a conventional Si process flow. Due to the very high thermal stability of GaN, the Si process did not affect the electrical properties of the embedded GaN layer.

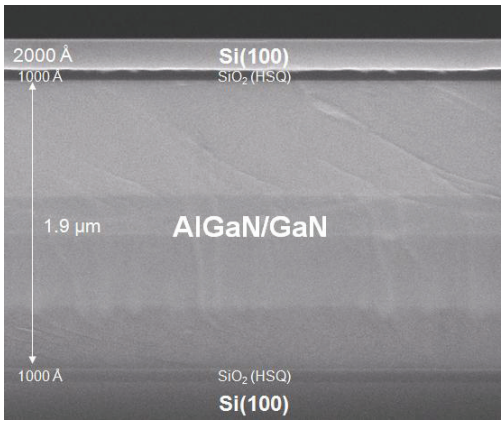

FIGURE 1: A cross-section scanning electron microscope (SEM) image of *Si(100)-GaN-Si(100) virtual substrate* through the layer transfer technology described in [1].

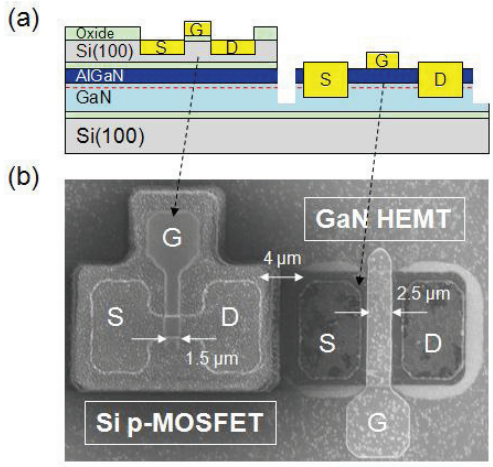

FIGURE 2: a) A cross-section schematic of fabricated Si p-MOSFETs and GaN HEMTs. b) A top SEM view of the fabricated transistors.

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AlGaN/GaN Vertical Power Transistors

B. Lu, T. Palacios
Sponsorship: Deshpande Center for Technological Innovation, MIT Energy Initiative

Due to the high critical electric field (more than 3MV/cm) and high density and mobility 2-dimensional electron gas (2DEG) induced by polarization charges, AlGaN/GaN transistors have attracted great interest for use in high-power electronics. As shown in Figure 1, AlGaN/GaN high-electron-mobility transistors (HEMTs) have already exceeded the theoretical performance limit of Si power transistors and they are approaching the limit of SiC.

Most AlGaN/GaN HEMTs are horizontal devices [1]. However, in high voltage applications, vertical transistors are highly preferred due to their lower parasitic inductance, higher blocking voltage, and smaller size. There have been several reports on GaN vertical transistors such as the current aperture vertical electron transistor (CAVET) [2] and the vertical trench gate GaN MOSFET [3], but they all suffer from either high leakage current or poor channel mobility. Moreover, they were fabricated on expensive bulk GaN substrate, which makes their commercialization very challenging.

In this project, we are developing a new approach to fabricate vertical AlGaN/GaN power transistors based on substrate removal and wafer-transfer technology. These new devices combine the excellent transport properties of horizontal transistors with the high power-handling capability of vertical devices. In addition, these new devices provide at least a 10-fold reduction in fabrication cost. Figure 2 shows the I-V curves of our first generation vertical AlGaN/GaN transistors

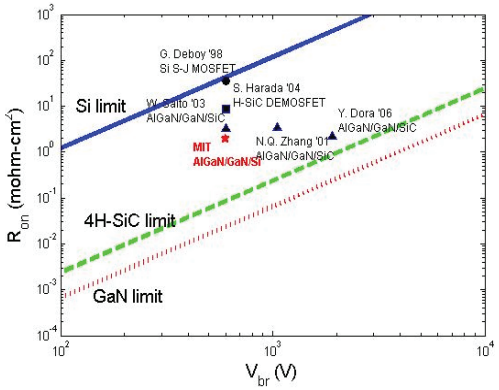

FIGURE 1: Blocking voltage (V_{br}) vs. on resistance (R_{on}) for Si, 4H-SiC and GaN with experimental data comparing the state-of-art Si super-junction MOSFET, SiC DEMOSFET, and AlGaN/GaN HEMTs.

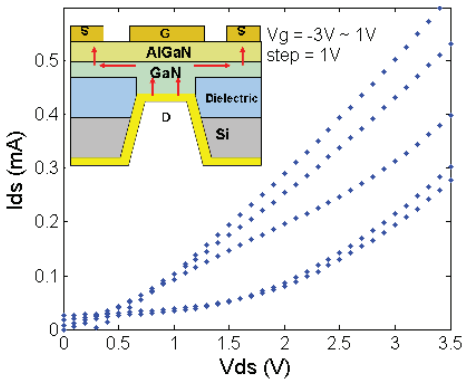

FIGURE 2: The V_{ds} - I_{ds} curve of our first-generation vertical AlGaN/GaN transistor and a schematic of the current flow in the transistor.

REFERENCES

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[2] S. Chowdhury, B. L. Swenson, and U. K. Mishra, "Enhancement and Depletion Mode AlGaN/GaN CAVET with Mg-Ion-Implanted GaN as Currrent Blocking Layer," IEEE Electron Device Lett., vol. 29, no. 6, June 2008.

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AlGaN/GaN Vertical Power Transistors

B. Lu, T. Palacios
Sponsorship: Deshpande Center for Technological Innovation, MIT Energy Initiative

AlGaN/GaN high-electron-mobility-transistors (HEMTs) have attracted great interests for use in high-power electronics, due to their high critical electric field and high density and high mobility 2-dimensional electron gas (2DEG) induced by polarization of the AlGaN/GaN material system [1]. As shown in Figure 1, AlGaN/GaN high-electron-mobility transistors (HEMTs) have already exceeded the theoretical performance limit of Si power transistors and they are approaching the limit of SiC.

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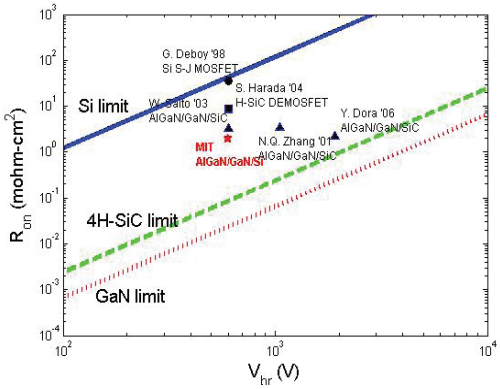

FIGURE 1: Blocking voltage V_B vs. on resistance R_{on} for Si, 4H-SiC and GaN with experimental data comparing the state-of-art Si super-junction MOSFET, SiC DEMOSFET, and AlGaN/GaN HEMTs.

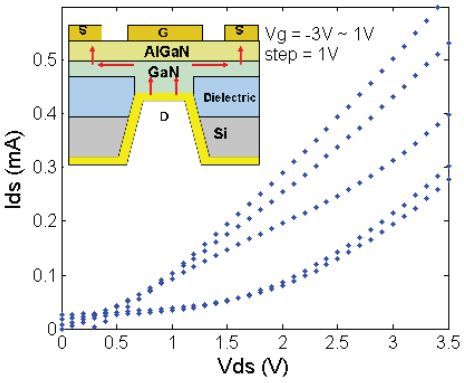

FIGURE 2: The V_{ds} - I_{ds} curve of our first-generation vertical AlGaN/GaN transistor and a schematic of the current flow in the transistor.

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[3] S. Chowdhury, B. L. Swenson, and U. K. Mishra, "Enhancement and Depletion Mode AlGaN/GaN CAVET with Mg-Ion-Implanted GaN as Currrent Blocking Layer," IEEE Electron Device Lett., vol. 29, no. 6, June 2008.

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Self-aligned AlGaN/GaN HEMTs

O. I. Saadat, J. W. Chung, T. Palacios
Sponsorship: M/A-COM, ONR

Applications like anti-collision car radars and point-to-point wireless transmitters stand to benefit greatly from the development of compact solid-state amplifiers at frequencies above 30 GHz. The AlGaN/GaN HEMTs are uniquely suited for such applications because of their high electron velocity, current density, and critical electric field. To increase the frequency performance of these devices, it is important to reduce not only the gate length but also the source and drain access resistances by minimizing the distances between the source and gate and the drain and gate contacts, respectively [1]. We are currently developing a new fabrication technology to self-align the gate contact to the ohmic contacts to minimize these distances.

In order to fabricate self-aligned HEMTs, T-shaped gates, like the one shown in Figure 2a, are fabricated by using e-beam lithography. Then, these gates are used as a shadow mask for a blanket ohmic metal deposition, which is then followed by the 870°C anneal. A proposed structure is shown in Figure 2b. This technology requires that the gate survives the standard ohmic annealing at 870°C. However, AlGaN/GaN HEMTs are normally fabricated with gate stacks composed of Ni-Au-Ni, which are not able to survive the ohmic metal anneal [2]. Therefore, in this project we have developed a new gate stack technology that can survive the 870°C ohmic anneal thanks to a combination of high-k gate dielectrics and tungsten, a refractory metal.

The new gate stacks developed in these process are also able to improve the transport properties of the AlGaN/GaN transistors. We studied the effect of different dielectrics on device performance by fabricating and testing W-dielectric HEMTs with Al_2O_3 and HfO_2 of different thicknesses along a W-dielectric HEMT with combination of a thin Ga_2O_3 interface layer with 12 nm of HfO_2. As shown in Figure 1, these devices have up to 20% higher transconductance than a standard HEMT with a Ni-Au-Ni gate stack. Due to the reduced gate leakage, positive gate voltages can be applied and drain current densities of up to 960 mA/mm can be achieved, which is a 40% improvement over a standard HEMT with a Ni/Au/Ni gate.

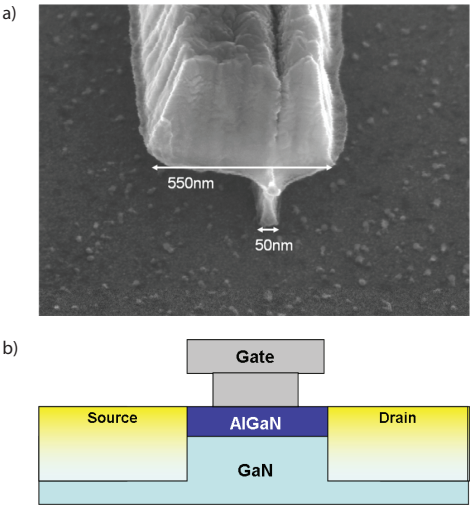

FIGURE 1: a) Scanning electron micrograph of an AlGaN/GaN HEMT with a 50-nm Ni/Au/Ni gate fabricated at MTL. b) Proposed structure with T-shaped gate and blanket ohmic metal deposition.

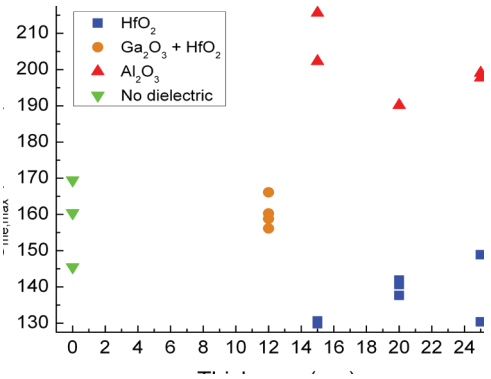

FIGURE 2: Transconductance vs. thickness for different dielectric thicknesses. Devices with the W-dielectric gate stack have up to 20% higher transconductance than devices with the standard Ni-Au-Ni gate stack.

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New Technologies for High-frequency GaN Transistors

H. Wang, T. Palacios
Sponsorship: ONR

The development of compact solid-state transistors at frequencies in the THz range (300 GHz-3 THz) can open the door to many exciting applications. THz imaging, concealed-weapon detection, ultra-high-speed point-to-point wireless transmitters, and highly efficient radars for the military are only a few of the many applications that would benefit from these devices. In this project, we explore new device structure and fabrication techniques to enable such transistors and related applications.

The GaN-based high-electron-mobility transistors (HEMTs) are one of the most promising options for power amplification and high-speed operations at frequencies above 150 GHz [1]. Reducing the gate length is crucial for increasing high-frequency performance; however, it becomes increasingly difficult to fabricate ultra-short gate-length devices. The smallest transistor gate reported in the literature for a HEMT is 22 nm [2]. In this project, we aim to shrink the gate length to sub-10 nm dimensions.

In parallel to the conventional method of defining small T-shape gates by using electron beam lithography, we also use carbon nanotubes (CNT) gates (Figure 1) as transistor gates. Single-wall CNTs can combine diameters as small as 2 nm [3] with very low resistivity.

In addition to the gate length, the distance between the gate and the channel is a critical dimension that strongly affects the frequency performance of transistors. Conventional AlGaN/GaN HEMTs need a relatively thick layer of AlGaN (>20 nm) to induce sufficient electrons in the channel. In this project, we use InAlN and AlN as the barrier layers. Both materials allow sub-10 nm gate-channel separation while providing high electron concentration. A recent InAlN/GaN HEMT with an 8.9-nm InAlN barrier, L_g=100 nm and L_{ds}=2.5 μm, fabricated in MTL shows current densities above 2.3 A/mm (Figure 2) at V_G=+2 V.

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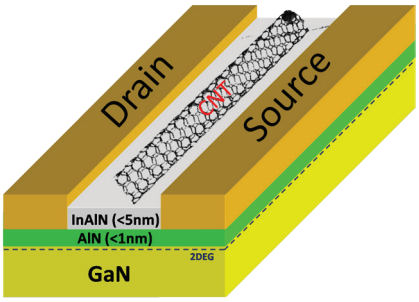

FIGURE 1: Envisioned HEMT with carbon nanotube gates. The effective gate length is much smaller than the diameter of the CNT due to its cylindrical shape.

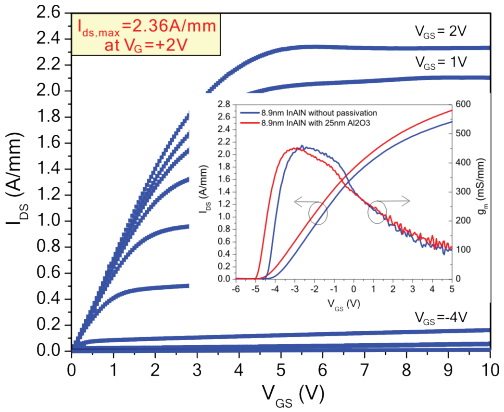

FIGURE 2: Current density (Ids) and transconductance (gm) of an InAlN HEMT with an 8.9-nm InAlN barrier, L_g=100 nm and L_{ds}=2.5 µm.

Generalized Drift-diffusion for Thermoelectrics

P. Santhanam, R. J. Ram
Sponsorship: DoD NDSEG, ONR, DARPA

To aid in the modeling and design of inhomogeneous thermoelectric elements with feature length-scales typical of micro-electronic devices, we have generalized the drift-diffusion (D-D) model to demonstrate the Seebeck effect. Since these new thermoelectric elements use the same semiconducting material-systems in similar ranges of doping and temperature as other electronic devices, the validity of the drift-diffusion framework remains, even as traditional models for thermoelectricity encounter challenges as modern nano-structuring techniques introduce features into thermoelectrics (TEs) on ever-shorter length-scales. Meanwhile, D-D models are substantially less computationally intensive than other valid techniques like direct Monte Carlo simulation of the Boltzmann Transport Equation (BTE) or quantum transport models. Beginning from the BTE and the Relaxation-Time Approximation, we have analytically re-derived a generalization of the traditional D-D equation that includes temperature-driven diffusion via a microscopically-defined Soret coefficient. We then solved this equation (see Figure 1) self-consistently with Poisson's equation to recover the Seebeck effect, thereby independently arriving at the previously-predicted [1] spatial variation of carrier-density within a homogeneously-doped semiconductor experiencing a temperature gradient and induced Seebeck voltage.

We also independently extended this model to include energy-dependent scattering [2], and further confirmed that both of these results align with the traditional theory as seen in Figure 2. Initial comparison of these findings with experimental data has been limited by the availability of data for materials with the simple bandstructure assumed in the simulation and direct measurements of the scattering parameter.

As the theoretical model is further validated, our attention turns to the modeling of inhomogeneous TE elements for thermal-to-electrical power conversion. Here the goal is to model both functionally-graded systems, whose parameters vary continuously from hot-side to cold, and segmented systems, which include interfaces between strongly differing material systems. In both types of inhomogeneous elements, however, the practical goal is to optimize the local material parameters for the expected operating temperature while ensuring compatibility between the operating points of various segments [3], [4].

Current investigations are underway into resolving the Peltier effect, another TE effect closely-related to the Seebeck effect, in the same theoretical and computational model. This work should permit the modeling and design of inhomogeneous elements for TE cooling, as the Seebeck effect does for power generation.

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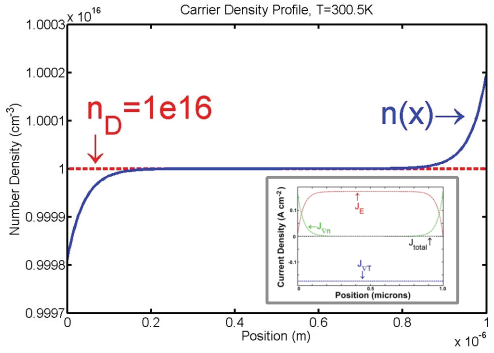


FIGURE 1: Spatial profile of carrier density for a solution in the computational generalized Drift-diffusion model. The associated source-specified current balance appears in the inset. This solution provides a real-space picture of microscopic thermoelectric transport and may form the basis for a new simulation technique useful for designing thermoelectric generators and coolers. The parameters for this simulation are taken from GaAs n-doped 1e16 cm^{-3} at 300K.

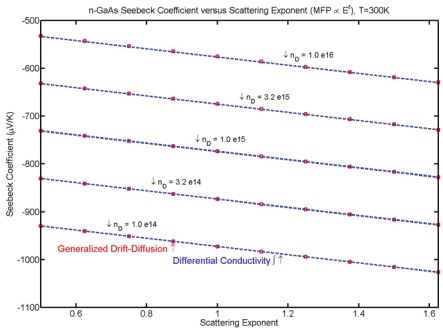


FIGURE 2: Comparison of the generalized Drift-diffusion model with calculations from the more common differential-conductivity model. Agreement is achieved for situations with energy-dependent relaxation time. Such systems hold promise for the improvement of thermoelectric efficiency. Experimental data is not presented for comparison because measurements of the scattering parameter r for these samples were not found.

Magnetic and Magnetoelectronic Memory and Logic

M. Mascaro, C. Nam, C. Garcia, D. Navas, B. Rasin, J. M. Florez, H. Koerner, V. Ng, C. A. Ross
Sponsorship: NRI INDEX program, NSF, Fulbright Fellowship

We are investigating the fabrication and magnetic properties of magnetic logic and memory devices. These consist of multilayer magnetoresistive ring-shaped structures as shown in Figure 1. The magnetic multilayers show giant magnetoresistance, in which the resistance is a function of the relative orientation of the magnetization directions in the magnetic layers. These small structures have potential uses in magnetic-random-access memories (MRAM), magnetic logic devices, and other magneto-electronic applications. Unlike that of conventional MRAM devices, the ring-shaped geometry of these devices allows for a complex response with multiple stable resistance states. This capability can be used for multi-bit memory and for programmable, non-volatile memory.

These devices are programmed using either a magnetic field or a current. Recently, we have been examining how the response of these structures depends on the magnitude of the magnetic field cycling. We found ranges of stable behavior where the response can be extremely uniform, and other field ranges where a variety of stochastic reversal paths occur. We have also shown that spin-polarized currents can reverse the devices in a low-power process. We are now exploring communication between these devices.

Simultaneously, we are exploring high-frequency behavior of magnetic nanostructures through giant magnetoimpedance. In GMI, the impedance of nanoscale structures varies dramatically with magnetic field and with frequency in the GHz range, and this variation can be used for sensitive magnetic field detection.

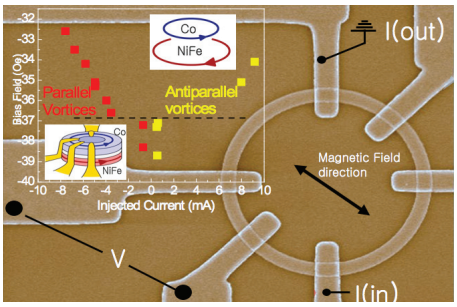
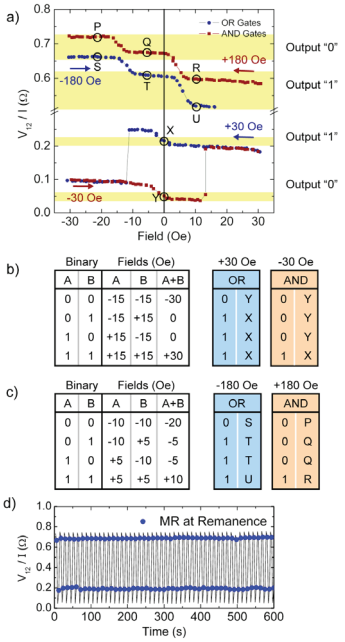


FIGURE 1: A magnetic ring made from Co/Cu/NiFe with diameter of 5 µm and several non-magnetic contacts overlaid. The inset shows the combination of current and magnetic field required to switch the ring from one magnetic state to another.



Binary A	Binary B	Fields (Oe) A	Fields (Oe) B	Fields (Oe) A+B	+30 Oe OR	-30 Oe AND
0	0	-15	-15	-30	0 Y	0 Y
0	1	-15	+15	0	1 X	0 Y
1	0	+15	-15	0	1 X	0 Y
1	1	+15	+15	+30	1 X	1 X

Binary A	Binary B	Fields (Oe) A	Fields (Oe) B	Fields (Oe) A+B	-180 Oe OR	+180 Oe AND
0	0	-10	-10	-20	0 S	0 P
0	1	-10	+5	-5	1 T	0 Q
1	0	+5	-10	-5	1 T	0 Q
1	1	+5	+5	+10	1 U	1 R

FIGURE 2: Electrical response of a magnetic ring tested under different field ranges, showing large resistance changes that can be used for logic operations.

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Dual-threshold-voltage Organic Thin-film Transistors for Mixed-signal Integrated Circuits

I. Nausieda, K. Ryu, D. He, A. I. Akinwande, V. Bulović, C. G. Sodini
Sponsorship: SRC/FCRP C2S2, Martin Family Fellowship

Organic thin-film transistors (OTFTs) hold the potential for large-area, flexible electronics because their near-room-temperature processing enables them to be fabricated on plastic substrates. We have developed a low temperature (≤95°C) process to fabricate integrated OTFTs [1]. Designing circuits using OTFTs is challenging since only p-channel transistors are typically available. The OTFT technology limits noise margins in digital circuits due to the lack of an NMOS load, the location of the threshold voltage (V_T), and the availability of a single V_T device [2]. We have addressed this problem by creating a dual V_T process, with the addition of only one mask to pattern a second gate metal. We present positive noise margin inverters and a near rail-to-rail ring oscillator using a 3V supply. The ring oscillator output waveform is shown in Figure 1.

The dual V_T process enables analog integrated circuits. We demonstrate an uncompensated, two-stage operational amplifier with open loop gain of 36dB, unity gain frequency of ~7Hz, and common-mode rejection ratio (CMRR) of 20.1dB. The dual V_T op amp has 30x better gain * -3dB frequency product than a single V_T implementation and uses a 5V power supply. The op-amp frequency response is pictured in Figure 2.

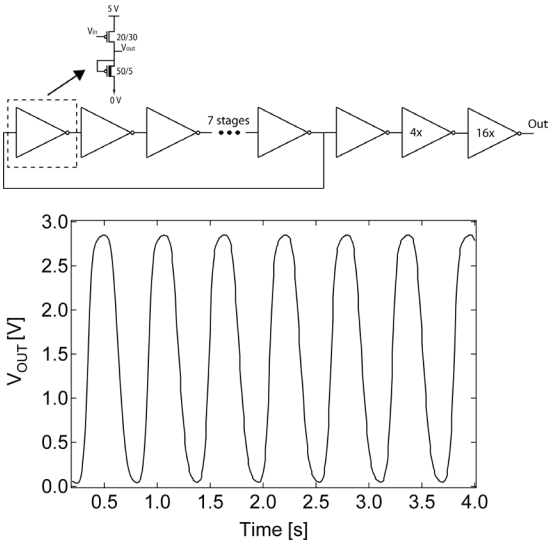

FIGURE 1: Schematic of 11-stage ring oscillator and buffer (top). A 1.7 Hz output transient, indicating an inverter propagation delay of 27 ms.

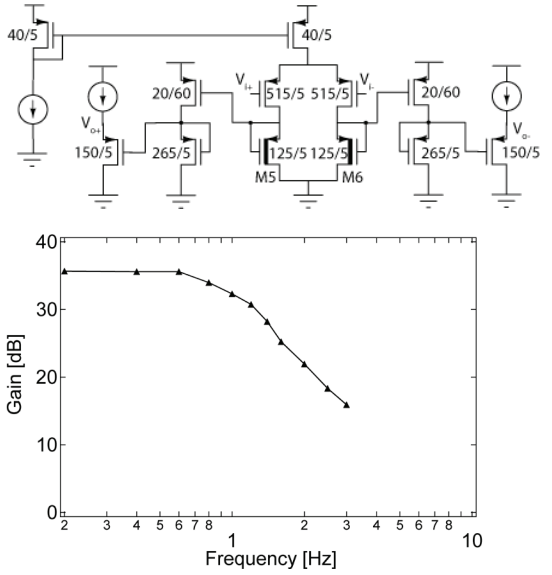

FIGURE 2: Schematic of op-amp (top). Open loop frequency response of dual V_T operational amplifier, indicating 2 poles (bottom).

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Effects of Bias Stress in Organic Thin-film Transistors

K. Ryu, I. Nausieda, D. He, A. I. Akinwande, V. Bulović, C. G. Sodini
Sponsorship: SRC/FCRP C2S2

Organic transistor technology holds the promise of large-area flexible electronics and integration of various sensors and actuators on a single substrate [1]. However, current-voltage (I-V) characteristics of organic transistors are known to change with the application of prolonged voltages [2]. Such change, termed the bias-stress effect, leads to operational instability, which limits the usable lifetime of the circuit. The bias-stress effect must be understood and minimized to enable the use of organic transistors in functional applications. In this work, we present a method to accurately measure the bias-stress effect and a model that predicts the effect at different stress conditions. The model provides physical insight into the mechanisms causing the bias-stress effect and an estimate of the expected lifetime of the transistor. It also provides a means to determine the operating region that minimizes the bias-stress effect.

To measure the bias-stress effect and no other degradation effects, we characterize pentacene OTFTs that have no measurable change by storage in nitrogen ambient. We demonstrate that the after-stress I-V characteristics can be accurately described by the initial I-V characteristics and a shift in applied gate voltage, ΔV. Based on this observation, we characterize the bias-stress effect with ΔV. We measure ΔV at different gate and drain bias (V_{SG} and V_{SD}) and stress times. Measurements with different V_{SD} at fixed V_{SG} stress show that ΔV decreases with increasing drain bias or current, indicating that gate field and channel carriers, not drain current, are responsible for the stress effect. We report that ΔV saturates independent of the V_{SG} stress. We propose a simple carrier-trapping rate model that results in a stretched-exponential equation that accurately describes the observed ΔV behavior with respect to stress times. The model suggests that the bias-stress effect is caused by trapping of the channel carriers. The bias-stress effect saturates due to a constant number of trap sites, unlike in a-Si:H TFTs, where the trap sites are continually created until there are no more channel carriers [3]. The saturation of the bias-stress effect independent of the V_{SG} stress is reported for the first time in organic transistors.

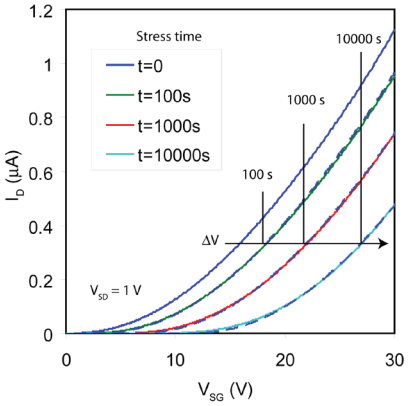

FIGURE 1: Transfer characteristics after bias stress at V_{SG} = 30 V, V_{SD} = 1 V at varying stress time, t. The dashed line shows the shifted transfer characteristics of the unstressed device (t = 0 s).

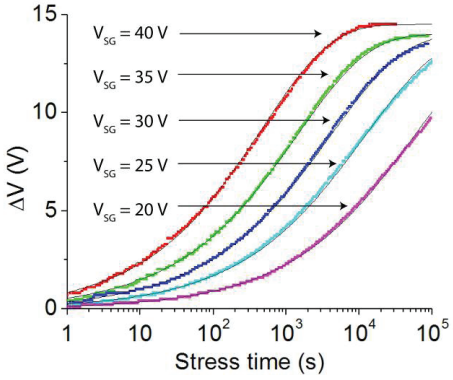

FIGURE 2: Measured stress time-dependence of the induced ΔV for different gate bias-stress conditions (colored dots) and the stretched-exponential fit made to the data (solid lines).

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Materials Reliability in GaN-based Devices

P. Makaram, J. A. del Alamo, T. Palacios, C. V. Thompson
Sponsorship: DURINT

GaN-based devices, traditionally used for light-emitting diodes [1], [2], are becoming very attractive for high-power, high-frequency applications for a variety of radar and communication applications [3]. Of particular interest are AlGaN/GaN-heterostructure-based high-electron-mobility transistors (HEMTs). Even though there has been intensive research done to improve these devices [4], their reliability is still a key issue and failure mechanisms are not well understood. The GaN films are typically in a high state of stress due to lattice and thermal mismatch. This state can lead to voiding and/or cracking that, in turn, leads to failure. Moreover, the piezoelectric properties of GaN couple with high electric fields to add to the complexity of the mechanical stress state. The goals of this project are to identify the material failure mechanisms for GaN-based devices, to develop reliability model to predict the lifetimes, and develop testing and lifetime projection methodologies.

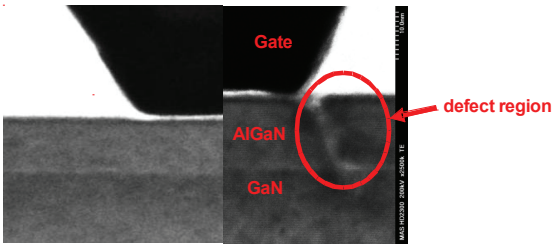

FIGURE 1: (left) A TEM image of a fresh device. (right) A TEM image of a degraded device [5].

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Effects of Active Atomic Sinks and Reservoirs on the Reliability of Cu/low-k Interconnects

F. L. Wei, C. S. Hau-Riege (AMD), A. P. Marathe (AMD), T. Chookajorn, C. V. Thompson
Sponsorship: Intel Corporation, AMD, SRC

Experiments using Cu/low-*k* interconnect tree structures have been used to characterize the rate and mechanisms of electromigration-induced voiding (Figure 1a) and extrusion (Figure 1b) [1], [2]. Kinetic parameters were extracted from resistance versus time data, giving $(Dz^*)_{0,eff} = 3.9 \times 10^{-10}$ m²/s and $z^* = 0.40 \pm 0.12$. Using these values, the evolution of stress in each of the interconnect tree segments could be calculated and correlated with the rate of void or extrusion growth and the failure times for all test configurations. It was demonstrated that segments that serve as atomic sinks and reservoirs for the failing segments affect the lifetime by modifying the conditions for stress-induced migration. Reservoirs can lead to increased lifetimes, while sinks can lead to reduced lifetimes. Quantitative predictions of the times required for failure for Cu/low-*k* interconnect trees as a function of the effective bulk elastic modulus of the interconnect system, *B*, are made. As the Young's modulus of the inter-level dielectric (ILD) films decreases, *B* decreases; additionally, the positive effects of reservoirs are diminished and the negative effects of sinks are amplified [1]. Analyses of extrusion-failure show that sparsely packed, intermediate-to-wide interconnect lines are most susceptible to electromigration-induced extrusion damage, and that extrusion failures are favored by ILDs with low stiffness, low elastic moduli, and thin liners. The latter are needed in future interconnect systems.

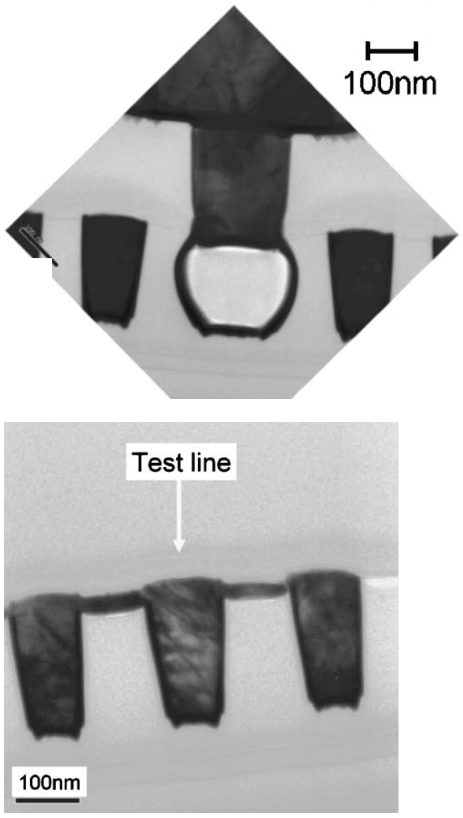

FIGURE 1: (a) Cross-sectional electron microscope image of the cathode end of a Cu/low-k interconnect for which electromigration-induced tensile stress led to void formation and growth and ultimately an open-circuit failure. (b) Cross-sectional electron microscope image of the anode end of a Cu/low-k interconnect for which electromigration-induced compressive stress led to extrusion of Cu at the Cu/capping-layer interface and ultimately short-circuit failure.

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