INTRODUCTION

Welcome to the 2009 Microsystems Technology Laboratories (MTL) Annual Report. This report summarizes the research from 115 faculty and senior research staff associated with the MTL. The report covers diverse research areas related to electronic device fabrication, integrated circuits and systems, photonics, and micro-electromechanical systems (MEMS), as well as molecular and nano-technologies. These investigators come from more than 38 different departments, labs, and centers across the Institute.

MTL is an interdepartmental laboratory at MIT with a mission to foster research and education in semiconductor process and device technology, and integrated circuits and systems design. MTL provides micro- and nano-fabrication and computer aided design (CAD) infrastructure to the entire campus. Last year, more than 550 researchers, primarily graduate students, conducted research using the MTL infrastructure. MTL also provides access to other educational /research institutes and the industrial communicty through its outreach program.

MTL's fabrication environment includes three clean rooms: the Class 10 Integrated Circuits Laboratory, the Class 100 Technology Research Laboratory, and the flexible Exploratory Materials Laboratory. The computational environment provides access to advanced electronic design automation (EDA) for device, circuit and system design. The fabrication and computation facilities of MTL are maintained and operated by approximately 20 full-time technical staff members.

MTL partners with industry through the Microsystems Industrial Group (MIG), who provide significant support, both financial and technical, for MTL's research and research infrastructure. This year, two new members, Qualcomm and Veeco, have joined the MIG. The members of the Industrial Advisory Board (one member from each of our MIG companies) provide guidance in shaping the vision of MTL. The current IAB can be found at the following website: http://mtlweb.mit.edu/mig/iab.html.

A number of committees set strategies and direction for the lab. The MTL Seminar Series Committee has put together an excellent seminar series open to the public. MTL's flagship event is the MTL Annual Research Conference (MARC) held annually. The most recent MARC was held on campus in January of 2009. The conference is run by MTL graduate students in collaboration with a steering committee chaired by Professor Joel Voldman. The conference has grown substantially over the past few years and is widely attended by industry, faculty, students and staff. MARC 2009 had more than 200 attendees. MTL also organized a highly successful workshop on next generation medical electronics (December 2008). We expect to significantly expand in the medical electronics area in the coming years. MTL Days at MIG companies, where MTL graduate students and faculty present leading-edge results to our industry partners, have also been popular.

Research conducted at MTL (as organized in the Annual Report) can be broadly classified into eight categories: Circuits & Systems, Electronic Devices. Energy, Materials, Medical Electronics, MEMS & BioMEMS, Nanotechnology, and Photonics. MTL has four affiliated industrial research centers with more focused interests: the Center for Integrated Circuits and Systems (CICS), the Intelligent Transportation Research Center (ITRC), MEMS@MIT, and the Center for Integrated Photonic Systems (CIPS).

MTL COMMITTEES, 2008-2009

Microsystems Industrial Group
Analog Devices
Applied Materials
Cadence, Inc.
IBM Corporation
Intel Corporation
National Semiconductor
NEC Corporation
Novellus Systems, Incorporated
Qualcomm, Inc.
Samsung
STMicroelectronics
TSMC
Texas Instruments, Inc.
Veeco Instruments

Directors
Anantha P. Chandrakasan, Director
Samuel C. Crooks, Associate Director, Finance
Jesus A. del Alamo, Associate Director, Computation & CAD
Vicky Diadiuk, Associate Director, Fabrication Operations
Judy L. Hoyt, Associate Director, Fabrication
Hae-Seung Lee, Associate Director, Industrial Relations & Publications

Policy Board
Anantha P. Chandrakasan, Chair
Dimitri A. Antoniadis
Akintunde I. Akinwande
Duane Boning
Samuel C. Crooks
Vicky Diadiuk
Judy L. Hoyt
Hae-Seung Lee

MARC 2009 Committee
Joel Voldman, Steering Committee Chair
Jing Kong, Faculty Advisor
Tayo Akinwande, Faculty Advisor
Samuel C. Crooks, Finance
Debroah Hodges-Pabon, Logistics
Mara Karapetian, Publications
Paul McGrath, Photography
Karthik Balakrishnan, Web Programming
Nicole DiLello, Program Committee Co-Chair
Ivan Nausieda, Program Committee Co-Chair

MTL Seminar Series Committee
Joel L. Dawson, Chair
Valerie DiNardo, Coordinator
Akintunde I. Akinwande
Dimitri A. Antoniadis
Jing Kong
Michael Perrott
Vladimir Stojanovic
Joel Voldman

Process Technology Committee
Vicky Diadiuk, Chair
Judy L. Hoyt, Associate Director, Fabrication
Pouya Hashemi,
Jeff Lang
Tomás Palacios
Kevin Ryu
Nader Shaar
Orit Shamir

Publications Committee
Mara Karapetian, Chair
Anantha P. Chandrakasan
Elizabeth Fox, Technical Editor
Hae-Seung Lee
Cheryl Slowik, Publishing Services Bureau Consultant

Social Committee
Debroah Hodges-Pabon, Chair
Nicole DiLello
Nigel Drego

PRINCIPAL INVESTIGATORS

Name	Research Interests	Office	Tel	E-mail
A. I. Akinwande	Micro- and Nano- structures for sensors & actuators and vacuum microelectronics. Devices for large area electronics and flat panel displays.	39-553a	617-258-7974	akinwand@mtl.mit.edu
D. A. Antoniadis	Fabrication, measurements and modeling of silicon- and germanium-based devices for high-speed and low-power integrated circuits.	39-427b	617-253-4693	daa@mtl.mit.edu
M. A. Baldo	Molecular electronics, integration of biological materials and conventional electronics, electrical and exciton transport in organic materials, energy transfer, metal-organic contacts, nanomechanical transistors.	13-3053	617-452-5132	baldo@mit.edu
K. K. Berggren	Superconductive nanodevice physics and applications; nanofabrication methods, processes, and tool-development for application to quantum computing and single-photon detection.	36-219	617-324-0272	berggren@mit.edu
S. N. Bhatia	Micro- and nano-technologies for tissue repair and regeneration. Applications in liver tissue engineering, cell-based BioMEMS, and nanobiotechnology.	E19-502d	617-324-0221	sbhatia@mit.edu
D. S. Boning	Design for manufacturability (DFM) of processes, devices, and integrated circuits. Characterization and modeling of variation in semiconductor and MEMS manufacturing, with emphasis on chemical-mechanical polishing (CMP), electroplating, plasma etch, and embossing processes.	38-435	617-253-0931	boning@mtl.mit.edu
V. M. Bove, Jr.	Sensing, display, user interface, and computation for consumer electronics applications, particularly self-organizing ecosystems of devices. Advanced data representations for multimedia.	E15-368B	617-253-0334	vmb@media.mit.edu
V. Bulović	Physical properties of organic and organic/inorganic nanocrystal composite thin films and structures; development of nanostructured electronic and optoelectronic devices.	13-3138	617-253-7012	bulovic@mit.edu
A. P. Chandrakasan	Design of digital integrated circuits and systems. Energy efficient implementation of signal processing, communication and medical systems. Circuit design with emerging technologies.	38-107	617-258-7619	anantha@mtl.mit.edu
L. Daniel	Parameterized model order reduction of linear and nonlinear dynamical systems; mixed-signal, RF and mm-wave circuit simulation and modeling for optimization; parasitic extraction and accelerated integral equation solvers; simulation and modeling of the human cardiovascular circulatory system.	36-849	617-253-2631	luca@mit.edu
J. L. Dawson	Design of RF and mixed-signal CMOS ICs for communications systems and medical applications.	39-527A	617-253-5281	jldawson@mtl.mit.edu
J. A. del Alamo	Microelectronics device technologies for gigahertz and gigabit-per-second communication systems: physics, modeling, technology and design. InGaAs as a post-CMOS semiconductor logic technology. Technology and pedagogy of online laboratories for engineering education.	39-567a	617-253-4764	alamo@mit.edu
C. G. Fonstad, Jr.	Compound semiconductor heterostructure devices and physics. Optoelectronics: laser diodes, photodiodes, quantum effect devices, and OEICs. Monolithic heterogeneous integration. Microscale thermophotovoltaics.	13-3050	617-253-4634	fonstad@mit.edu
S. Gradečak	Nano-electronics and photonics; correlation of structural, optical, electronic, and magnetic properties of semiconducting materials; inorganic nanowires, nanowire heterostructure and devices; III-V semiconductor epitaxial films and low-dimensional systems; development of advanced electron microscopy techniques.	13-5094	617-253-9896	gradecak@mit.edu
J. Han	Nanofluidic / Microfluidic technologies for advanced biomolecule analysis and sample preparation: novel nanofluidic phenomena, nanofluidic biomolecule separation and pre-concentration, Molecular transport in nano-confined space.	36-841	617-253-2290	jyhan@mit.edu

Name	Research Interests	Office	Tel	E-mail
J. L. Hoyt	Fabrication and device physics of silicon-based heterostructures and nanostructures. High mobility Si and Ge-channel MOSFETs, nanowire FETs, novel transistor structures, and silicon-germanium photodetectors for electronic/photonic integrated circuits.	39-427A	617-452-2873	jlhoyt@mtl.mit.edu
Q. Hu	Physics and applications of millimeter-wave, terahertz, and infrared devices.	36-465	617-253-1573	qhu@mit.edu
P. Jarillo-Herrero	Quantum electronic transport in novel low-dimensional systems such as graphene and carbon nanotubes. Specific areas include: graphene nanoribbons, superconducting graphene nanoelectronic devices, suspended graphene devices, and graphene-carbon nanotube junctions.	13-2017	617-253-3653	pjarillo@mit.edu
S.-G. Kim	Nanomanufacturing, carbon nanotube assembly, piezoelectric energy harvesting, PZT MEMS, MEMS by ink jet printing	1-310	617-452-2472	sangkim@mit.edu
L. C. Kimerling	Electronic, photonic, and magnetic materials; nanotechnology	13-4118	617-253-5383	lckim@mit.edu
L. A. Kolodziejski	Research in integrated photonic devices and optoelectronic components. Design and fabrication of photonic crystals and III-V semiconductor devices. Semiconductor materials growth and characterization.	36-287	617-253-6868	leskolo@mit.edu
J. Kong	Synthesis, characterization and applications of carbon-based nanomaterials (nanotubes and graphene) and inorganic nanowires.	13-3065	617-324-4068	jingkong@mit.edu
J. H. Lang	Analysis, design and control of electromechanical systems with application to traditional electromagnetic actuators, micron-scale actuators and sensors (MEMS), and flexible structures.	10-176	617-253-4687	lang@mit.edu
H.-S. Lee	Analog and mixed-signal integrated circuits, with a particular emphasis in data conversion circuits in scaled CMOS.	39-521	617-253-5174	hslee@mtl.mit.edu
C. Livermore	MicroElectroMechanical Systems (MEMS). Design and fabrication of high power microsystems, including pumps and MEMS components for lasers. Energy storage in carbon nanotube springs. Assembly of MEMS devices. Self-assembly techniques for nano- and micro-scale manufacturing.	3-449C	617-253-6761	livermor@mit.edu
S. R. Manalis	Microdevices for biomolecular and single cell analysis.	E15-422	617-253-5039	scottm@media.mit.edu
I. Masaki	VLSI architecture. Emphasis on interrelationship among applications, systems, algorithms, and chip architectures. Major application fields include intelligent transportation systems, video, and multimedia.	38-107	617-253-8532	imasaki@aol.com
T. Palacios	Design, fabrication and characterization of novel electronic devices in wide bandgap semiconductors; polarization and bandgap engineering; transistors for sub-mm wave power and digital applications; new ideas for power conversion and generation; interaction of biological systems with semiconductor materials and devices; nanowires and graphene –based transistors.	39-567B	617-324-2395	tpalacios@mit.edu
D. J. Perreault	Power electronics and energy conversion, Electronic circuit design and control. Applications to industrial, commercial, scientific, transportation, and biomedical systems.	10-039	617-258-6038	djperrea@mit.edu
R. J. Ram	Photonic devices for applications in communications, computing, and biological sensing with special emphasis on fiber-to-the-home, InP photonic integration, Silicon photonics and high speed interconnects, microscale bioreactors, and biomanufacturing.	36-491	617-253-4182	rajeev@mit.edu
C. A. Ross	Fabrication, properties and applications of magnetic and magnetooptical films, nanostructures and devices; self assembly, block copolymer lithography.	13-4005	617-258-0223	caross@mit.edu
R. Sarpeshkar	Biomedical systems, circuit modeling of biology, bio-inspired systems.	38-294	617-258-6599	rahuls@mit.edu

Name	Research Interests	Office	Tel	E-mail
M. L. Schattenburg	Advanced lithography, including x-ray, electron-beam, ion-beam, and optical. Nanotechnology and nanofabrication. Precision engineering and nano-accuracy dimensional metrology. Advanced interference lithography technology for high-accuracy patterning of general grating and grid patterns. Micro and nanometer fabrication technology applied to advanced astronomical and laboratory instrumentation. Silicon micromachined structures applied to high-precision optical assembly. X-ray optics and instrumentation.	37-487	617-253-3180	marks@space.mit.edu
M. A. Schmidt	Micromechanical systems (MEMS). Microfabrication technologies for integrated circuits, sensors, and actuators; design of micromechanical sensor and actuator systems; mechanical properties of microelectronic materials with emphasis on silicon wafer bonding technology; integrated microsensors, and microfluidic devices. Novel applications of MEMS and nanotechnologies to a variety of fields, including miniature gas turbines, miniature chemical reactors, miniature gas analyzers, microswitches, biological applications, and sensors monolithically integrated with electronics.	39-521	617-253-7817	schmidt@mtl.mit.edu
H. I. Smith	Co-director, NanoStructures Lab. Development of nanofabrication tools and techniques aimed at reaching molecular dimensions and sub-1nm positional accuracy; nanophotonics; templated self assembly.	36-225	617-253-6865	hismith@mit.edu
C. G. Sodini	Electronics and integrated circuit design and technology. More specifically, technology intensive integrated circuit and systems design, with application toward sensory interface electronics and wireless communication emphasizing analog signal processing and RF integrated circuits.	39-527B	617-253-4938	sodini@mtl.mit.edu
V. Stojanović	On-chip interconnects and high-speed off-chip interfaces (electrical, photonic). Circuit and interconnect design with novel devices (CNTs, NEM relays, Si-photonic). Modeling and analysis of noise and dynamics in circuits and systems. Application of optimization techniques to digital communications, analog and digital circuits. Digital communications and signal-processing architectures, clock generation and distribution, high-speed digital circuit design, VLSI and mixed-signal IC design.	38-260	617-324-4913	vlada@mit.edu
C. V. Thompson	Processing and property optimization for thin films and nanostructures for applications in electronic and electromechanical integrated device systems. Advanced, reliable integrated circuit interconnects.	13-5069	617-253-7652	cthomp@mit.edu
H. L. Tuller	Energy related materials, micro-fuel cells, solar cells, resonant and chemoresistive sensors, high K dielectrics, electro-optic and piezoelectric thin films, solid state ionics, thin film transistors, MEMS structures and devices.	13-3126	617-253-6890	tuller@mit.edu
J. Voldman	Microtechnology for basic and applied cell biology; Microsystems for stem cell biology; Electrostatics at the microscale, especially dielectrophoresis.	36-824	617-253-2094	voldman@mit.edu
E. N. Wang	Micro/nanoscale transport micro-/nanoscale transport phenomena, MEMS/NEMS design and sensing, optical diagnostics, numerical modeling, and surface nanoengineering for thermal management, energy conversion, and water desalination.	3-461B	617-324-3311	enwang@mit.edu
B. L. Wardle	Nano-engineered composites; nanocomposites; MEMS Power Devices and Energy Harvesting; Advanced Composite Materials and Systems; Structural Health Monitoring (SHM); Fracture, Fatigue and Damage Mechanics; Durability Modeling/Testing; Finite-Element Modeling; Structural Response and Testing; Buckling Mechanics	33-314	617-252-1539	wardle@mit.edu

Circuits & Systems

Test Circuits for Characterization of Process, Device, and Interconnect Variation

K. Balakrishnan, A. H. Chang, N. Drego, D. S. Boning
Sponsorship: SRC/FCRP IFC, SRC/FCRP C2S2, TSMC, Samsung Electronics

Due to the continuous and aggressive scaling of CMOS technology, the variability in parameters that are most critical in determining the quality and robustness of a device must be accurately characterized. For process- and device-level characterization, a test chip that characterizes contact plug resistance variability has been designed, fabricated, and measured. In addition, a test circuit has been designed to characterize layout-induced systematic variability in transistor saturation current.

One trend affecting device interconnect is the impact of contact resistance, which is becoming an increasingly larger component of the total resistance in a MOSFET. The characterization of contact resistance variability will allow for the generation of a compact model that incorporates sensitivities to various parameters into the determination of individual contact resistances. A test chip that can characterize the variability of resistance in contact plugs is implemented in a 90nm CMOS process; the chip contains over 40,000 devices under test. Figure 1 shows the distribution of normalized contact plug resistance across one die. These results are unique in measuring components of plug resistance within a transistor environment, as opposed to measurements using contact/via chains. Results show that the within-die resistance has a $\sigma/\mu \approx 4.6\%$ and the die-to-die resistance has a $\sigma/\mu \approx 4.4\%$. In addition, there is a clear systematic offset in the contact resistance between two regions of the chip, possibly caused by variability in the step-and-scan lithography process. The contact plug resistance is also a function of the distance from the contact to both the polysilicon gate and the edge of the diffusion region. Device simulations to further investigate this effect are ongoing.

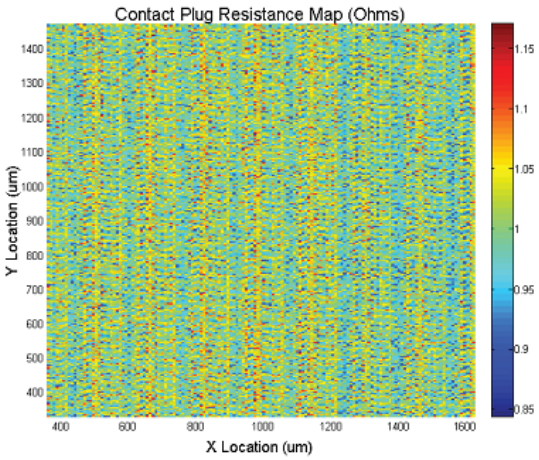


FIGURE 1: Normalized contact plug resistance map for a representative test chip.

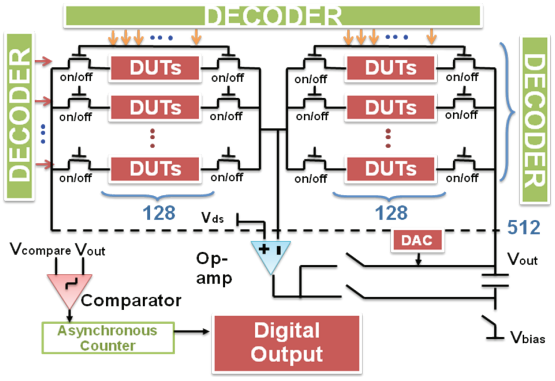


FIGURE 2: Hierarchical design of on-chip current measurement.

A test chip has also been designed to study layout-induced systematic variation in transistor behavior. Two pattern densities are chosen in our design: polysilicon density and shallow-trench isolation (STI) density. A test structure is designed to study these pattern density effects, as well as systematic spatial dependency between transistors. One goal is to decouple the impact of different variation sources on transistor characteristics and determine the farthest layout distance that should be taken into account when determining local transistor characteristics. More accurate transistor models based on surrounding layout details can then be built using our results.

The test structure is divided into six blocks, each with a different polysilicon density or STI density. A rapid change of pattern density between blocks is designed to emulate a step response for future modeling. The two pattern densities are chosen to reflect the introduction of a new process technology, such as strain engineering or rapid thermal annealing. The test structure is designed to have more than 260K devices under test (DUT). The test circuit is designed to enable on-chip current measurement with a high dynamic range analog-to-digital converter (ADC). The ADC, shown in Figure 2, has a dynamic range of over four orders of magnitude, to measure current from 50nA to 1mA. The test chip also implements a hierarchical design with a minimum amount of periphery circuitry around the DUTs, so most of the chip area is dedicated to the transistors under test.

Variation-Induced Energy Overhead Reduction in Multicore Processors

N. Drego, A. P. Chandrakasan, D. S. Boning
Sponsorship: SRC/FCRP C2S2

In modern process technologies it is clear that performance, power/energy, cost and variation are intricately linked to each other. As system architects value core homogeneity in multicore processors, the burden of finding energy-efficient variation mitigation solutions increases. Balancing other constraints, such as area overhead and design complexity, must also play into any mitigation technique. Evaluation of some of the more common mitigation schemes, in the context of these constraints, reveals a need for an energy-efficient technique capable of guaranteeing both performance and yield constraints while introducing minimal overhead.

Introducing additional system voltages (fewer than one per core) provides a compromise between excess design/area overhead and energy efficiency while maximizing performance for multicore systems with N cores. An analytic framework capable of optimal voltage selection, to minimize energy and reduce the energy overhead required to mitigate variation, is developed and analyzed in-depth. Specifically, a simple, efficient Minimum Energy Voltage Selection (MEVS) algorithm to select optimal voltages forms the basis of this framework, allowing for multiple types of analysis. Though the optimization problem is not convex in general and simplifying approximations are used, the algorithm is nevertheless able to find optimal (for N = 2) or near optimal solutions. Furthermore, the behavior of the algorithm is mathematically bounded and shown to perform according to the bounds.

Using a custom simulation methodology and the MEVS algorithm, a core designed specifically for multicore contexts is simulated to observe the magnitude of performance variation and the impact of introducing additional voltages to a massively parallel 1K-core processor. Analysis shows that a single additional power-supply voltage provides the greatest incremental impact, with 59-75% reduction in the variation-induced energy overhead and 6-16% total energy reduction, as seen in Figure 1. The desired yield constraint also has a significant impact on energy reduction: though counterintuitive, turning off a small fraction of the thousand cores can provide a positive trade-off between performance and energy, as depicted in Figure 2, with multiple system voltages further improving this trade-off. Lastly, when voltage regulator efficiencies are properly accounted for, using only a few system voltages ($2 \leq N \leq 10$) provides greater energy reduction than supplying each core with its own voltage.

REFERENCES

[1] N. Drego, "Characterization and Mitigation of Process Variation in Digital Circuits and Systems," PhD Thesis, Massachusetts Institute of Technology, Cambridge, 2009.

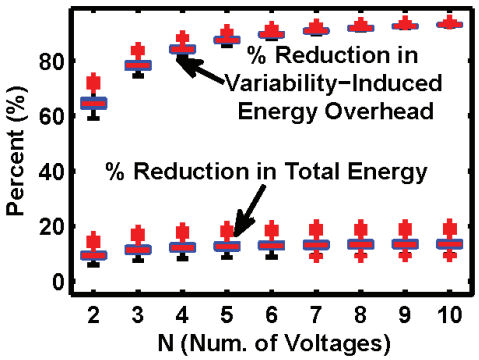


FIGURE 1: Energy reduction by adding voltages to a multicore system. A single additional power-supply voltage provides the most incremental benefit in such systems, with asymptotic gains in energy reduction for additional power-supply voltages.

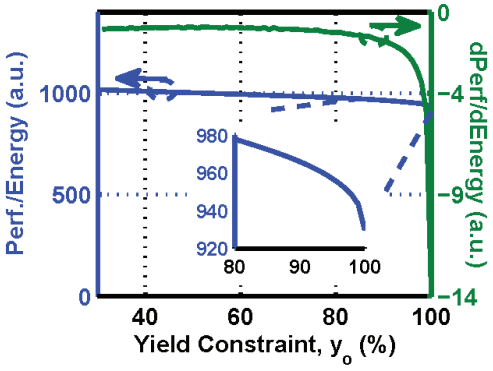


FIGURE 2: Joint performance/energy metric as a function of yield. Due to the exponential tails of the performance distributions, turning off the last 5-15% of poor-performing cores leads to a positive trade-off. The incremental change in performance for a given increment of energy severely degrades at the yield constraint is increased beyond 85% (green plot, right axis).

45nm Direct-battery DC-DC Converter for Mobile Applications

S. Bandyopadhyay, Y. K. Ramadass, A. P. Chandrakasan
Sponsorship: MTL, MIT

Mobile applications use lithium-ion batteries as the power supply. With the aggressive downscaling of transistors, it is becoming increasingly difficult to interface the low-voltage digital core with the battery, which may be at voltages as high as 5.5V. The interfacing can be done by a DC-DC converter, which may be a separate IC designed on an older generation process capable of handling high voltages. In this work, a buck converter has been designed in a 45-nm process so that it can be integrated with the 45-nm digital core on the same die. This design gives us cost and performance advantages for a single chip solution. This work presents a wide load range DC-DC converter that gives more than 80% efficiency from 10μA to 100mA of load currents. This efficiency is accomplished by using both the PFM and PWM control schemes [1], [2]. Further, the converter requires Switched Capacitor (SC) converters [3] to generate the voltages for stacking and for the control circuitry. Figure 1 shows the block diagram of the cellular system with the battery and the direct-battery DC-DC converter.

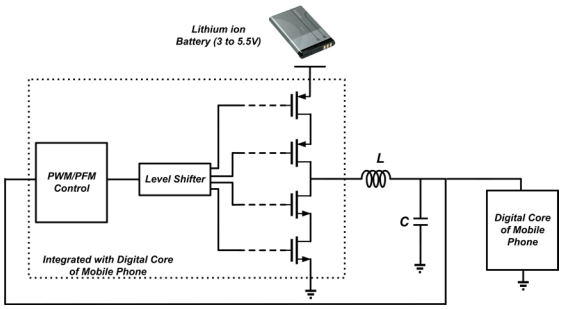


FIGURE 1: Block Diagram showing the Lithium ion battery with DC-DC converter and the digital core of mobile phone at 45nm.

REFERENCES

[1] J. Xiao et.al "A 4-µA Quiescent-Current Dual-Mode Digitally Controlled Buck Converter IC for Cellular Phone Applications," *IEEE Journal of Solid State Circuits*, Vol. 39, No. 12, December 2004

[2] Y. K. Ramadass and A.P. Chandrakasan, "Minimum Energy Tracking Loop with Embedded DC-DC Converter Delivering Voltages down to 250mV in 65nm CMOS," *International Solid State Circuits Conference*, February 2007, San Francisco.

[3] J. Kwong, Y. K. Ramadass, N. Verma, and A.P. Chandrakasan, "A 65nm Sub-Vt Microcontroller With Integrated SRAM and Switched Capacitor DC-DC Converter," *IEEE Journal of Solid State Circuits*, Vol.44 No.1, Jan 2009.

A Low-power AES Engine with Resistance to Differential Power Analysis Side-channel Attacks

H. W. Chung, A. P. Chandrakasan

Security concerns for transmission or storage of data by battery-operated wireless systems require the development of an energy-efficient encryption coprocessor. However, even with the security ICs, core information can be discovered by attackers since the ICs are vulnerable to side-channel attacks. Among all the side-channel attacks, differential power analysis (DPA) attack is effective in finding a secret key. Measuring the current from power supply and then performing statistical analysis of the measured power traces can lead to discovery of the secret key. Therefore, development of an energy-efficient encryption processor that is immune to differential power analysis attack is required for the secure transmission and storage of the data in battery-operated security ICs.

The Advanced Encryption Standard algorithm [1] is a block cipher that converts 128-bit plaintext to ciphertext with selectable key lengths (128, 192, or 256 bits). The algorithm is organized as a repeated "round transformation" that includes four types of sub-operations, i.e., "S-Box," "ShiftRows," "MixColumns," and "AddRoundKey"(Figure 1). The DPA attack occurs at the transition of the RB registers (Figure 1). Correlation between the modeled power trace based on a guessed secret key and the measured transition power of the RB registers can give enough information to find out a secret key.

A novel architecture is suggested to guarantee DPA-immunity. First, S-Box is designed with decoder-encoder block [2], and then the RB register is moved between the decoder and encoder of S-Box so that the number of 0 to 1 transitions is the same for all the possible encryption data. With this design, attackers cannot get any information about the secret key since there is no data-dependency in the measured current trace of the RB registers. Area overhead exists area for this architecture, but the power overhead is not significant with proper clock-gating of the RB registers. Moreover, maximizing parallel operation of data can lower the supply voltage into the sub-threshold region with satisfying the performance specification. Sub-threshold operation is beneficial not only for energy-efficient operation, but also for improvement of DPA-immunity.

REFERENCES

[1] NIST, "Federal Information Processing Standards PUB 197 Advanced Encryption Standard" (2001, Nov.). [Online]. Available: http://www.nist.go/aes/

[2] G. Bertoni, M. Macchetti, and L. Negri, "Power-Efficient ASIC Synthesis of Cryptographic Sboxes," *ACM Great Lake Symposium on VLSI*, pp. 277-281, April. 2004

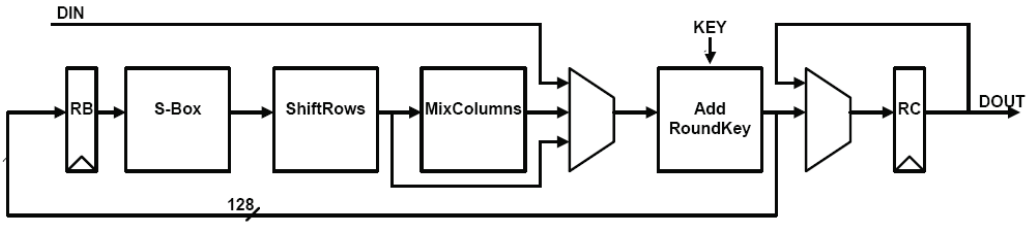


FIGURE 1: Architecture of AES core: DPA attack mainly occurs at the transition time of the RB registers.

A Pulsed UWB Receiver SoC for Insect Motion Control

D. C. Daly, P. P. Mercier, M. Bhardwaj, H. Liang, A. P. Chandrakasan
Sponsorship: DARPA, NSERC

For decades, scientists and engineers have been fascinated by cybernetic organisms, or cyborgs, that fuse artificial and natural systems. Cyborgs enable the harnessing of biological systems that have been honed by evolutionary forces over millennia to achieve astounding feats. Male moths can detect a single pheromone molecule, a sensitivity of roughly 10^{-21} grams. Thus, cyborgs can perform tasks at scales and efficiencies that would ordinarily seem incomprehensible. Semiconductor technology is central to realizing this vision because it offers powerful processing and communication capabilities as well as low weight, small size, and deterministic control. An emerging cyborg application is moth flight control, where electronics and MEMS devices are placed on and within a moth to control flight direction. To receive commands on the moth, a lightweight, low-power and low-volume receiver is required. Figure 1 presents an overview of the moth flight control system being developed in collaboration with other scientists and researchers at MIT, the University of Washington, and the University of Arizona.

A critical component of the hybrid-insect system is the wireless communication link, which provides flight control commands to the moth. Pulsed ultra-wideband (UWB) wireless signaling is employed as UWB radios can achieve highly integrated, energy-efficient operation in nanometer CMOS processes [1]-[3]. Power, weight and volume are all highly constrained, necessitating a highly integrated solution with minimal off-chip components. Data is transmitted by PPM modulation in one of three 500-MHz channels in the 3-to-5-GHz band. Figure 2 presents a block-diagram of the wireless receiver system-on-chip. The non-coherent receiver amplifies, squares, and integrates received pulses to measure the amount of energy received in a given time period. A differential, inverter based front end is employed to reduce current consumption while allowing for a single 1V core power supply. The highly duty cycled RX requires 0.5-to-1.4nJ/bit and achieves a sensitivity of -76dBm at a data rate of 16 Mb/s (10^{-3} BER). The moth stimulator generates a multi-channel, digital, pulse-width modulated signal to control flight direction. The radio has been integrated on a miniature, 1g PCB; and preliminary flight control in a wind tunnel has been demonstrated.

REFERENCES

[1] P. P. Mercier, D. C. Daly, and A. P. Chandrakasan, "A 19pJ/pulse UWB Transmitter with Dual Capacitively-Coupled Digital Power Amplifiers," *IEEE Radio Frequency Integrated Circuits Symposium*, pp. 47-50, June 2008.

[1] P. P. Mercier, M. Bhardwaj, D. C. Daly, A. P. Chandrakasan, "A 0.55V 16Mb/s 1.6mW Non-Coherent IR-UWB Digital Baseband with ±1ns Synchronization Accuracy," *IEEE International Solid-State Circuits Conference (ISSCC)*, pp. 252-253, Feb. 2009.

[2] D. C. Daly, P. P. Mercier, M. Bhardwaj, A. L. Stone, J. Voldman, R. B. Levine, J. G. Hildebrand, A. P. Chandrakasan, "A Pulsed UWB Receiver SoC for Insect Motion Control," *IEEE International Solid-State Circuits Conference (ISSCC)*, pp. 200-201, Feb. 2009.

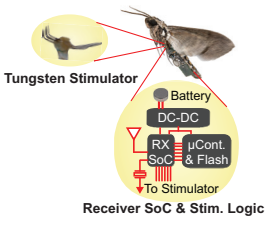


FIGURE 1: Overview of hybrid-insect flight control system.

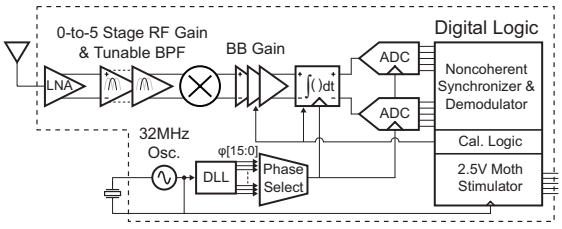


FIGURE 2: Block diagram of the wireless receiver SoC.

A Low-voltage, Fault-tolerant Microprocessor

N. Ickes, Y. Koken, F. Pappalardo (STMicroelectronics), A. P. Chandrakasan
Sponsorship: STMicroelectronics

Digital logic circuits are most energy-efficient when operated at very low (near subthreshold) voltages. However, many severely energy-constrained applications (e.g., implanted medical devices) also require high reliability, and the rate of radiation-induced soft-errors increases significantly at low voltages [1]. Existing techniques for improving soft-error resilience come with significant power overhead. The purpose of this project is to investigate error detection and correction mechanisms, for both memory and logic, which are specifically optimized for micropower, low-voltage systems.

Soft error events affect both combinational and sequential logic gates, as shown in Figure 1. Due to the necessarily tight power supply voltage margins at low voltage, power supply droop can also generate errors by causing signals to arrive late. Flip-flop and latch designs capable of detecting these errors [2], [3] have been previously demonstrated by others. However, their work has focused on high-performance processors with significant speculative state, so that errors can be recovered from simply by flushing speculative instructions from the pipeline. Micro-power processors have little or no speculative state, so we are exploring alternative error recovery mechanisms.

SRAMs make up the majority of the area of most microprocessor chips and must be continuously powered for data retention. Designing SRAMs for low voltage operation is therefore particularly important. However, scaling down power supply voltage not only increases susceptibility to radiation-induced soft errors but also degrades bit-cell stability due to device variation effects. Simple SECDED Hamming codes are quite effective at recovering from radiation-induced errors. We are exploring the use of higher-order BCH codes capable of correcting multiple bits per word, in order to address both radiation and bitcell variation induced errors (Figure 2). In particular, we are looking at how error-correcting capability might be efficiently scaled with the operating voltage.

As a test vehicle for these techniques, we are modifying an existing 32b microcontroller for operation at 0.5V in 90nm CMOS. In addition to adding error detection and correction logic, we are exploring the design of miniature instruction and data caches to both improve performance at very low voltages, and to reduce memory access energy.

REFERENCES

[1] T. Heijmen, P. Roche, G. Gasiot, K. R. Forbes and D. Giot, "A Comprehensive Study on the Soft-Error Rate of Flip-Flops From 90-nm Production Libraries," *Device and Materials Reliability, IEEE Transactions on,* vol. 7, pp. 84-96, 2007.

[2] S. Das, C. Tokunaga, S. Pant, W. Ma, S. Kalaiselvan, K. Lai, D. M. Bull and D. T. Blaauw, "RazorII: In Situ Error Detection and Correction for PVT and SER Tolerance," *Solid-State Circuits, IEEE Journal of,* vol. 44, pp. 32-48, 2009.

[3] K. A. Bowman, J. W. Tschanz, Nam Sung Kim, J. C. Lee, C. B. Wilkerson, S. L. Lu, T. Karnik and V. K. De, "Energy-Efficient and Metastability-Immune Resilient Circuits for Dynamic Variation Tolerance," *Solid-State Circuits, IEEE Journal of,* vol. 44, pp. 49-63, 2009.

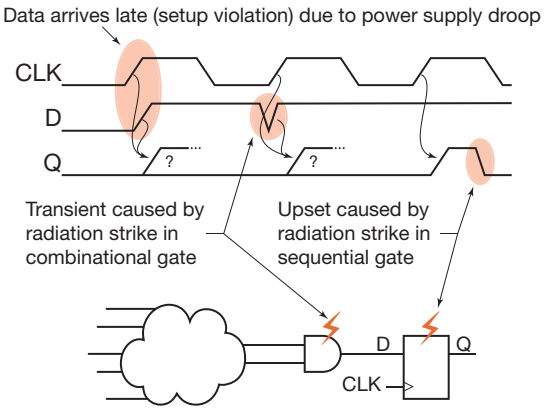


FIGURE 1: Soft error mechanisms in logic: delay violations, transients in combinational logic, and upsets in sequential gates.

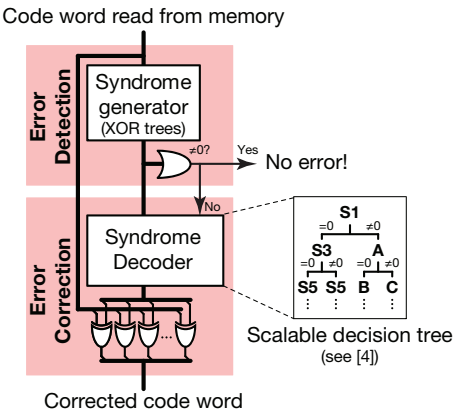


FIGURE 2: BCH decoding, showing the separate phases of error detection and correction.

Wearable Medical Monitoring Platform

J. Kwong, P. Mercier, M. Yip, A. P. Chandrakasan

Sponsorship: Texas Instruments, DARPA, SRC/FCRP C2S2

Advances in mobile electronics are fueling new possibilities in medical monitoring in which sophisticated, wearable devices can monitor a subject's vital signs. As illustrated in Figure 1, these signals can be securely transmitted over the internet via a local relay (often a cell phone or PDA) for preventative medicine, diagnostics, or emergency monitoring purposes. In these applications, comfort and convenience are important considerations, motivating a high level of integration to achieve small form factors and long operating lifetimes from a small battery or scavenged energy. Fortunately, the low rates of biological signals, which are typically on the order of tens to hundreds of Hz, make basic monitoring applications amenable to low-power processing [1], [2]. To support the wide range of signals, sensors, and algorithms, we propose a reconfigurable and energy-efficient platform for medical monitoring.

A block diagram of the platform is shown in Figure 2. The system requires a flexible sensor front-end and ADC that can interface with different types of sensors. The sensor front-end must have adjustable gain, bandwidth, and noise settings, as signals from different sensors can vary by several orders of magnitude in amplitude and frequency. The ADC should have configurable resolution from 8 to 12 bits to enable a variety of applications. A processor retrieves the digitized data from the ADC and performs local processing tasks specified in software. To save energy, the processor can operate at a low voltage and frequency when executing simple algorithms, but it maintains flexibility by elevating its voltage when high performance is needed. The architecture includes hardware accelerators to speed up computations. When not in use, each accelerator can be powered off to reduce idle leakage. To further save energy, local sensor nodes transmit processed data only to the local relay, instead of directly to the cellular network. The short transmission distance (1-2m) and inherently low data rates (1-10kbps) promote the design of highly-digital, energy-efficient communication circuits involving wired clothing networks [3] and/or wireless ultra-wideband [4]. A high-powered radio, as typically found in a PDA, can then consolidate sensor node data and transmit them over the cellular network to the internet for monitoring purposes.

REFERENCES

[1] A. P. Chandrakasan, N. Verma, D.C. Daly, "Ultralow-Power Electronics for Biomedical Applications," *Annual Review of Biomedical Engineering*, vol. 10, pp. 247-274, August 2008.

[2] A.C.-W. Wong, D. McDonagh, G. Kathiresan, et al., "A 1V, Micropower System-On-Chip for Vital-Sign Monitoring in Wireless Body Sensor Networks," *IEEE International Solid-State Circuits Conference*, February 2008, pp. 138-139.

[3] S. Lee, J. Yoo, and H-J. Yoo, "A Healthcare Monitoring System with Wireless Woven Inductor Channels for Body Sensor Network," *IEEE International Workshop on Wearable and Implantable Body Sensor Networks*, June 2008.

[4] P.P. Mercier, D.C. Daly, and A.P. Chandrakasan, "A 19pJ/pulse UWB Transmitter with Dual Capacitively-Coupled Digital Power Amplifiers," *IEEE Radio Frequency Integrated Circuits (RFIC) Symposium*, June 2008, pp. 47-50.

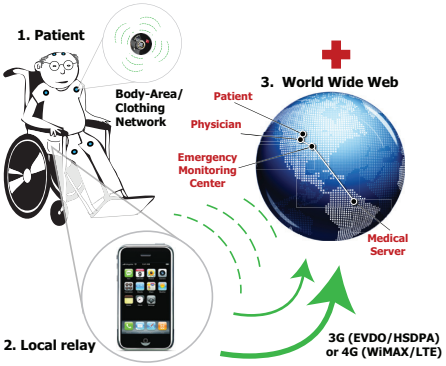


FIGURE 1: The vision of connected health care enabled by the wearable medical monitoring platform, a local relay and the World Wide Web.

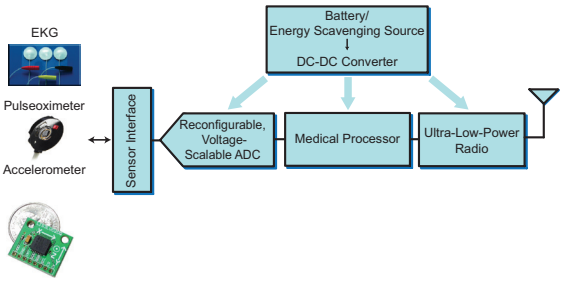


FIGURE 2: Block diagram of the wearable medical monitoring platform.

A Non-coherent Pulsed-UWB Digital Baseband Employing Quadratic Correlation

P. P. Mercier, M. Bhardwaj, D. C. Daly, A. P. Chandrakasan
Sponsorship: DARPA

Pulsed-ultra-wide-band (UWB) radios are finding increasing use in low-data-rate sensing applications, in part because they can be easily duty-cycled to achieve extreme energy efficiency. Within pulsed radios, non-coherent RF front-ends that use simple square-and-integrate samplers offer significant energy-per-bit savings over their coherent counterparts [1], [2]. However, such samplers lose phase information and accumulate squared noise over the integration period. While this loss increases the SNR required to relay a bit reliably, the greater challenge is achieving signal synchronization. Telemetry applications often have small payloads (10-100 bits) where synchronization time dominates. Furthermore, synchronization performance is being continually pushed to enable positioning capability. Hence, the ultimate advantage of non-coherent receivers relies on their ability to synchronize efficiently.

The proposed UWB digital baseband, whose top-level block diagram is shown in Figure 1, reduces synchronization overhead without any increase in RF front-end power or complexity using modified synchronization codes and quadratic correlators (QCORRs) in place of matched filters [3]. These features result in synchronization times that are 11x shorter than repetition codes, or, equivalently, require 10dB lower SNR than repetition codes, as shown in Figure 2. To further reduce energy and decrease synchronization latency, the baseband is highly parallelized, and operates down to a supply voltage as low as 0.55V. Implemented in 90nm CMOS, the baseband occupies an area of 2.55mm^2 and consumes an average power of 1.6mW during a typical preamble.

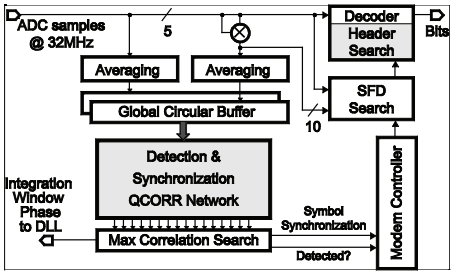


FIGURE 1: A top-level block diagram of the fabricated UWB modem.

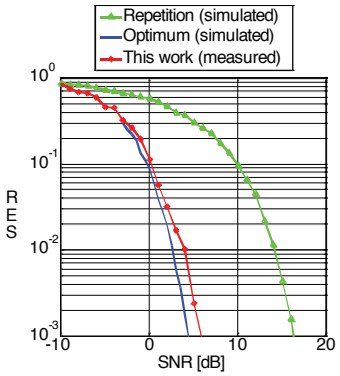


FIGURE 2: Synchronization error rate (SER) curves for the proposed baseband plotted with a simulated repetition-code receiver and an ideal maximum-likelihood receiver.

REFERENCES

[1] F.S. Lee, and A.P. Chandrakasan, "A 2.5nJ/b 0.65V 3-to-5GHz Subbanded UWB Receiver in 90nm CMOS," *IEEE ISSCC Dig. Tech. Papers*, pp. 116-117, Feb. 2007.

[2] D.C. Daly, P. P. Mercier, M. Bhardwaj, A. L. Stone, J. Voldman, R. B. Levine, J. G. Hildebrand, A. P. Chandrakasan, "A Pulsed UWB Receiver SoC for Insect Motion Control," *IEEE ISSCC Dig. Tech. Papers*, pp. 200-201, February 2009.

[3] P. P. Mercier, M. Bhardwaj, D. C. Daly, and A. P. Chandrakasan, " A 0.55V 16Mb/s 1.6mW Non-Coherent IR-UWB Digital Baseband with ±1ns Synchronization Accuracy," *IEEE ISSCC Dig. Tech. Papers*, pp. 252-253, Feb. 2009.

Statistical SRAM Optimization

M. Qazi, A. P. Chandrakasan
Sponsorship: SRC/FCRP C2S2

Process variation in deep-submicron technologies is especially pronounced for embedded SRAM, which must meet demands for higher density and higher performance at increased levels of integration. The very low failure probabilities required of the highly repeated memory cells must be predicted—both in terms of functionality and performance. To address these issues, we have developed a novel statistical simulation methodology for bitcell stability. Next, we extend this algorithm with new circuit insight into evaluating the worst-case performance of the SRAM critical path. The overall goal is to provide a comprehensive and efficient statistical design methodology of embedded memory from memory cell to block-level architecture.

We have developed and reported a novel importance sampling via norm minimization algorithm that achieves up to 10,000x speedup over conventional Monte Carlo simulation for very low failure probabilities [1]. We are also working on a statistical simulation tool flow that evaluates worst-case performance of SRAM critical paths.

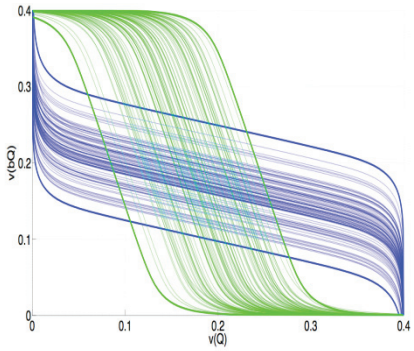


FIGURE 1: The SRAM memory cell exhibits a significant amount of variation as the supply voltage is reduced. Shown here is the variation under the retention condition of 32nm SRAM at 400mV supply for predictive technology models [2].

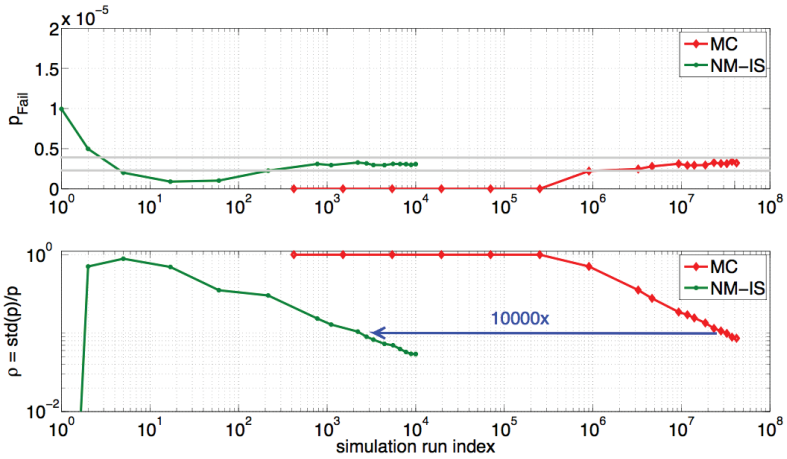


FIGURE 2: The top plot shows the comparison of the retention failure as evaluated by Monte Carlo simulation and the Norm Minimization Importance Sampling algorithm. 10,000X fewer runs are required with the sped-up algorithm for the same level of confidence as depicted in the lower plot.

REFERENCES

[1] L. Dolecek, M. Qazi, D. Shah and A. Chandrakasan, "Breaking the simulation barrier: SRAM evaluation through norm minimization," in *IEEE/ACM International Conference on Computer-Aided Design,* 2008, pp. 322-329.

[2] W. Zhao and Y. Cao, "New generation of predictive technology model for sub-45nm design exploration," *IEEE Transactions on Electron Devices,* vol. 53, pp. 2816-2823, 2006.

An Efficient Piezoelectric Energy-harvesting Interface Circuit

Y. K. Ramadass, A. P. Chandrakasan
Sponsorship: DARPA

Energy harvesting is an emerging technology with applications to handheld, portable, and implantable electronics. Harvesting ambient vibration energy through piezoelectric (PE) means is a popular energy-harvesting technique that can potentially supply 10's-100's of μW of available power [1]. One of the limitations of existing PE-harvesters is in their interface circuitry. Commonly used full-bridge rectifiers and voltage doublers [2] severely limit the electrical power extractable from a PE-harvesting element. Further, the power consumed in the control circuits of these harvesters reduces the amount of usable electrical power. This work presents a bias-flip rectifier that can improve upon the power extraction capability of existing full-bridge rectifiers by greater than 4X. An efficient control circuit with embedded DC-DC converters that can share their filter inductor with the bias-flip rectifier, thereby reducing the volume and component count of the overall solution, is demonstrated.

Figure 1 shows a conventional full-bridge rectifier circuit together with the implemented bias-flip rectifier circuit. The main limitation of the full-bridge rectifier is that, even when ideal diodes are considered, most of the current available from the harvester does not go into charging the output capacitor CRECT at high values of VRECT. The shaded portion of the current waveform in Figure 1 shows the time spent in charging or discharging CP every half-cycle. This loss in charge limits the amount of electrical power that can be extracted using the full-bridge rectifier. The bias-flip rectifier consists of an inductor LSHARE that is connected in parallel with the PE-harvester. When switches M1 and M2 of the bias-flip rectifier are turned ON, the inductor helps in flipping the voltage VBF across CP. After the switches close, the PE current IP needs to supply a smaller amount of charge to CP to bring it up to ±VRECT. This reduction in charge lost significantly improves the amount of power extractable from the harvester. The inductor used in the rectifier is shared efficiently with other DC-DC converters in the system. The entire chip was fabricated in a 0.35-μm CMOS process [3]. Figure 2 shows the measured power obtained at the output of the rectifier for the different rectifier scenarios with off-chip diodes. The effectiveness of the bias-flip rectifier improves as the inductance is increased. An 820μH inductor provides a 4.2X improvement in power extracted compared to the full-bridge rectifier. This power improvement increases to above 7X when on-chip diodes are used. The DC-DC converters employed in the system achieve greater than 85% efficiency with shared inductors, in the micro-watt power levels output by the piezoelectric energy- harvester.

REFERENCES

[1] S. Roundy, P.K. Wright and J. Rabaey, Energy Scavenging for Wireless Sensor Networks with Special Focus on Vibrations, Kluwer Academic Press, 2003.

[2] T. T. Le et al., "Piezoelectric Micro-Power Generation Interface Circuits," *IEEE J. Solid-State Circuits*, pp. 1411-1420, June 2006.

[3] Y.K. Ramadass and A. Chandrakasan, "An Efficient Piezoelectric Energy Harvesting Interface Circuit Using a Bias-Flip Rectifier and Shared Inductor," *IEEE Int. Solid-State Circuits Conference*, pp. 296-297, Feb. 2009.

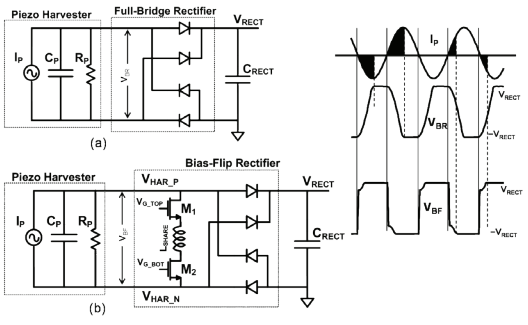


FIGURE 1: (a) Conventional full-bridge rectifier, (b) bias-flip rectifier. The right-hand side shows simulated input current and voltage waveforms for the different scenarios. The shaded portions of the current waveforms depict the amount of charge not delivered to the output capacitor C_{RECT}.

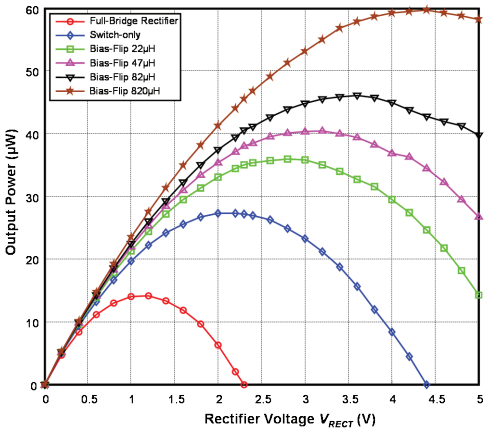


FIGURE 2: The measured electrical power output by the piezoelectric-energy-harvester as a function of the rectifier output voltage (V_{RECT}). The optimal value of V_{RECT} for maximal power transfer increases with the switch-only and bias-flip rectifier schemes.

Statistical Static Timing Analysis for Sub-0.5V Operation

R. Rithe, S. Chou, D. Buss, A. P. Chandrakasan

Statistical process variations have long been an important design issue. Until recently, process variations have been assumed to be global [1], [2]. With transistor geometries shrinking below 65nm, it is no longer valid to assume that transistor parameters are constant across a die because there are "local" or intra-die variations [1], [2]. The traditional corner-based analysis is not enough to correctly determine the performance of the integrated circuits. Despite the importance of SSTA for accurate performance analysis, the biggest challenge is to develop the statistical models and develop a computationally efficient algorithm for performing SSTA. At low voltage (V_{DD} ~0.5V), circuit delay is a non-linear function of the transistor random variables. This trait complicates the statistical analysis because the circuit delay is no longer Gaussian [3]. This work is aimed at developing such an algorithm that can perform accurate path-based SSTA in the regime where delay is a highly non-linear function of the random variables.

In this work, the dimensionality of the problem is significantly reduced by mapping the non-Gaussian delay PDF on to a Gaussian parameter through a non-linear function called Cell/Arc Delay Function. The novel concept of Operating Point (the point where joint PDF of the cell delays in a timing path attains the maxima) is introduced which allows us to determine the most probable combination of cell delays that would result into the *3-Sigma* delay (or in general *f-Sigma* delay) of the Timing Path (TP) without the need to compute the entire delay PDF.

Cell characterization is computationally efficient because we do not calculate entire delay PDF. We calculate the minimum information required to combine cell delay statistics into Timing Path delay. No expensive Monte Carlo (MC) simulation is required during characterization or timing closure. Our SSTA analysis runs in linear time with respect to number of stages, whereas MC run time increases exponentially. The concept of Operating Point that has been introduced here greatly simplifies computations despite non-linearities without sacrificing accuracy. The approach is tested on a library implemented using commercial scaled 32nm technology. We have been able to achieve accuracy of within 5% compared to MC simulation with more than 120 times improvement in run-time. The approach can be extended to perform hold-time analysis and can also be used to determine the design strategy to minimize stochastic delays.

REFERENCES

[1] A. Agarwal, D. Blaauw and V. Zolotov, "Statistical timing analysis for intra-die process variations with spatial correlations," *Computer Aided Design, 2003. ICCAD-2003. International Conference on*, pp. 900-907, 2003.

[2] B. Liu, "Gate Level Statistical Simulation Based on Parameterized Models for Process and Signal Variations," *Quality Electronic Design, 2007. ISQED '07. 8th International Symposium on*, pp. 257-262, 2007.

[3] L. Cheng, J. Xiong and L. He, "Non-Linear Statistical Static Timing Analysis for Non-Gaussian Variation Sources," *Design Automation Conference, 2007. DAC '07. 44th ACM/IEEE*, pp. 250-255, 2007.

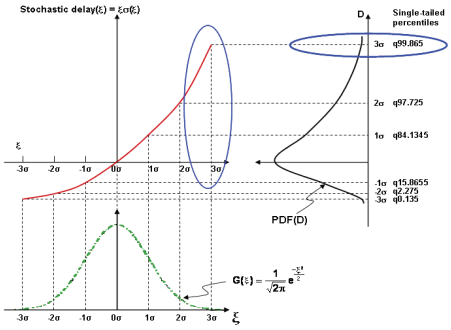


FIGURE 1: Mapping of non-Gaussian delay PDF on to a Gaussian parameter ξ through the non-linear Cell/Arc Delay Function. The CADF is stored as the output of cell characterization.

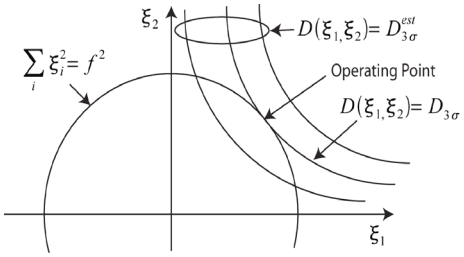


FIGURE 2: The operating point for a 2-stage TP that gives f-Sigma delay at the output. The operating point allows us to easily determine the stochastic delay imparted by each cell by referring to the stored CADFs without having to look into the transistor RVs.

An 8T Reconfigurable SRAM in 65-nm CMOS Achieving 0.25-1.2V Operating Voltage Range

M. E. Sinangil, A. P. Chandrakasan
Sponsorship: DARPA

In modern integrated circuits (ICs), the trend of integrating more on-chip memories on a die has led SRAMs to account for a large fraction of total chip area as well as the total chip energy. Hence, applying energy-saving schemes such as dynamic voltage scalability (DVS) to SRAMs is an important research area. However, optimizing circuit operation over a large voltage range is not trivial due to conflicting trade-offs of low-voltage (moderate and weak inversion) and high-voltage (strong inversion) transistor characteristics. Specifically, low-voltage operation requires various assist circuits for functionality, which might severely impact high-voltage performance. Previous work in literature focused on either sub-threshold operation [1] or DVS in only the above-threshold regime [2]. In this work [3], SRAM design for a very large voltage range including both sub-threshold and above-threshold regions is investigated. Reconfigurable circuit assists are proposed as a solution to the problem of optimizing circuits over a large voltage range with minimum performance penalty and power overhead.

A test chip is implemented in 65-nm low-power CMOS process to demonstrate an ultra-dynamic voltage scalable (U-DVS) SRAM. The 64-kbit memory array is structured in 8 blocks, each with 64 rows and 128 columns of memory cells. Figure 1 shows the die photo of the test chip. Read and write functionality is achieved from 1.2V down to 0.25V at 200MHz and 20kHz, respectively, as shown in Figure 2. Over this voltage range, leakage power scales down by more then 50x. The minimum energy point of this work lies close to 0.4V at less than 0.1pJ/bit/access.

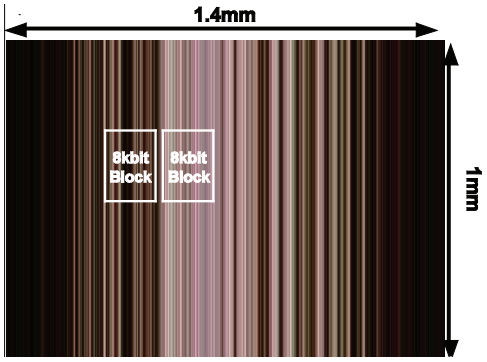


FIGURE 1: Die photo of the 64kbit SRAM test chip fabricated in 65-nm CMOS process. Die area is 1mm x 1.4mm.

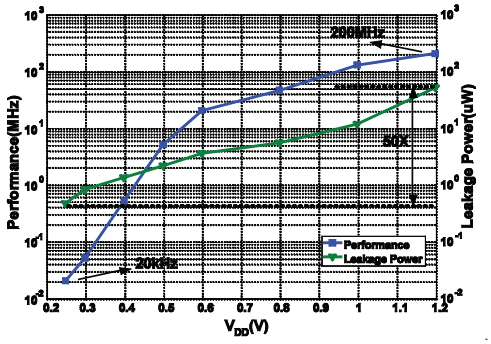


FIGURE 2: Measured performance and leakage power plots for the 64-kbit SRAM array. Over the 0.25-1.2V operating voltage range, leakage power scales by more than 50X.

REFERENCES

[1] N. Verma and A. P. Chandrakasan, "A 65nm 8T sub-vt SRAM employing sense-amplifier redundancy," in *IEEE International Solid-State Circuits Conference, Digest of Technical Papers,* 2007, pp. 328-606.

[2] L. Chang, Y. Nakamura, R. K. Montoye, J. Sawada, A. K. Martin, K. Kinoshita, F. H. Gebara, K. B. Agarwal, D. J. Acharyya, W. Haensch, K. Hosokawa and D. Jamsek, "A 5.3GHz 8T-SRAM with operation down to 0.41V in 65nm CMOS," in *IEEE Symposium on VLSI Circuits,* 2007, pp. 252-253.

[3] M. E. Sinangil, N. Verma and A. P. Chandrakasan, "A reconfigurable 65nm SRAM achieving voltage scalability from 0.25–1.2V and performance scalability from 20kHz–200MHz," in *European Solid-State Circuits Conference,* 2008, pp. 282-285.

A Low-Power 0.7-V H.264/AVC 720p Video Decoder

V. Sze, D. Finchelstein, A. P. Chandrakasan
Sponsorship: Nokia, Texas Instruments

The H.264/AVC video coding standard can deliver high compression efficiency at a cost of large complexity and power [1]. The increasing popularity of video capture and playback on portable devices requires that the power of the video codec be kept to a minimum.

This work proposes several architecture optimizations such as increased parallelism, multiple voltage/frequency domains, and custom voltage-scalable SRAMs that enable low voltage operation to reduce the power of a high-definition decoder. Additionally, this work highlights the importance of on-chip caching in reducing the power and performance penalty of accessing a large off-chip memory. Dynamic voltage and frequency scaling can efficiently adapt to the varying workloads by leveraging the low voltage capabilities and domain partitioning of the decoder. The decoder architecture, shown in Figure 1, is organized as a pipeline that processes 4x4 luma and chroma blocks in parallel [2]. The pipeline units are decoupled by variable-length FIFOs, in order to average out the variable latency of the units, and minimize pipeline stall cycles.

An H.264/AVC Baseline Level 3.2 decoder ASIC was fabricated in 65-nm CMOS and verified. For high definition 720p video decoding at 30 frames per second, it operates down to 0.7 V and has a measured power of 1.8 mW, which is over an order of magnitude lower than previously published results, as shown in Figure 2. The decoder highly scalable and is capable of operating down to 0.5 V for decoding QCIF at 15 frames per second with a measured power of 30 μW. During P-frames (temporally predicted), the decoder power is dominated by the motion compensation (MC) and deblocking filter (DB). The on-chip SRAM caches take up 75% of the active die area, while the parallelism proposed less than 3% area overhead.

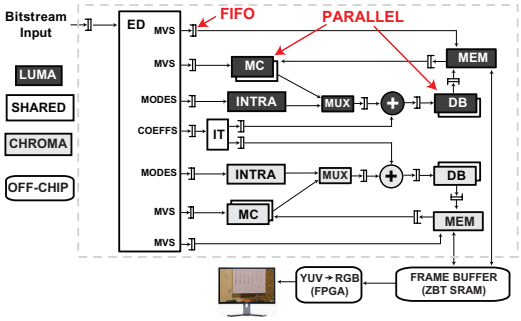


FIGURE 1: H.264 decoder architecture. Pixels are processed using a 4x4 pipeline, separated by FIFOs to average out workload. Luma and chroma pipelines run concurrently, with the exception of ED and IT.

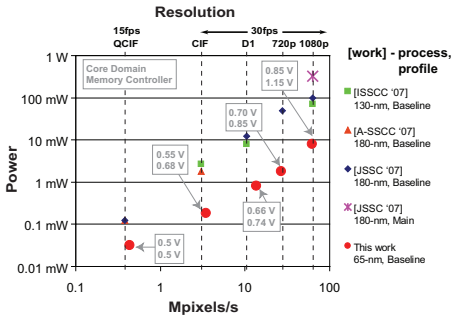


FIGURE 2: Comparison of this chip with other publications. At 720p, our decoder uses 13x lower power than the previous low, though in a more advanced technology (65nm vs. 130nm). Our decoder can scale from QCIF@15 to 1080p@30, with the core voltage scaling from 0.5V to 0.85V.

REFERENCES

[1] J. Ostermann, Bormans, P. List, D. Marpe, M. Narroschke, F. Pereira, T. Stockhammer, and T. Wedi, "Video coding with H.264/AVC: Tools, Performance, and Complexity," *IEEE Circuits and Systems Magazine*, vol. 4, pp. 7– 28, 2004.

[2] D. Finchelstein, V. Sze, M. Sinangil, Y. Koken, A. Chandrakasan, "A Low-power 0.7-V H.264 720p Video Decoder," in *IEEE Asian Solid State Circuits Conference*, November 2008.

A Micro-Power EEG Acquisition SoC with Integrated Seizure Detection Processor for Continuous Patient Monitoring

N. Verma, A. Shoeb, J. Guttag, A. P. Chandrakasan

Sponsorship: Intel Foundation Ph.D. Fellowship Program, CICS, NSERC, National Semiconductor

Epilepsy, a neurological disorder affecting 50 million people worldwide, causes sudden seizures that result in convulsions, loss of coherence, or even death. Seizure detection, before the onset of these symptoms, can improve the lives of patients tremendously by providing an early warning to them and their caregivers, or by triggering therapy to stop the seizure. Early detection, however, requires sophisticated processing to separate normal and abnormal neural activity, which varies greatly from patient-to-patient.

We present a system-on-chip, integrating an ultra-low-power instrumentation amplifier, ADC, and digital processor [1]. The chip continuously senses a patient's neural firings through non-invasive electrodes on the scalp (i.e. EEG). The neural signals are processed to extract the subtle information necessary to detect seizure onset. Seizures are then detected through further processing using a machine-learning classifier. By compressing the neural information, it can be transmitted wirelessly with 14x lower system power, eliminating hazardous cables from the patient's scalp. The detection algorithm has been tested through 536 hours of patient tests [2], and the chip consumes less than 10 micro-Watts/channel (depending on the patient, up to 18 channels may be used).

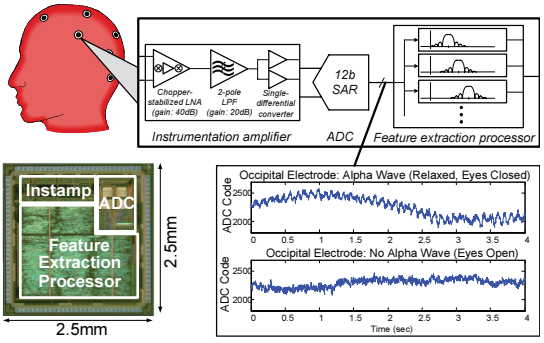


FIGURE 1: Chip block diagram showing instrumentation amplifier, ADC, and seizure feature extraction processor; measured EEG are also shown, sensing neural firings of relaxed eyes closed state.

REFERENCES

[1] N. Verma, A. Shoeb, J. Guttag, and A. Chandrakasan, "A Micro-power EEG Acquisition SoC with Integrated Seizure Detection Processor for Continuous Patient Monitoring," *VLSI Symposium of Circuits*, 2009.

[2] A. Shoeb, B. Bourgeois, S. T. Treves, S. C. Schachter and J. Guttag, "Impact of Patient-Specificity on Seizure Onset Detection Performance," *Engineering in Medicine and Biology Society, 2007. EMBS 2007. 29th Annual International Conference of the IEEE*, pp. 4110-4114, 2007.

Stable Model Reduction: A Semi-definite System-identification Approach for Nonlinear Systems

B. Bond, Z. Mahmood, A. Megretski, L. Daniel
Sponsorship: DARPA, SRC/FCRP IFC

During recent years, a great effort has been made by researchers of the Electronic Design Automation community to develop new techniques for automatically generating accurate compact models of nonlinear system blocks. The majority of existing methods for creating stable reduced models of nonlinear systems, such as [1], require knowledge of the internal structure of the system, as well as access to the exact model formulation for the original system. Unfortunately, this information may not be available if a designer is using a commercial design tool, or may not even exist if the system to be modeled is a physical fabricated device.

As an alternative approach to nonlinear model reduction, we have proposed a system-identification procedure. This procedure requires only data available from simulation or measurement of the original system, such as input-output data pairs. By enforcing incremental passivity, as shown in [2], it is possible to formulate a semi-definite optimization problem whose solution is a stable nonlinear model that optimally matches the given data pairs from the original system. In addition, the proposed optimization formulation allows us to specify completely the complexity of the identified reduced model through the choice of both model order and nonlinear function complexity.

Applications for the proposed modeling technique include analog circuit building blocks such as operational amplifiers and power amplifiers, MEMS devices, and individual circuit elements such as transistors. The resulting compact models may then be used in a higher-level design optimization process of a larger system. One such example of an analog circuit block is the low-noise amplifier shown in Figure 1; it contains both nonlinear and parasitic elements. For this example, input-output training data was generated from a commercial circuit-simulator and used to identify a compact nonlinear model. The output responses of the original system and the identified model are compared in Figure 2.

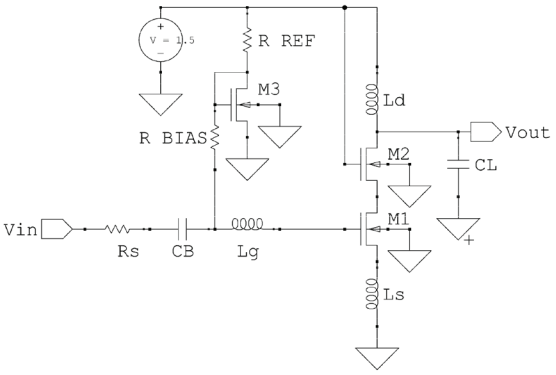


FIGURE 1: Application example: Low-noise amplifier designed in CMOS technology.

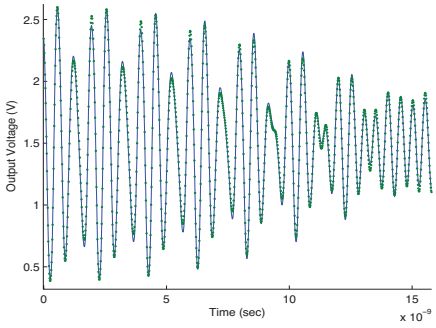


FIGURE 2: Comparison of the output response from a commercial circuit simulator (solid blue line) and the output response from a stable nonlinear reduced model created with the proposed approach (green dots).

REFERENCES

[1] B. Bond and L. Daniel, "Stabilizing schemes for piecewise-linear reduced order models via projection and weighting functions," *Proc. of the IEEE Conference on Computer-Aided Design*, San Jose, CA, Nov. 2007, pp. 860-867.

[2] A. Megretski, "Convex optimization in robust identification of nonlinear feedback," *in Proc. of the IEEE Conference on Decision and Control*, Cancun, Mexico, Dec. 2008, pp. 1370-1374.

Stable Model Reduction: A Projection Approach for Indefinite and Possibly Unstable LINEAR Systems

B. Bond, L. Daniel
Sponsorship: SRC/FCRP IFC

Although stable model reduction for linear systems has been an extremely popular topic for many years and has generated many useful results, there is still a need for more robust and efficient techniques. In [1], a very efficient model-reduction technique preserves stability and passivity only for systems described by system matrices with a particular structure. In [2], a stability-preserving technique is presented for unstructured stable linear systems, but the method is computationally prohibitively expensive. Additionally, existing methods focus only on preserving stability, when in fact it is sometimes necessary to create stability through the model-reduction process. It is not uncommon, for instance, to obtain large unstable models of stable physical systems from field-solvers, as a result of numerical error arising from discretization.

In our work, we have developed a stability-preserving projection framework for model reduction of linear systems that is cheap in terms of computation complexity, puts no requirements on the structure of the original system, and can even generate accurate stable reduced models from originally unstable models of stable physical systems. Specifically, given a right-projection matrix, we derive a set of linear constraints for the left-projection matrix resulting in a projection framework that is guaranteed to generate a stable and passive reduced model. We formulate the problem of computing the stabilizing projection matrix as a semi-definite program that can be solved efficiently using existing techniques, resulting in an optimal stabilizing projection framework. Details of this procedure can be found in [3].

Our algorithms have been tested on a large variety of typical VLSI applications, including field-solver-extracted models of RF inductors for analog applications, power-distribution grids for large VLSI digital integrated circuits, and MEMS devices for sensing and actuation applications. One such application, a spiral RF inductor, is shown in Figure 1. For this example, an electro-magneto-quasi-static (EMQS) field solver was first used to extract a large linear system of order 647 (which turned out to be slightly numerically unstable). The proposed optimization-based method was then used to compute a stabilizing projection framework, finally resulting in a stable 10th order reduced model. Figure 2 plots the quality factor of the large extracted model (solid blue line) and the stable reduced model (red crosses) generated with the proposed approach.

REFERENCES

[1] A. Odabasioglu, M. Celik, and L.T. Pileggi, "PRIMA: passive reduced order interconnect macromodeling algorithm," in *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems*, vol. 17, no. 8, pp. 645-654, Aug. 1998.

[2] B. Moore, "Principal component analysis in linear systems: controllability, observability, and model reduction," *IEEE Transactions on Automatic Control*, vol. 26, no. 1, pp. 17-32, Feb. 1981.

[3] B. Bond and L. Daniel, "Guaranteed stable projection-based model reduction for indefinite and unstable linear systems," *Proc. of the IEEE Conference on Computer-Aided Design*, San Jose, CA, Nov. 2008, pp. 728-735.

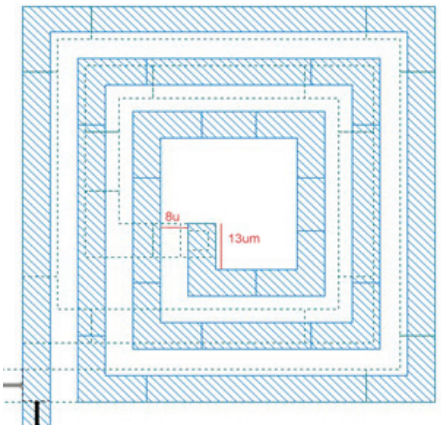


FIGURE 1: Application example: Spiral RF inductor.

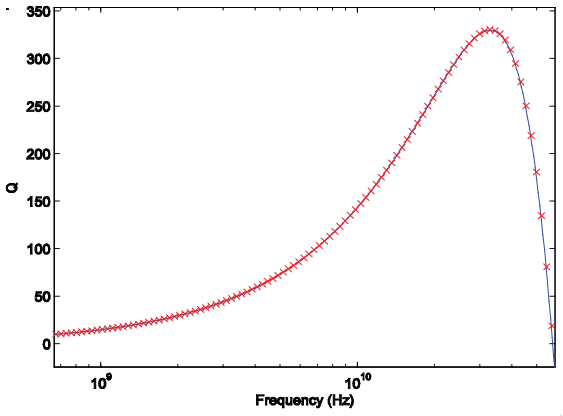


FIGURE 2: Comparison of quality factor for order 647 model extracted from EMQS field solver (solid blue line) and a 10th-order reduced model created with the proposed approach (red crosses).

Stable Model Reduction: A Projection Approach for NONLINEAR Systems in the More General Descriptor Form

B. Bond, L. Daniel
Sponsorship: SRC/FCRP IFC

The ability to generate accurate reduced-order models (ROMs) of nonlinear dynamical systems, such as analog circuits and micro-electro-mechanical systems (MEMS), is a crucial first step in the automatic design and optimization of such systems. One popular approach to model order reduction (MOR) of highly nonlinear systems employs trajectory-based methods, such as the piecewise-linear (PWL) approach. Despite substantial recent interest in such methods [1], [2], trajectory-based models (TBMs) have failed to gain widespread acceptance due to a lack of theoretical statements concerning the accuracy of the resulting ROMs. In this work we address one such theoretical issue: guaranteed stability. Specifically, we present a scheme for preserving stability in PWL models, whose system matrices possess a certain structure. We also propose a projection scheme that allows us to extend some of these stability results to PWL systems composed of arbitrary unstructured matrices.

The stability of nonlinear systems can be certified for instance by the existence of a Lyapunov function. Our stabilizing scheme ensures stability by constructing the projection matrices such that there exists a Lyapunov function for the resulting ROM. In the case where all the Jacobians of the linearized systems possess a certain structure, examples of which are given in [3], we present a projection routine that guarantees the existence of a quadratic Lyapunov function for both the large PWL model and the ROM. In the case where the system's Jacobians have no structure and it is not known whether a Lyapunov function exists for the large PWL model, we utilize a new nonlinear projection to create a collection of stable reduced local models. The resulting nonlinear model is guaranteed to be at least locally stable. One example of a system that produces unstructured Jacobians, and thus potentially unstable TBMs, is a MEMS switch (shown in Figure 1). Figure 2 shows a sample output from the MEMS switch, a stable TBM generated by our approach, and an unstable TBM generated by the traditional approach. For further details on the stabilizing procedure, see [3].

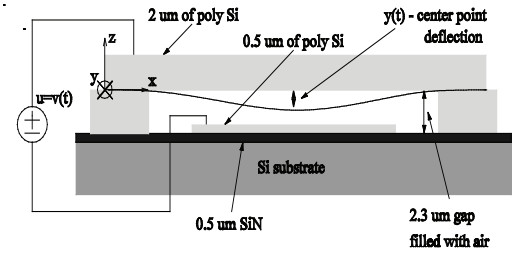


FIGURE 1: Application example: MEM switch realized by a polysilicon beam fixed at both ends and suspended over a semiconducting pad and substrate expansion.

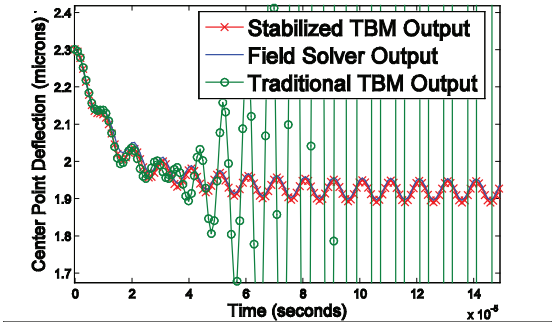


FIGURE 2: Center-point deflection predicted by our stabilized reduced model (red crosses), compared to a finite-difference detailed simulation (solid blue lines) and the traditional TBM approach (green circles).

REFERENCES

[1] M. Rewienski and J.K. White, "A trajectory piecewise-linear approach to model-order reduction and fast simulation of nonlinear circuits and micromachined devices," in *Proc. of IEEE/ACM International Conference on Computer Aided-Design*, San Jose, CA, Nov. 2001, pp 252-257.

[2] B. Bond and L. Daniel, "A piecewise-linear moment-matching approach to parameterized model-order reduction for highly nonlinear systems," *IEEE Trans. on Computer-Aided Design*, vol. 26, no. 12, pp. 2116-2129, Dec. 2007.

[3] B. Bond and L. Daniel, "Stabilizing schemes for piecewise-linear reduced order models via projection and weighting functions," *Proc. of the IEEE Conference on Computer-Aided Design*, San Jose, CA, Nov. 2007, pp. 860-867.

Efficient Capacitance Solver for 3D Interconnect Based on Template-instantiated Basis Functions

Y-C. Hsiao, L. Daniel
Sponsorship: SRC/FCRP IFC, Mentor Graphics, AMD

Integrated circuit performance and signal integrity can be largely affected by interconnect parasitic capacitance, and they require fast and accurate extraction tools. Satisfying simultaneously both constraints is, however, an extremely challenging task. The current state-of-the-art in efficient extraction methods involves 2D cross-section scanning, determining wire adjacency, calculating 2D capacitance in a table lookup approach, and then reconstructing quasi-3D capacitance. Such an approach is indeed fast, yet it is accurate only for 2D structures. Full 3D structures (e.g., crossing wires in adjacent metal layers) need the accuracy of field solvers such as FastCap [1] and Precorrected FFT [2]. Such tools are based on piece-wise constant basis functions and are accelerated by fast matrix-vector products that have a significant computational overhead but scale almost linearly with the number of conductors. Hence they are ideal for very large-scale examples.

This project is targeted instead at efficient small-to-medium scale capacitance extraction. The key idea is to exploit the highly restrictive design rules of the recent sub-micro to nano-scale technologies. In this scenario, a limited number of pre-computed surface charge distributions can be used as a set of fundamental template basis functions. Figure 1 shows an example of charge distribution "stretchability," enabling the instantiation of basis functions for every practical interconnect structure. Using a total of just 72 template-instantiated basis functions, the example in Figure 2 demonstrates a worst-case relative error of 3% with respect to the total capacitance of each conductor, compared to the result extracted by FastCap in a very fine discretization with tens of thousands of unknowns. FastCap requires 732 unknowns to produce the same 3% error in a coarser discretization. Hence, for the same 3% accuracy, our algorithm requires approximately 10x fewer unknowns. In such medium-size examples, the overhead of the FastCap multipole expansion makes the linear acceleration ineffective, while in our approach, analytical formulas and numerical tabulation of the Galerkin coefficients for our template basis functions can effectively limit the setup overhead, producing a *two-orders-of-magnitude* improvement in both simulation time and memory requirement.

REFERENCES

[1] K. Nabors and J. White, "FastCap: A Multipole-Accelerated 3-D Capacitance Extraction Program," *IEEE Transactions on Computer-Aided Design*, vol.10, no. 10, pp. 1447-1459, November 1991.

[2] J.R. Phillips and J. K. White, "A Precorrected-FFT method for Electrostatic Analysis of Complicated 3-D Structures," *IEEE Trans. on Computer-Aided Design*, vol. 16, no.10, p.059-1072, October 1997.

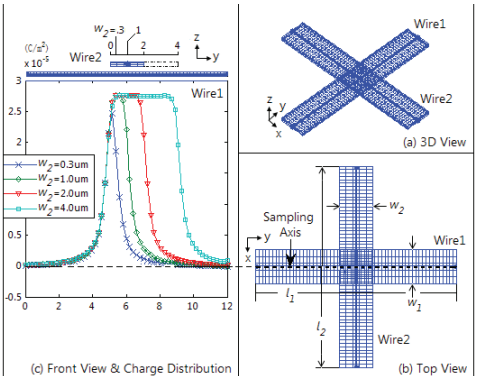


FIGURE 1: A pair of crossing wires: (l_1, w_1, l_2, w_2) = (12, 2, 12, 2) (um). (a) 3D view, (b) Top view (x-y plane), (c) Front view (y-z plane), and charge distribution sampled along the sampling axis of Wire1 shown in (b) as a broken line. Note the charge distributions are "stretchable" with w_2 while preserving decaying shapes off the edge of Wire2.

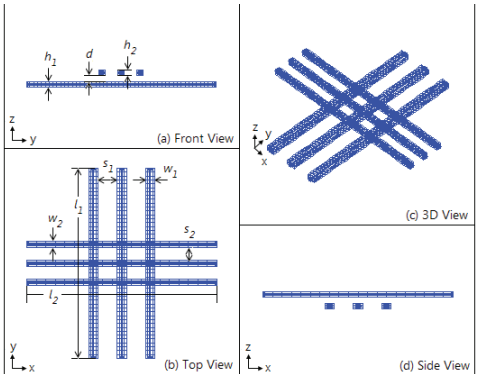


FIGURE 2: Six wires in two metal layers: (l_1, w_1, h_1, s_1 | l_2, w_2, h_2, s_2 | d) = (10, 0.2, 0.3, 0.2 | 10, 0.2, 0.3, 0.2 | 0.3) (um). (a) Front view (y-z plane), (b) Top view (x-y plane), (c) 3D view, and (d) Side view (x-z plane). The width and spacing are exaggerated for clarity.

Variation-aware Parasitic Extraction: A Deterministic Approach

T. A. El-Moselhy, L. Daniel
Sponsorship: SRC/FCRP IFC, IBM

On-chip and off-chip fabrication processes may typically generate interconnect structures of irregular geometries. Such irregularities are not deterministic and are produced by several different manufacturing steps such as etching, chemical mechanical polishing (CMP), electro-deposition, and photolithography. However, as a result of technology scaling, such manufacturing uncertainties significantly affect the electrical characteristics of the interconnect structures. The effect of such variations on the electrical characteristics can be efficiently extracted using what we call "variation-aware" parasitic extraction tools. Such solvers can in general be divided into two categories, namely, those based on deterministic algorithms and those based on stochastic algorithms.

In this project we have developed new ***deterministic*** variation-aware extraction algorithms based on the well-known floating random walk (FRW) algorithm [1]. First, we have presented a new finite-difference-based sensitivity analysis [2] within the improved FRW algorithm to efficiently compute capacitance sensitivities with respect to a large number of small parameter variations. We have demonstrated that the expected complexity of computing the nominal capacitance and all the sensitivities is less than 2 times that of computing only the nominal capacitance regardless of the number of parameters. The complexity of our sensitivity algorithm is therefore independent of the number of varying parameters (unlike standard finite difference sensitivity analysis) and independent of the number of output capacitances (unlike standard adjoint sensitivity analysis [3]). Second, we have presented a new incremental FRW algorithm [2] to efficiently compute the capacitances of similar geometrical configurations resulting from simultaneous large perturbations of the geometrical parameters of a common geometrical topology. The new algorithm satisfies a major objective of variation-aware parasitic extraction, namely, that the average time required to solve a single geometrical configuration within a set of similar configurations is reduced as the cardinality of the set is increased. We have observed that the average simulation time of a single configuration from a set of similar configurations of cardinality 100,000 is reduced by three orders of magnitude. Consequently, we were able to solve more than 130,000 similar configurations in the time required to solve just 50 independent configurations. We believe that the latter result will naturally fit in a litho- and CMP-aware extraction flow.

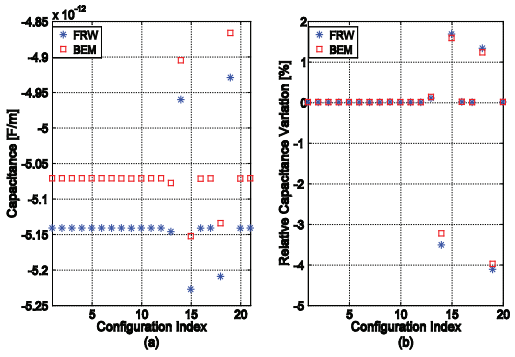


FIGURE 1: (a) Capacitance, (b) Relative capacitance variation, i.e., the difference between the capacitance of any configuration and that of the nominal configuration divided by the capacitance of the nominal, as computed using our FRW sensitivity algorithm and the standard boundary element method (BEM) for different geometrical configurations.

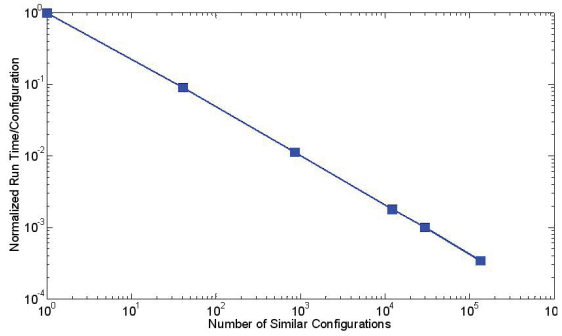


FIGURE 2: Normalized average simulation time for a single geometry (configuration) in a set of similar geometries versus the total number of configurations in the set.

REFERENCES

[1] R. B. Iverson and Y. L. Le Coz, "A Stochastic Algorithm for High Speed Capacitance Extraction in Integrated Circuits" *Solid-State Electronics*, vol. 35, no. 7, pp. 1005-1012, 1992.

[2] T. Moselhy, I. M. Elfadel and L. Daniel, "A Capacitance Solver for Incremental Variation-Aware Extraction," in *Proc. IEEE/ACM International Conference on Computer Aided Design*, 2008.

[3] J. Wang and J. White, "Fast Algorithms for Computing Electrostatic Geometric Sensitivities" in *Proc. International Conference on Simulation of Semiconductor Processes and Devices*, pp. 121-123, 1997.

Variation-aware Parasitic Extraction: A Stochastic Approach

T. A. El-Moselhy, L. Daniel
Sponsorship: SRC/FCRP IFC, IBM

On-chip and off-chip fabrication processes may typically generate interconnect structures of irregular geometries. Such irregularities are not deterministic and are produced by several different manufacturing steps such as etching, chemical mechanical polishing (CMP), electro-deposition, and photolithography. However, as a result of technology scaling, such manufacturing uncertainties significantly affect the electrical characteristics of the interconnect structures. The effect of such variations on the electrical characteristics can be extracted using what we call "variation-aware" extraction tools. Such solvers can in general be divided into two categories, namely, those based on deterministic algorithms and those based on stochastic algorithms.

In this research we have developed a new ***stochastic*** algorithm to solve large stochastic linear systems typically appearing during variation-aware extraction [1]. We have derived a new theorem to compute the coefficients of the multivariate Hermite expansion using only low dimensional integrals, resulting in a time complexity that is independent of the number of variables and dependent only on the order of the expansion. Practically speaking, for a typical large multivariate expansion, the new theorem provides an improvement in the computation time by 86 orders of magnitude as compared to the standard tensor product rule or by 10 orders of magnitude as compared to the state of the art (Monte Carlo integration or sparse grid integration [2]). Such a theorem is not only useful for our methodology but it can also be applied to any algorithm that relies on expanding a random process, such as the stochastic finite element method (SFE) [3]. We have also provided a new stochastic simulation technique by merging both the Neumann expansion and the polynomial chaos expansion. The main advantages of the resulting technique are the compact size of the system (unlike SFE) and the ease of calculating the statistics of the high order terms (unlike Neumann expansion [4]). In addition, the new simulation algorithm is parallelizable and can therefore take advantage of the multicore platforms readily available in recent processor technologies. We have demonstrated the computational efficiency of the new methodology by solving problems that were completely intractable before. We have demonstrated that our algorithm can be used to compute the complete probability density function of the input impedance of very large problems (up to 400 random variables) in less than 8 hours using Matlab on a standard 4-core machine and using only 121MB RAM.

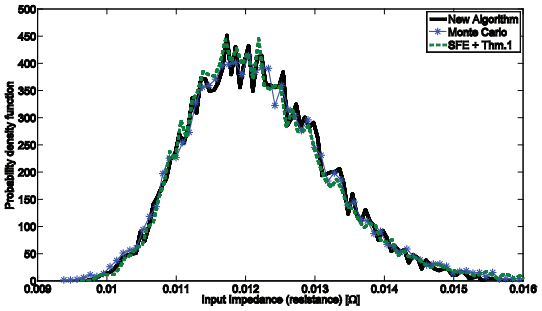


FIGURE 1: Comparison between the probability density function of the microstrip line obtained from our new algorithm and the reference Monte Carlo simulation.

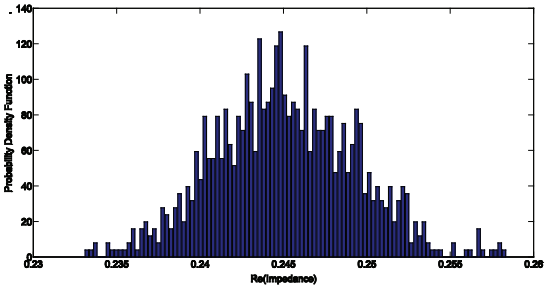


FIGURE 2: Probability density function of the real part of the input impedance at 1GHz for correlation length Lc = 50μm. The resistance of the non-rough surface is 11.3% smaller than the mean of the obtained distribution.

REFERENCES

[1] T. Moselhy and L. Daniel, "Stochastic Integral Equation Solver for Variation-Aware Interconnect Extraction," in *Proc. IEEE/ACM Design Automation Conference,* 2008.

[2] D. Xiu and G. Karniadakis, "The Wiener-Askey Polynomial Chaos Expansion For Stochastic Differential Equations," *SIAM Journal of Scientific Computing*, vol. 24, pp. 619-644, Oct. 2002.

[3] R. Ghanem and P. Spanos, *Stochastic Finite Elements: A Spectral Approach*. Spring-Verlag, 1991.

[4] Z. Zhu and J. White, "FastSies: A Fast Stochastic Integral Equation Solver for Modeling the Rough Surface Effect," in *Proc. IEEE/ACM International Conference on Computer Aided Design,,* pp. 675-682, Nov. 2005.

Digital-to-RF-Phase Converter for AMO Architecture

T. W. Barton, S. Chung, P. A. Godoy, D. J. Perreault, J. L. Dawson
Sponsorship: Desphande Center for Technological Innovation, SiGe Semiconductor

This work presents a digital to RF phase converter (DRFPC) designed specifically for the Asymmetric Multilevel Outphasing (AMO) transmitter architecture [1]. The AMO architecture, shown in Figure 1, has great advantages in efficiency over similar architectures such as Multilevel LINC (linear amplification with non-linear components) without loss of linearity. By allowing the power amplifiers (PA) supplies to vary independently between multiple levels, the DRFPC reduces the burden on outphasing as a way to control output signal amplitude. Instead, outphasing is used primarily for pulse shaping. This use, along with the abrupt phase-changes required when the amplitude path steps between discrete levels, translates to a requirement for a high-speed phase path.

The DRFPC presented in this work is designed to perform the phase modulation required for the AMO phase path. Because of the requirement that this phase path be very wideband, a closed loop approach such as a phase locked loop (PLL) is impractical. Instead, a differential current-steering topology is the preferred approach, in which weighted quadrature signals are added to produce an arbitrary output angle [2], [3]. The design choice made in this work exploits its use in the AMO architecture. In particular, the digital predistortion used in the transmitter allows for reduced linearity requirements in the design and therefore creates a topology that is relatively low-area and low-power. For example, by constraining the possible inputs to the DRFPC so that the amplitudes of the quadrature signals always sum to one, it is possible to use only one set of binary weighted current sources. This constraint results in a nonlinearity in the DRFPC but nearly halves its area and reduces matching requirements as compared to a generalized approach. A simplified DRFPC schematic is shown in Figure 2.

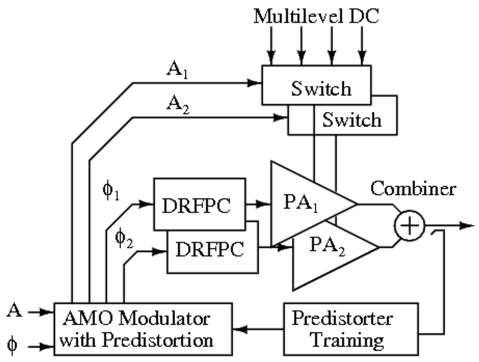


FIGURE 1: The AMO architecture. The ability in the amplitude path to independently switch between discrete voltages moves the outphasing focus from amplitude control to pulse shaping.

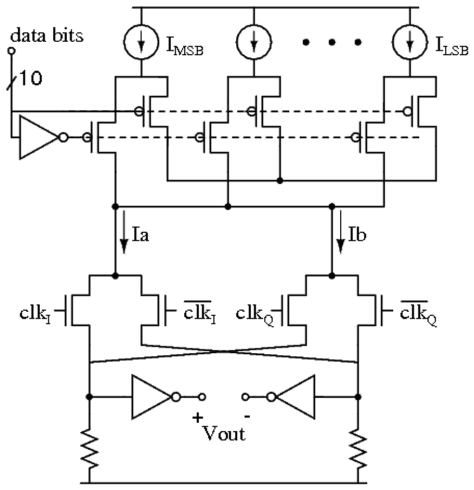


FIGURE 2: Digital to RF phase converter (DRFPC) schematic. The AMO digital predistortion allows for the use of only one set of current sources, nearly halving the required area.

REFERENCES

[1] S. Chung, P. A. Godoy, T.W. Barton, E. W. Huang, D. J. Perreault, and J. L. Dawson, "Asymmetric Multilevel Outphasing Architecture for multi-standard transmitters," *Radio Frequency Integrated Circuits Symposium, 2009. RFIC 2009. IEEE*, 2009.

[2] P. Eloranta, P. Seppinen, S. Kallioinen, T. Saarela and A. Parssinen, "A Multimode Transmitter in 0.13 µm CMOS Using Direct-Digital RF Modulator," *Solid-State Circuits, IEEE Journal of*, vol. 42, pp. 2774-2784, 2007.

[3] M. E. Heidari, M. Lee and A. A. Abidi, "All-Digital Outphasing Modulator for a Software-Defined Transmitter," *Solid-State Circuits, IEEE Journal of*, vol. 44, pp. 1260-1271, 2009.

Digitally-Assisted Analog Front-End for Biomedical Sensors

J. L. Bohorquez, M. Yip, A. P. Chandrakasan, J. L. Dawson

Sponsorship: Texas Instruments, DARPA

Biomedical sensors are used to measure a myriad of biopotential signals including electroencephalogram (EEG), electrocardiogram (EKG), electromyogram (EMG), and neural field potential (NFP) signals [1], [2], [3]. Most of the useful information in these signals resides in the frequency range of 0.5 Hz to 1 kHz, allowing ultra-low power circuits to be used when processing them. This is critical for systems that are implanted, since energy is extremely scarce, and the lifetime of the device must be on the order of 10 years. Unfortunately, these signals are often as small as 10 μVs, and their low frequency location make them vulnerable to aggressors such as DC offset, powerline noise, and flicker noise. DC offset can result from charge accumulation at the interface between the metal electrodes and the skin, and also from amplifier offsets caused by random mismatches. While chopper stabilization has proved effective at mitigating the effects of amplifier DC offset and flicker noise, electrode DC offset cannot be removed through chopping and must be high-pass filtered at the front end of the system to prevent saturation [1], [2], [3]. Powerline noise, typically at 50 or 60 Hz, is mostly a common-mode signal that requires adequate common-mode rejection. However, if there are mismatches or inductive loops in the electrodes, these aggressors can become differential-mode signals, corrupting the desired signal, and potentially saturating the system. In closed-loop deep brain stimulation systems, another aggressor arises from stimulation artifacts [4]. In that case, the NFPs can be much smaller than stimulation artifacts placing stringent requirements on the dynamic range of the system and potentially leading to signal corruption.

We propose a mixed-signal sensor interface that mitigates the effects of all of the aforementioned aggressors in an area efficient manner. Area efficiency is particularly compelling in implantable devices that use tens or hundreds of electrodes, such as neural recording systems [3]. The proposed system, shown in Figure 1, uses a chopper stabilized operational amplifier with capacitive feedback to achieve accurate gain (The system is shown as single-ended for simplicity, but is implemented in a fully differential manner). Figure 2 shows a simplified schematic of the amplifier, including a novel input chopper that creates a switched capacitor resistance between its inputs and a reference voltage. This resistance is shown as Rp in Figure 1 and is used to create a high-pass filter with a corner frequency well below 1 Hz, while setting the common-mode voltage of the input to a desired level. The pole frequency is actually set by the Miller-multiplied feedback capacitor Cf and is inversely proportional to the amplifier's gain A_v, allowing a reduction of many orders of magnitude in component sizes. An additional feedback path is introduced that includes the filter, ADC, DSP, and a feedback DAC. This path can be used to notch out unwanted signals such as powerline noise or stimulation artifacts before they can saturate the system.

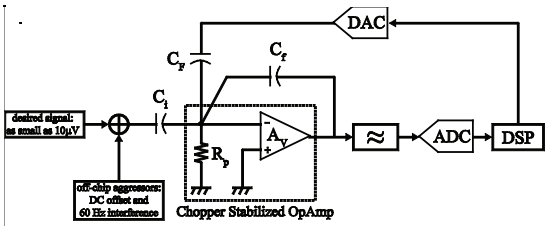


FIGURE 1: Biomedical sensor interface system employing chopper stabilization, and mixed signal feedback to mitigate the effects of DC offset, flicker noise, and other aggressors.

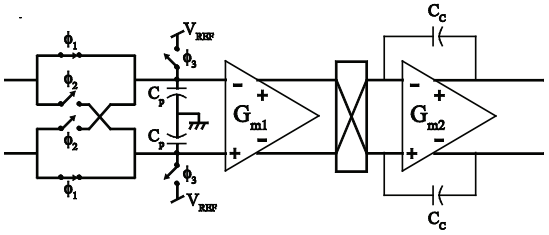


FIGURE 2: Simplified schematic of a chopper stabilized operational amplifier that exploits the parasitic switched-capacitor conductance to implement a high-pass filter.

REFERENCES

[1] T. Denison, K. Consoer, W. Santa, A. Avestruz, J. Cooley, and A. Kelly, "A 2μW 100nV/rtHz chopper-stabilized instrumentation amplifier for chronic measurement of neural field potentials," *IEEE J. Solid-State Circuits*, vol. 42, no. 12, pp. 2934–2945, Dec. 2007.

[2] R. F. Yazicioglu, P. Merken, R. Puers, and C. V. Hoof, "A 200μW eight-channel EEG acquisition ASIC for ambulatory EEG systems," *IEEE J. Solid-State Circuits*, vol. 43, no. 12, pp. 3025–3038, Dec. 2008.

[3] R. R. Harrison *et al.*, "A low power integrated circuit for a wireless 100-electrode neural recording system," *IEEE J. Solid-State Circuits*, vol. 42, no. 1, pp. 123–133, Jan. 2007.

[4] J. Lee, H.–G. Rhew, D. Kipke, and M. Flynn, "A 64 channel programmable closed-loop deep-brain stimulator with 8 channel neural amplifier and logarithmic ADC," in *Symp. VLSI Circuits Dig.*, Honolulu, HI, Jun. 2008, pp. 76–77.

Asymmetric Multilevel Outphasing Architecture for Multi-standard Transmitters

S. Chung, P. A. Godoy, T. W. Barton, Z. Li, T. W. Huang, D. J. Perreault, J. L. Dawson
Sponsorship: Lincoln Laboratory, Deshpande Center for Technological Innovation

In order to increase overall power efficiency of RF power amplifiers (PAs) over a wider output power range and significantly simplify RF/analog front-end for the PAs, we designed a new outphasing transmitter architecture based on asymmetric multilevel outphasing (AMO) modulation [1]. Figure 1 compares the AMO modulation with linear amplification with nonlinear component (LINC) [2] and multilevel (ML) LINC modulation [3]. Independently switching the supply voltage for each PA achieves the smallest outphasing angle with AMO. Discrete supply voltage levels and low oversampling allow wideband transmission such as for WLAN, WiMAX, and 4G LTE systems.

The power-efficiency improvement of AMO transmitter is compared with LINC and ML-LINC in Figure 2. Depending on the probability density distribution of transmission signal amplitude, each of the supply voltage levels can be optimized. For demonstration, an overall transmitter is simulated in a 65-nm CMOS process with HSUPA and WLAN signals. Compared to conventional outphasing modulation, the simulation results show an efficiency improvement from 17.7% to 40.7% for HSUPA at 25.3 dBm output power and from 11.3% to 35.5% for WLAN 802.11g at 22.8 dBm, while still meeting system linearity requirements.

A compact and low-power all-digital modulator, replacing the bulky RF/analog front-end, has been designed to drive a PA in AMO transmitters. For a small silicon footprint and wideband linear operation, digital predistortion technique is applied to compensate for the mismatch existing in an open-loop direct RF phase converter.

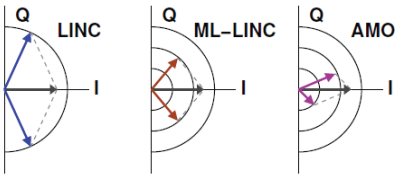


FIGURE 1: Signal component vector diagram for LINC, ML-LINC, and AMO. The smallest outphasing angle is achieved with AMO.

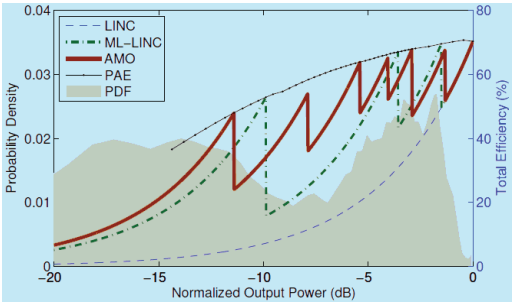


FIGURE 2: Probability density distribution of HSUPA signal amplitude and corresponding efficiency for standard LINC, ML-LINC, and AMO with a 65-nm CMOS switching PA.

REFERENCES

[1] S. Chung, P. A. Godoy, T. W. Barton, Z. Li, T. W. Huang, D. J. Perreault, J. L. Dawson, "Asymmetric multilevel outphasing architecture for multi-standard transmitters," to be presented *at IEEE Symposium on Radio Frequency Integrated Circuits*, Boston, MA, June, 2009.

[2] D. Cox, "Linear amplification with nonlinear components," *IEEE Transactions on Communications*, vol. 12, pp. 1942-1945, Dec. 1974.

[3] Y.-J. Chen, K.-Y. Jheng, A.-Y. Wu, H.-W. Tsao, and B. Tzeng, "Multilevel LINC system design for wireless transmitters," in *Proc. International Symposium on VLSI Design, Automation, and Test*, 2007, pp. 25-27.

[4] M. E. Heidari, M. Lee, and A. A. Abidi, "All digital outphasing modulator for a software-defined transmitter," *IEEE Journal of Solid State Circuits*, vol. 44, pp. 1260-1271, Apr. 2009.

Digitally Assisted Subsampler for RF Power-amplifier Linearization Systems

S. Chung, J. L. Dawson
Sponsorship: SRC/FCRP C2S2

Subsampling is recognized as an energy-efficient signal processing technique for highly digital transceivers [1]-[3]. However, subsamplers are notorious for low SNR performance due to noise folding and for stringent requirements for anti-aliasing prefilters. This combination of faults has largely undermined their use in high-performance receivers. In transmitters, however, the situation is *fundamentally* different. The signal environment has fewer extreme aggressors, such as blockers, and the transmitted data is often known in advance of actual transmission. This last fact enables the use of averaging and other signal processing techniques to overcome the noise-folding problem.

Figure 1 shows a digitally assisted subsampler, which is designed to serve as a downconversion path in adaptive predistortion transmitters with 800MHz-5.8GHz RF power amplifiers [4]. We use digital averaging to overcome the noise-folding problems of subsampling, obtaining a final SNDR of 73.1dB for signals centered around a 2.4GHz carrier. Using quadrature subsampling, we obtain both I and Q samples from the same physical path and thereby eliminate the IQ gain mismatch. When used as part of an adaptive predistortion system, the subsampler enables an EVM improvement of 3.2% and distortion products suppression of up to 7.6dB for 802.11g signals. The subsampler IC, designed in a 90-nm CMOS process, consumes 6.0mW from a 1.2V supply.

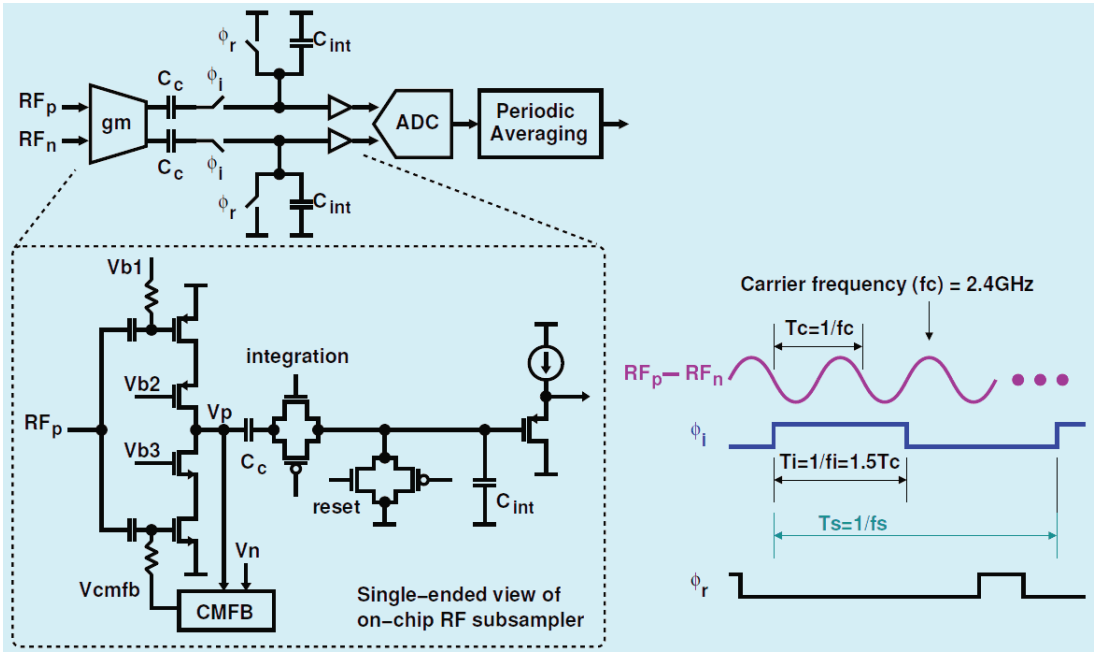


FIGURE 1: Digitally assisted subsampler architecture. Quadrature sampling is employed (i.e., Q samples are offset from I samples by Tc/4), allowing both the I and Q samples to be obtained from the same physical signal path.

REFERENCES

[1] H. Pekau *et al.,* " 2.4GHz CMOS sub-sampling mixer with integrated filtering," *IEEE Journal of Solid-State Circuits*, pp. 2159-2166, Nov. 2005.

[2] S. Karvonen *et al.,* "A quadrature charge-domain sampler with embedded FIR and IIR filtering functions," *IEEE Journal of Solid-State Circuits*, pp. 507-515, Feb. 2006.

[3] R Bagheri *et al.,* "An 800-MHz.6-GHz software-defined wireless receiver in 90-nm CMOS," *IEEE Journal of Solid-State Circuits*, pp. 2860-2876, Dec. 2006.

[4] S. Chung and J. L. Dawson, "73.1dB SNDR digitally assisted subsampler for RF power amplifier linearization systems," to be presented at *IEEE Symposium on VLSI Circuits*, Kyoto, Japan, June, 2009.

Outphasing Energy-recovery Amplifier with Resistance Compression for Improved Efficiency

P. A. Godoy, D. J. Perreault, J. L. Dawson

Sponsorship: Deshpande Center for Technological Innovation, CICS

The outphasing power amplifier dates back to the early 1930's as an approach for the simultaneous realization of high-efficiency and high-linearity amplification [1]. The principle of outphasing, also known as linear amplification of nonlinear components (LINC) [2], is shown in Figure 1(a). It is based on the idea that an arbitrary input signal can be divided into two constant-amplitude, phase-modulated signals that can each be non-linearly amplified and then recombined as a vector sum to produce an output signal that is a linearly amplified version of the input. The key advantage of this approach is that each amplifier operates in an efficient albeit nonlinear mode, and yet the final output can be highly linear, breaking the usual tradeoff between efficiency and linearity. The disadvantage lies in the output-combining network: when the two amplifiers are outphased to vary the amplitude, power is wasted as heat in the isolation resistor [3].

We describe a new outphasing energy recovery amplifier (OPERA) shown in Figure 1(b) that replaces the isolation resistor in the conventional matched combiner with a resistance-compressed rectifier for improved efficiency. The rectifier recovers the power normally wasted in the isolation resistor back to the power supply, while a resistance compression network (RCN) [4] reduces the impedance variation of the rectifier as the output power varies. Because the combiner requires a fixed resistance at the isolation port to ensure matching and isolation between the two outphased power amplifiers (PAs), the RCN serves to maintain high linearity as well as high efficiency in the switching-mode PAs. For demonstration, a prototype OPERA system is designed and implemented with discrete components at an operating frequency of 48MHz, delivering 20.8W peak power with 82.9% PAE. The measurement results show an efficiency improvement from 17.9% to 42.0% for a 50kHz 16-QAM signal with a peak-to-average power ratio of 6.5dB.

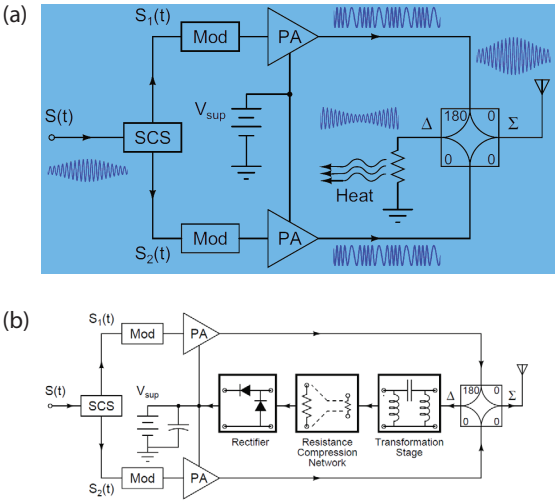


FIGURE 1: (a) Outphasing power amplifier illustrating power wasted in the combining network. (b) Proposed outphasing energy recovery amplifier, utilizing a resistance-compression network in the power-recycling network.

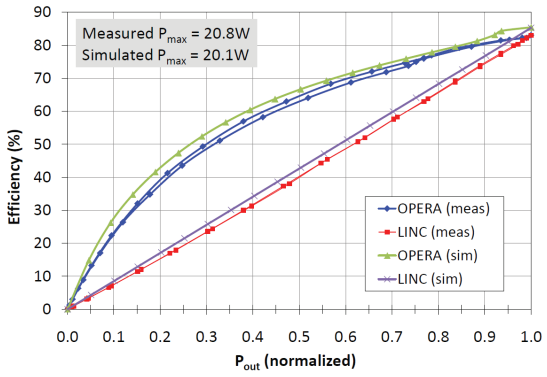


FIGURE 2: Simulated and measured system efficiency vs. output power for the OPERA prototype, with and without energy recovery.

REFERENCES

[1] H. Chireix, "High Power Outphasing Modulation," *Proceedings of the IRE,* vol. 23, pp. 1370-1392, 1935.

[2] D. Cox, "Linear Amplification with Nonlinear Components," *Communications, IEEE Transactions on,* vol. 22, pp. 1942-1945, 1974.

[3] I. Hakala, D. K. Choi, L. Gharavi, N. Kajakine, J. Koskela and R. Kaunisto, "A 2.14-GHz Chireix outphasing transmitter," *Microwave Theory and Techniques, IEEE Transactions on,* vol. 53, pp. 2129-2138, 2005.

[4] Y. Han, O. Leitermann, D. A. Jackson, J. M. Rivas and D. J. Perreault, "Resistance Compression Networks for Radio-Frequency Power Conversion," *Power Electronics, IEEE Transactions on,* vol. 22, pp. 41-53, 2007.

SAR ADC with Local Supply Capacitors and Adiabatic Charging for Use in Medical Implants

T. Khanna, J. L. Dawson

The proposed research program has two primary goals. The first goal is to improve the evaluation and treatment of patients with diabetes and a variety of movement disorders, including Parkinson's disease, restless legs syndrome, and essential tremor, by allowing doctors to continuously monitor relevant biomarkers over much longer time scales and with better precision than currently possible. The second goal is that the proposed implant be a *platform* for electronic sensory monitoring that is inexpensive and flexible and that can be used with a wide variety of sensors and for a wide variety of purposes, such as chemical sensors for monitoring blood chemistry. In this work, we develop an energy-efficient analog-to-digital converter designed to operate with a power management scheme using ultracapacitors as opposed to a battery.

Two techniques are employed to save on energy for the entire system. The first is the use of an integrated capacitor that acts as a local supply for the data conversion circuit. This technique allows for us to duty-cycle the bandgap reference circuit used for power management and can be seen in Figure 1. The second technique is to use adiabatic charging [1], [2] of the capacitors contained in the SAR ADC. This application is ideal for adiabatic techniques because of the low frequency of operation and the ease with which we can reclaim energy from discharging the capacitors. Building on the application in [3], our integrated capacitor acting as a local supply allows us to reclaim energy without having to design any energy-recovery circuitry.

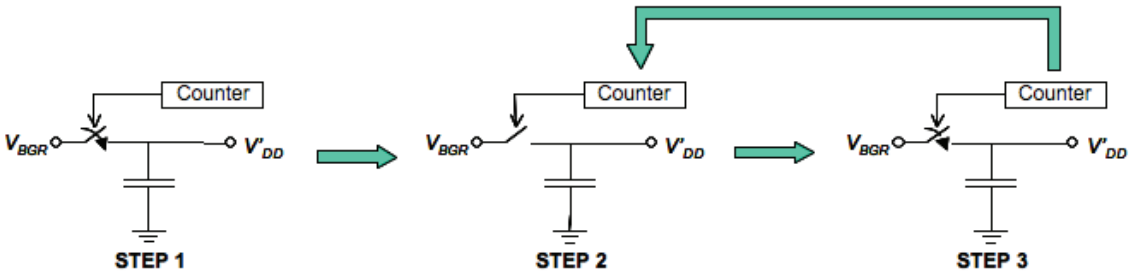


FIGURE 1: Charging algorithm for local supply capacitor.
Step 1: Charge integrated capacitor to bandgap reference (BGR) voltage, V_{BGR}.
Step 2: Run circuits for N clock cycles until temporary supply voltage, V'_{DD}, is reduced by m%.
Step 3: On-chip counter triggers switch after N clock cycles and charges integrated capacitor up to BGR voltage. Return to Step 2.

REFERENCES

[1] L. J. Svensson and J. G. Koller, "Driving a capacitive load without dissipating fCV^2," *Low Power Electronics, 1994. Digest of Technical Papers. , IEEE Symposium,* pp. 100-101, 1994.

[2] J. G. Koller and L. J. Svensson, "Adiabatic charging without inductors," *USC/ISI technical report ACMOSTR-3a*, Feb 8, 1994.

[3] M. van Elzakker, E. van Tuijl, P. Geraedts, D. Schinkel, E. Klumperink and B. Nauta, "A 1.9µW 4.4fJ/Conversion-step 10b 1MS/s Charge-Redistribution ADC," *Solid-State Circuits Conference, 2008. ISSCC 2008. Digest of Technical Papers. IEEE International,* pp. 244-610, 2008.

[4] T. Denison, W. Santa, G. Molnar and K. Miesel, "Micropower Sensors for Neuroprosthetics," *Sensors, 2007 IEEE,* pp. 1105-1108, 2007.

Memory Architecture for µImplant

H. S. Khurana, J. L. Dawson

Sponsorship: Irwin Mark Jacobs and Joan Klein Jacobs Presidential Fellowship

The evaluation and effective treatment of patients suffering from movement disorders such as Parkinson's disease, restless legs syndrome, and others require continuous monitoring and reliable data collection. This monitoring is a challenge due to routine movements of patients and shortcoming of the methods that rely on patients measuring themselves. To overcome these challenges the group uImplant focuses on developing an inconspicuous and minimally invasive IC system encapsulated in a bio-compatible packaging. The complete system will consist of three main areas: power management, signal collection, and data storage and communication. In this direction we have designed a customized low-power sub-threshold SRAM with on-chip features that reduce energy consumption.

The SRAM (Figure 1) is designed with the low-power application in focus. It is 32-kb, 6T bit-cell sequential read/write memory with on-chip power-saving features. Since the data gets written sequentially, the rows are powered just before they get written with valid data. After each row-write, the row written stays on for data retention. The unused rows at any given time stay unpowered, thereby saving precious energy in micro-implant applications. Further savings come by lowering the leakage currents associated with standby cells.

In low-frequency sub-threshold operations, the leakage currents dominate the power consumption and are the main energy sinks. Since leakage currents are a strong function of the supply voltage, it is important to reduce the voltage to the lowest possible levels without losing the bit cell data. In this memory, the system supply voltage is stepped down using a capacitor stack (Figure 2) that switches between a series and a parallel configuration to divide the voltage to desired voltage levels. Besides low standby leakage currents, low dynamic currents give additional savings during the write operation.

The architecture enables independent floating of the supply voltage to each word in the memory. This floating trait reduces power consumption during the write operation. It also reduces the minimum size requirement on the pass transistors connecting the data input bit-lines to the bit cell during the write operation.

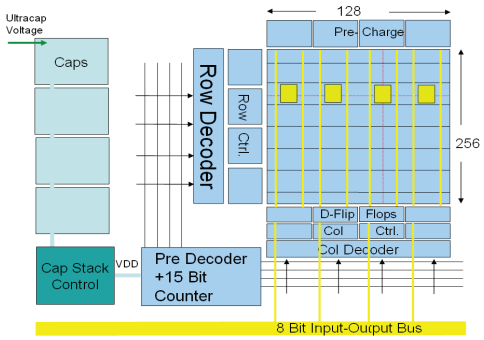


FIGURE 1: Architecture of the 32-kb (128x256) SRAM with energy-saving features.

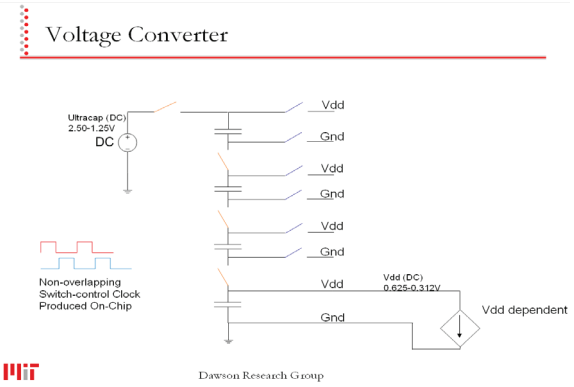


FIGURE 2: Voltage divider using capacitor stack with switches.

REFERENCES

[1] B. H. Calhoun, and A. P. Chandrakasan, "A 256-kb 65-nm Sub-threshold SRAM Design for Ultra-Low-Voltage Operation," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 3, pp. 680-688, Mar. 2007.

[2] Jan M. Rabaey, Anantha Chadrakasan, and Borivoje Nikolic, *Digital Integrated Circuits*. New Jersey: Prentice Hall, 2003.

[3] Jiann S. Yuan, and Li Yang, "Teaching Digital Noise and Noise Margin Issues in Engineering Education," *IEEE Transactions on Education*, vol. 48, pp. 162-167, Feb 2005.

[4] R.J. Baker, *CMOS – Circuit Design, Layout, and Simulation*. John Wiley and Sons: IEEE Press, 2005.

Transmitters for High Efficiency, 10 Gb/s Wireless Communications in the 60 GHz Band

O. T. Ogunnika, J. L. Dawson
Sponsorship: SiGe Semiconductor, Lincoln Laboratory

The purpose of this project is to design an RF transmitter architecture that achieves 10 Gb/s data transfer over a 60 GHz wireless link with high power efficiency. With the availability of 7 GHz of unlicensed bandwidth centered at 60 GHz, this space has emerged as an active area of research. A number of challenges will be faced in the process of bringing this project to completion. Strong atmospheric absorption at 60 GHz lowers the signal-to-noise ratio (SNR) available at the receiver [2]. The low SNR limits the complexity of the constellations that can be used and thus reduces the number of bits per symbol that can be encoded with the modulation strategy. Extremely fast baseband modulators will therefore be required for high data rate transmission because more symbols per second will have to be transmitted. The fundamental challenge of simultaneously obtaining good linearity and high efficiency in power amplifiers is further exacerbated at this carrier frequency, complicating transceiver design. Delivering significant power at 60 GHz requires very fast devices with high f_{max} and f_T. This technological hurdle has been lowered with recent advances in SiGe, III-V semiconductor technology and deeply scaled CMOS.

The technical approach of this project is to exploit complete co-design of the modulation strategy with a new power amplifier concept: Asymmetric Multilevel Outphasing (AMO) [1]. This architecture combines the best properties of polar transmitters and outphasing (LINC) transmitters [5]. The power amplifier's efficiency is improved without significantly degrading its linearity by using the combination of drain voltage modulation and rapid outphasing. A key aspect of this project will be the investigation of energy recovery as a means of further improving the transmitter's efficiency. The use of resistance compression networks [3] as a means of recovering the energy normally lost during outphasing will be critical. To achieve these goals, the most significant research challenges are:

1. achieving baseband modulation commensurate with 10 Gb/s transmission with the new AMO architecture and
2. designing a symbol constellation and modulation strategy that maximally exploits the architecture.

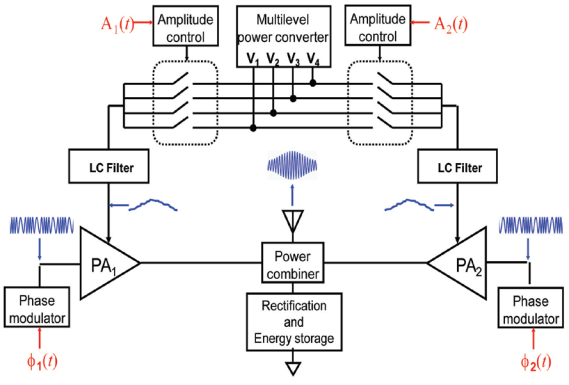


FIGURE 1: System diagram of the Asymmetric Multilevel Outphasing PA. The energy recovery network and amplitude path will be designed to function at a 60 GHz carrier frequency and 10 Gb/s data rate.

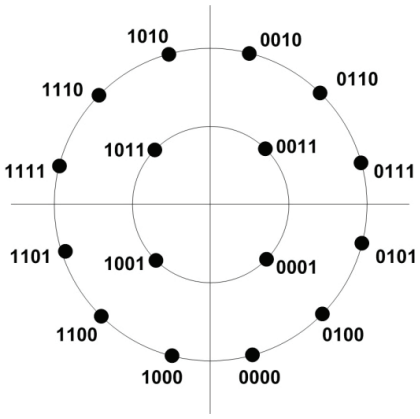


FIGURE 2: Constellation diagram for 16-APSK [4]. This constellation is a potentially suitable modulation scheme because it requires just two amplitude levels.

REFERENCES

[1] S-W Chung, P. A. Godoy, T. W. Barton, E.W. Huang, D. J. Perreault and J. L. Dawson, "Asymmetric Multilevel Outphasing Architecture for Multi-standard Transmitters," IEEE Radio-Frequency Integrated Circuits (RFIC) Symposium, pp. 237-240, June 2009.

[2] C. H. Doan, S. Emami, D. Sobel, A. M. Niknejad, and R.W. Brodersen, "60 GHz CMOS radio for Gb/s wireless LAN," IEEE Radio Frequency Integrated Circuits (RFIC) Symposium, pp. 225-228, June 2004.

[3] Y. Han, O. Leitermann, D. A. Jackson, J. M. Rivas and D. J. Perreault, "Resistance Compression Networks for Radio-Frequency Power Conversion," IEEE Transactions on Power Electronics, Vol. 22, No. 1, pp. 41-53, Jan. 2007.

[4] R. De Gaudenzi, A. G. Fabregas and A. Martinez, "Turbo-coded APSK modulations design for satellite broadband communications," International Journal of Satellite Communications and Networking, Vol. 24, pp. 261-281, 2006.

[5] D. C. Cox, "Linear Amplification with Nonlinear Components," IEEE Transactions on Communications, Vol. 22, No. 12, pp. 1942-1945, Dec. 2004.

A Distributed Power-management Integrated Circuit Based on Ultracapacitors

W. Sanchez, J. L. Dawson
Sponsorship: Gates Millennium Scholars Graduate Fellowship

Presently, continuous monitoring of patients is very difficult and typically intrudes greatly on their lifestyles and daily routines. Methods that rely on patients measuring themselves are unreliable. An unobtrusive, minimally invasive monitoring platform would give medical scientists unprecedented access to continuous long-term data on patients. In this work, we develop a power management integrated circuit (IC) to power minimally invasive monitors using ultracapacitors. The focus of the project is to improve the evaluation and treatment of patients with a variety of movement disorders including Parkinson's disease, restless legs syndrome, and essential tremor by allowing doctors to continuously monitor relevant biomarkers over much longer time scales and with better precision than currently possible.

Because of the strict size requirements of a minimally invasive IC, a simple battery cannot be used due to the area overhead and replacement requirements. As a solution, a wirelessly rechargeable ultracapacitor network can be used as the power supply for sensing and data conversion, storage, and transmission circuitry.

Ultracapacitors can carry 5-10% the energy densities of conventional battery chemistries of comparable weight [3]. With over 10^5 recharge cycles possible, they are attractive candidates for implantable applications employing efficient wireless recharging schemes. Figure 1 is a block diagram for the power management IC. Discrete ultracapacitors from Maxwell (5F, 14mmx24mmx0.5mm) are used in the initial prototype. Figure 2 demonstrates the principle of operation that achieves use of 96.8% of the initial charge. Currently, a prototype whereby the ultracapacitors are recharged using RF rectification is under development.

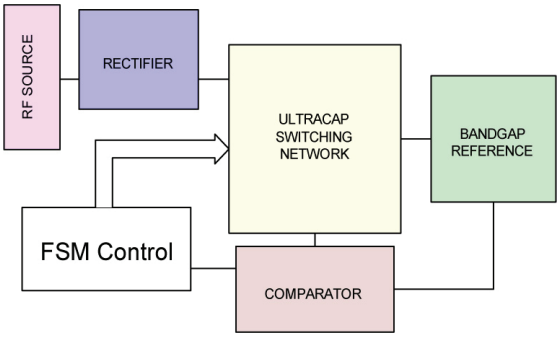


FIGURE 1: Block diagram of power management integrated circuit.

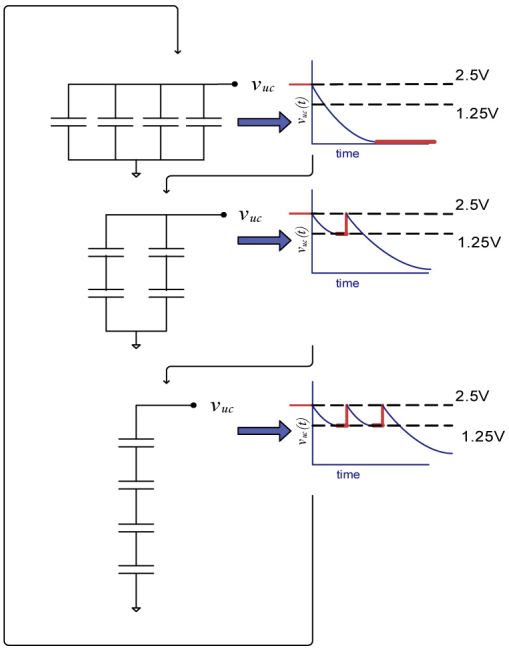


FIGURE 2: Operating principle of ultracapacitor stacking network. Three-step stacking maintains a voltage adequate for circuit operation, utilizing 96.8% of the initial charge stored on the ultracapacitors.

REFERENCES

[1] Nesscap Ultracapacitor - Technical Guide, Nesscap Co., Ltd., 2008

An Ultra-high-speed Zero-crossing-based ADC

A. Chow, H.-S. Lee
Sponsorship: SRC/FCRP C2S2

With an increasing need for higher data rates, both wireless applications and data links are demanding higher speed analog-to-digital converters (ADC) with medium resolution. This work will investigate ADCs with a sampling rate up to 2 Gs/s with 6-8 bits of resolution. Time-interleaved converters achieve their high sampling rate by placing several converters in parallel. Each individual converter, or channel, has a delayed sampling clock and operates at a reduced sampling rate. Therefore, each channel is responsible for digitizing a different time slice. This method requires that the individual converters, which make up the parallel combination, be matched. Mismatches and non-idealities such as gain error, timing error, and voltage offset degrade the performance. Hence channel matching is an important design consideration for time-interleaved ADCs.

Although digital calibration can mitigate many of these non-idealities, a timing mismatch is a non-linear error that is more difficult to remove. At sampling rates up to 2Gs/s, digital calibration would consume a large amount of power. An alternative solution uses a global switch running at the full speed of the converter. Although this technique works reasonably well for medium-high speed ADC's [1], [2], its effectiveness is limited by parasitic capacitance. We have developed a double-global sampling technique to remove the effect of parasitic capacitance on the timing skew. At higher speeds the ability to turn the switch on and off at the full sampling rate becomes a major challenge. The use of scaled CMOS technology and gate-boosted switches still enables multi-GHz input bandwidth.

In this work, we employ a fast, single-slope architecture (Figure 1). Since the single-slope architecture is more sensitive to non-idealities such as ramp nonlinearity, the design uses several innovative ideas to improve the linearity. Offset cancellation is also incorporated in the design. The first silicon fabricated in a 90-nm CMOS technology has been received and is being characterized.

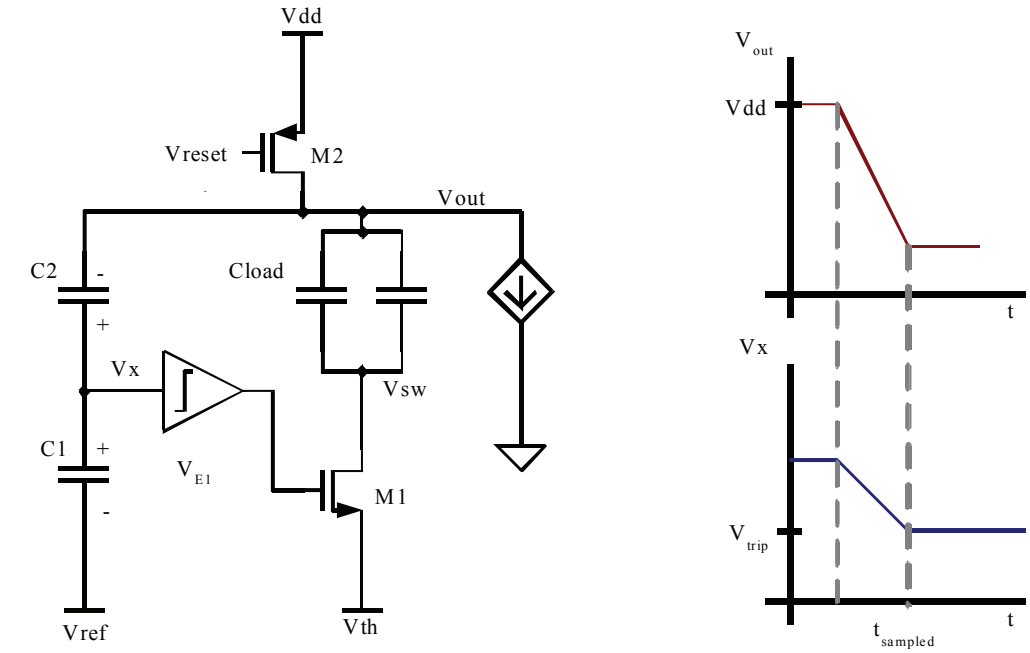


FIGURE 1: One stage of a single-slope CBSC-based pipelined ADC.

REFERENCES

[1] M. Gustavsson and N. N. Tan, "A global passive sampling technique for high-speed switched-capacitor time-interleaved ADCs," *Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on*, vol. 47, pp. 821-831, 2000.

[2] S. Gupta, M. Choi, M. Inerfield and Jingbo Wang, "A 1GS/s 11b Time-Interleaved ADC in 0.13/ spl mu/m CMOS," *Solid-State Circuits Conference, 2006. ISSCC 2006. Digest of Technical Papers. IEEE International*, pp. 2360-2369, 2006.

A High-performance Zero-Crossing-based Pipeline ADC

J. Chu, H.-S. Lee
Sponsorship: SRC/FRCP C2S2

In this work, we are designing a high-performance pipeline ADC using a Zero-crossing-based (ZCB) structure [1]. The ZCB circuits offer many advantages compared with the earlier comparator-based switch-capacitor circuits (CBSC) [2]. The focus of the project is to explore novel circuit structures for ZCB circuits to improve the speed and accuracy as well as the figure-of-merit (FOM). In particular, we employ a fully-differential structure to improve ZCBC's robustness against common mode noise. An additional benefit of differential design is the increase in the available signal range, which helps to improve SNR. We implemented a multi-bit MDAC to improve its power-efficiency and to help relax component accuracy requirements. In this design, we used dynamically biased current sources to achieve high linearity at high operating frequencies. Dynamic biasing can be used to compensate for nonlinearity of the ramp to improve the linearity of the system.

A prototype chip has been fabricated, and the preliminary measurement data indicates a better-than-10 effective number of bits (ENOBs) at 100MHz sampling rate. More tests are currently being performed.

In the next iteration of this project, time-interleaving will be used to achieve ultra-high sampling rates with very low power. In a time-interleaved structure, matching between the different channels will be very important to maintain the desired performance. Any mismatch in gain, offset, and timing can greatly degrade the performance. We plan to use sample-time adjustment to mitigate the timing errors. Careful design and layout will be needed to reduce the other mismatches.

REFERENCES

[1] L. Brooks and Hae-Seung Lee, "A Zero-Crossing-Based 8b 200MS/s Pipelined ADC," *Solid-State Circuits Conference, 2007. ISSCC 2007. Digest of Technical Papers. IEEE International,* pp. 460-615, 2007.

[2] T. Sepke, J. K. Fiorenza, C. G. Sodini, P. Holloway and Hae-Seung Lee, "Comparator-based switched-capacitor circuits for scaled CMOS technologies," *Solid-State Circuits Conference, 2006. ISSCC 2006. Digest of Technical Papers. IEEE International,* pp. 812-821, 2006.

[3] M. Gustavsson and N. N. Tan, "A global passive sampling technique for high-speed switched-capacitor time-interleaved ADCs," *Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on,* vol. 47, pp. 821-831, 2000.

[4] S. Gupta, M. Choi, M. Inerfield and Jingbo Wang, "A 1GS/s 11b Time-Interleaved ADC in 0.13/ spl mu/m CMOS," *Solid-State Circuits Conference, 2006. ISSCC 2006. Digest of Technical Papers. IEEE International,* pp. 2360-2369, 2006.

A Low-voltage Zero-crossing-based Delta-Sigma ADC

M. Guyton, H.-S. Lee
Sponsorship: CICS

Many analog signal-processing circuits use operational amplifiers (op-amps) in a negative feedback topology. The error in these feedback systems is inversely proportional to the gain of the op-amp. Because scaled CMOS technologies use shorter channel lengths and require lower power supply voltages, it becomes more difficult to implement high gain op-amps. Recently, a comparator-based switched-capacitor (CBSC) technique was proposed [1] that uses a comparator rather than an op-amp to implement switched-capacitor topologies. This technique was generalized to the use of zero-crossing detectors [2].

In this project, we investigate very-low-voltage delta-sigma converters. One of the biggest challenges of low-voltage circuits is the transmission gates that must pass the signal. If the signal is near the middle of the power supply range, neither the NMOS nor the PMOS transistor has sufficient gate drive to pass the signal properly. The switched-op-amp technique [3] was proposed to mitigate this problem. In this technique, the output of the op-amp is directly connected to the next sampling capacitor without a transmission gate to perform charge transfer.

During the charge-transfer phase, the op-amp is switched off, and the output is grounded.

Much like the standard switched-capacitor technique, zero-crossing-based (ZCB) circuits use two-phase clocking, having both sampling and charge-transfer clock phases. Unlike in a standard switched-capacitor circuit, in a ZCB circuit all current sources connected to the output node are off at the end of the charge-transfer phase. Therefore, there is no op-amp or current source to turn off to accommodate the charge transfer without a transmission gate. Thus, the ZCB technique is inherently better suited to low-voltage applications than are switched-op-amp circuit topologies. Figure 1 shows a fully-differential low-voltage ZCB integrator stage using the combined techniques. We have designed a fourth-order delta-sigma ADC for operation at 1-V power supply using this integrator stage for audio-band applications. A new output pre-sampling technique has been developed to dramatically reduce the linearity requirement of the ramp waveform. The chip fabricated in 130-nm CMOS is currently being tested.

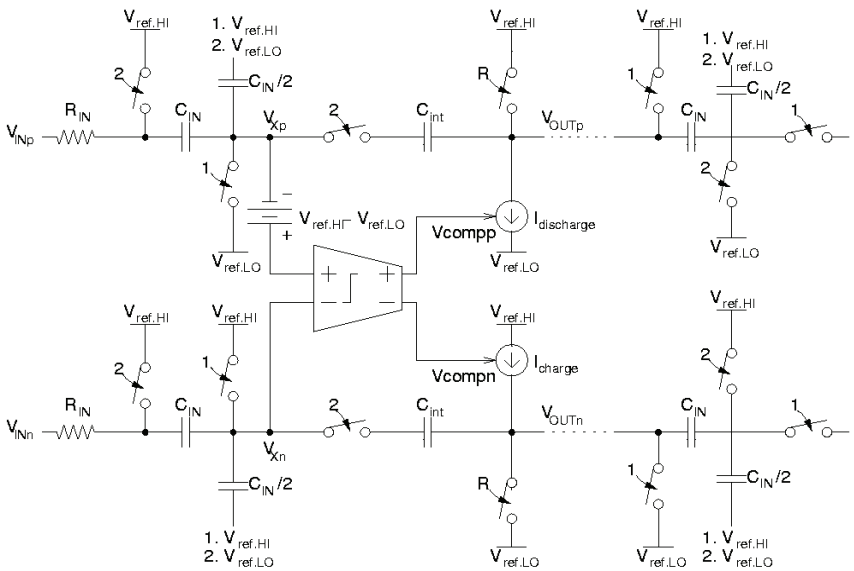


FIGURE 1: Fully-differential zero-crossing-based switched-capacitor integrator. The input of the next integrator stage is also shown.

REFERENCES

[1] T. Sepke, J.K. Fiorenza, C.G. Sodini, P. Holloway, and H.S. Lee, "Comparator-based switched-capacitor circuits for scaled CMOS technologies," *2006 IEEE ISSCC Digest of Technical Papers*, Feb. 2006, p. 220.

[2] L. Brooks and H.S. Lee, "A zero-crossing-based 8b, 200 MS/s pipelined ADC," *2007 IEEE ISSCC Digest of Technical Papers*, Feb. 2007, pp.460-461.

[3] J. Crols and M. Steyaert, "Switched-op-amp: an approach to realize full CMOS switched-capacitor circuits at very low power supply voltages," *IEEE Journal of Solid-State Circuits*, vol. 29, no. 8, pp. 936-942, Aug. 1994.

Design of a Reconfigurable Mixed-Signal System

P. Lajevardi, A. P. Chandrakasan, H.-S. Lee
Sponsorship: CICS

Switched-capacitor circuits can be used to implement many analog systems such as ADCs, DACs, filters, amplifiers, and integrators. In earlier phase of this research, a reconfigurable switched-capacitor system is proposed to implement different analog systems. A prototype system has been fabricated that shows basic reconfigurability to implement a pipe-lined ADC and a switched-capacitor filter. A second prototype system is being designed that utilizes highly reconfigurable blocks. Figure 1 shows the block diagram of such systems. The building blocks have the same functionality and can be programmed to implement a multiplier or an integrator with a reconfigurable coefficient. Such a system has many applications such as in software-defined radios and rapid prototyping of analog circuits.

The design of such systems has had limited success since many different op-amp topologies are required to cover a large performance and configuration space. Recently, [1] and [2] proposed zero-crossing based (ZCB) circuits to design ADCs. ZCB circuits replace the op-amp in traditional switched-capacitor circuits with a combination of a current source and a zero-crossing detector. ZCB circuits are well suited for highly reconfigurable system since their power consumption scales with the operating frequency and required SNR. In addition, ZCB circuits benefit from technology scaling due to their more digital circuit-like operation in contrast to conventional op-amp based circuits.

The system is designed to operate at different speeds while the power consumption is kept at the optimum level. A key challenge in design of this system is to keep the cost of programmability low in terms of additional power consumption and performance degradation. Several innovative circuit techniques have been used to address this issue.

REFERENCES

[1] T. Sepke, J. Fiorenza, C.G. Sodini, P. Holloway, and H.-S Lee, "Comparator-based switched-capacitor circuits for scaled CMOS technologies," in *IEEE International Solid-State Circuits Conference Digest of Technical Papers*, San Francisco, CA, Feb. 2006, pp.220-221.

[2] L. Brooks and H.-S. Lee, "A zero-crossing-based 8b 200MS/S pipeline ADC," in *IEEE International Solid-State Circuits Conference Digest of Technical Papers*, San Francisco, CA, Feb. 2007, pp. 460-461.

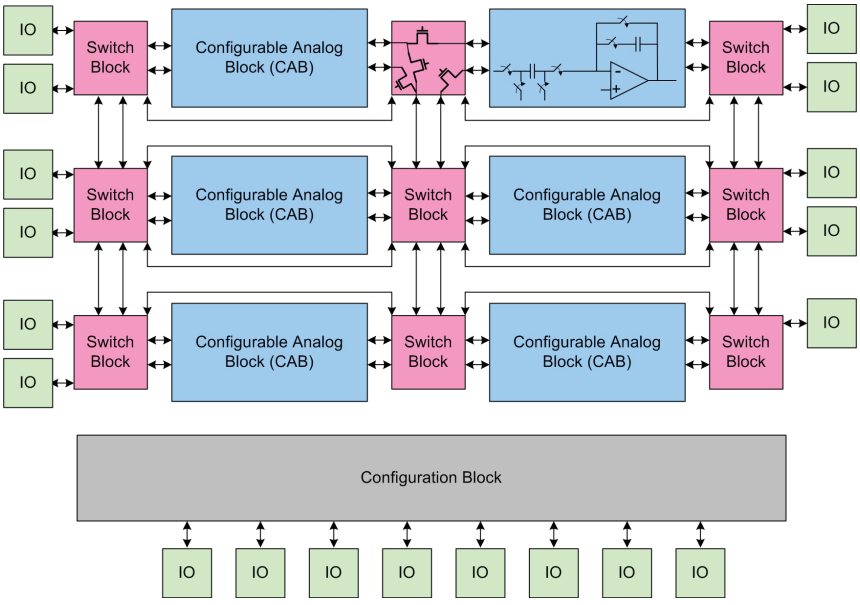


FIGURE 1: Block diagram of reconfigurable zero-crossing-based analog circuits. Each configurable analog block can be programmed to perform an integration or multiplication. The connection of blocks is also programmable.

Front-end Design for Portable Ultrasound Systems

S. Lee, A. P. Chandrakasan, H.-S. Lee
Sponsorship: Samsung Fellowship, CICS

Most current ultrasound imaging systems use piezoelectric materials for the ultrasound transducer. The recent development of micro-electromechanical systems (MEMS) allowed fabrication of capacitive micromachined ultrasound transducers (CMUTs). A CMUT is a micromachined capacitor whose value changes according to the DC bias voltage or external pressure due to the physical deformation of the top plate by electrostatic force or external pressure. The major advantages of this transducer technology are the potential for integration with supporting electronic circuits, ease of fabrication, higher resolution due to small transducer size, and improved bandwidth and sensitivity [1].

This project focuses on the front-end design of portable ultrasound systems using CMUTs. Figure 1 presents a conceptual block diagram of the system. Implementing an ADC at each channel input makes possible digital beam-forming in the receive (Rx) path, which enhances ultrasound image quality. To implement as many ADCs as the number of transducer channels, each ADC must consume as little power as possible, and each should be implemented in a small area. With the performance requirements at 10~20MHz sampling frequency with 8~10bits of resolution, successive approximation or zero-crossing-based (ZCB) ADC are good candidates [2]. We are investigating these topologies to determine the optimum topology for the application. We are also exploring the control of the fire timing and pulse shape of the transmit (Tx) elements, such that beam-forming in the Tx path is possible to give a larger Rx signal.

Recently, a few 2D imaging systems using CMUT as ultrasound transducers have been reported, but they do not use real-time imaging [1]. The digital image processing block will be considered in the system level for real-time imaging. After completing the 2D ultrasound image system using a 1D transducer, we will examine the feasibility of the 3D ultrasound image system using 2D transducers.

REFERENCES

[1] O. Oralkan, "Acoustical Imaging Using Capacitive Micromachined Ultrasonic Transducer Arrays: Devices, Circuits, and systems", Ph.D. thesis, Stanford University, 2004.

[2] L. Brooks and H.-S. Lee, "A Zero-Crossing-Based 8b 200MS/s Pipelined ADC," *Solid-State Circuits Conference, 2007. ISSCC 2007. Digest of Technical Papers. IEEE International*, pp. 460-615, 2007.

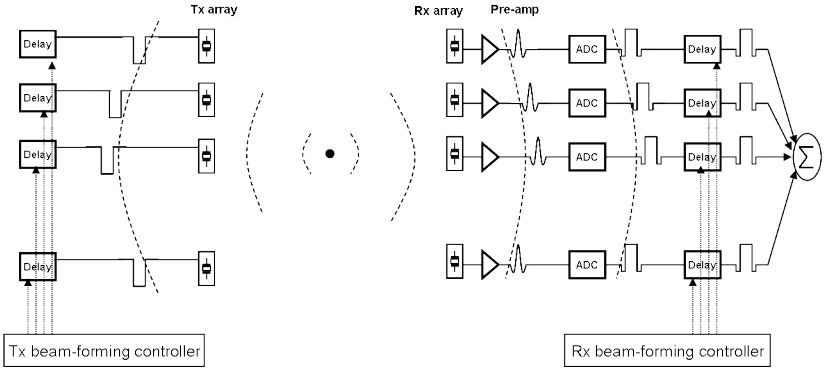


FIGURE 1: system block diagram

A High-accuracy, Zero-crossing-based Pipeline ADC

M. Markova, P. Holloway, H.-S. Lee
Sponsorship: CICS

Technology scaling poses challenges in designing analog circuits because of the decrease in intrinsic gain and reduced swing. An alternative to using high-gain amplifiers in the implementation of switched capacitor circuits has been proposed [1] that replaces the amplifier with a current source and a comparator. The new comparator-based switch capacitor (CBSC) and zero-crossing-based circuit (ZCBC) techniques have been implemented in two pipelined ADC architectures at 10MHz and 200MHz and 10-bit and 8-bit accuracy, respectively [1], [2].

The purpose of this project is to explore the use of the ZCBC technique for very-high-precision AD converters. The goal of the project is a 100MHz, 14-bit pipelined ADC. First, we are investigating dual-phase hybrid ZCBC operation to improve the power-linearity trade off of the A/D conversion [3] and to improve the power supply rejection. The first phase approximates the final output value, while the second phase allows the output to settle to its accurate value. Since the output is allowed to settle in the second phase, the currents through capacitors decay, permitting higher accuracy and power-supply rejection compared with standard ZCBCs. We are also developing linearization techniques for the ramp waveforms. Linear ramp waveforms require less correction in the second phase for given linearity, thus allowing faster operation. Innovative techniques for improving linearity beyond using a cascoded current source are explored, including output pre-sampling. In addition, overshoot reduction techniques will be used to improve the linearity requirements of the final phase. Alternatively, improvements in the zero-crossing detector design are pursued to lessen the linearity requirement of the ramp. Chopper stabilization will be used to reduce the effects of offsets and flicker noise.

REFERENCES

[1] T. Sepke, J.K. Fiorenza, C.G. Sodini, P. Holloway, and H.-S. Lee, "Comparator-based switched capacitor circuits for scaled CMOS technologies," *IEEE Journal of Solid State Circuits, IEEE International Solid State Circuits Conference Digest of Technical Papers*, February 2006, pp 220-221.

[2] L. Brooks, H.-S. Lee, "A zero-crossing based 8b 200MS/s pipelined ADC," *IEEE International Solid State Circuits Conference Digest of Technical Papers*, February 2007, pp 460-461.

[3] J.K. Fiorenza, "A comparator-based switched –capacitor pipelined analog-to-digital converter ," Ph.D. thesis, Massachusetts Institute of Technology, Cambridge, 2007.

Machine Vision for an Intelligent Transportation System

Y. Fang, B. K. P. Horn, I. Masaki
Sponsorship: Intelligent Transportation Research Center, MTL

Environment-understanding technology is very vital for intelligent vehicles that are expected to respond automatically to fast- changing environments and dangerous situations. To obtain perceptual abilities, we should automatically detect static and dynamic obstacles and obtain related information such as their locations, speed, possible collision or occlusion, and other dynamic current or historic information. Conventional methods independently detect individual information, which is normally noisy and not very reliable. Instead we propose fusion-based and layered-based information-retrieval methodology as shown in Figure 1 to systematically detect obstacles and obtain their location/timing information for visible and infrared sequences. The proposed obstacle detection methodologies take advantage of the connections between different pieces of information and increase the computational accuracy of obstacle information estimation, thus improving environment understanding abilities and driving safety. Three examples are shown in Figures 2, 3 and 4.

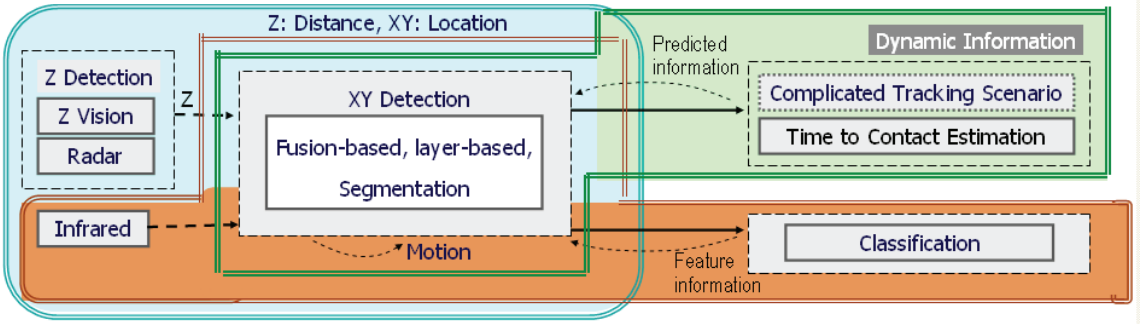


FIGURE 1: Segmentation result for urban day-time driving environment.

FIGURE 2: Segmentation result for urban day-time driving environment.

FIGURE 3: Segmentation result for night driving environment.

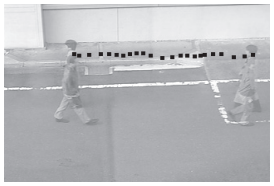


FIGURE 4: The segmentation/ tracking results before and after two people intersect.

REFERENCES

[1] Y. Fang, S. Yokomitsu, B. Horn, I. Masaki, "A Layered-based Fusion-based Approach to Detect and Track the Movements of Pedestrians through Partially Occluded Situations," to be presented at the *IEEE Intelligent Vehicles Symposium 2009 (IV2009)*.

[2] B. Horn, Y.Fang, I.Masaki, "Hierarchical framework for direct gradient-based time-to-contact estimation," to be presented at the *IEEE Intelligent Vehicles Symposium 2009 (IV2009)*.

[3] Y. Fang, B. K. P. Horn and I. Masaki, "Systematic information fusion methodology for static and dynamic obstacle detection in ITS," presented at *15th World Congress on Intelligent Transport Systems*.

[4] B. K. P. Horn, Yajun Fang and I. Masaki, "Time to Contact Relative to a Planar Surface," *Intelligent Vehicles Symposium, 2007 IEEE*, pp. 68-74, 2007.

[5] S. Negahdaripour and B. K. P. Horn, "Direct Passive Navigation," *Pattern Analysis and Machine Intelligence, IEEE Transactions on*, vol. PAMI-9, pp. 168-176, 1987.

[6] B. K. P. Horn and E. J. Weldon, "Direct Methods for Recovering Motion," *International Journal of Computer Vision*, vol. 2, pp. 51-76, 06/01. 1988.

[7] Y. Fang, K. Yamada, Y. Ninomiya, B. Horn and I. Masaki, "Comparison between infrared-image-based and visible-image-based approaches for pedestrian detection," *Intelligent Vehicles Symposium, 2003. Proceedings. IEEE*, pp. 505-510, 2003.

[8] Y. Fang, K. Yamada, Y. Ninomiya, B. K. P. Horn and I. Masaki, "A shape-independent method for pedestrian detection with far-infrared images," *Vehicular Technology, IEEE Transactions on*, vol. 53, pp. 1679-1697, 2004.

Power-efficient Impedance-modulation Wireless Data Links for Biomedical Implants

S. Mandal, D. P. Kumar, R. Sarpeshkar

Low-power wireless links are important for the development of long-term implantable neural prostheses. Furthermore, in implanted systems with many neural recording electrodes, the data rate of the wireless link will need to be quite high since each electrode typically requires at least 5kHz of bandwidth. For low-power operation, inductively-coupled near-field wireless links have shown great promise and were used to develop a power-efficient data link for biomedical implants.

A bidirectional half-duplex wireless link that uses near-field inductive coupling between the implanted system and an external transceiver was designed in a 0.5-μm CMOS process. Our system minimizes power consumption in the implanted system by using impedance modulation to transmit high-bandwidth information in the uplink direction, i.e., from the implanted to the external system. We measured a data rate of 2.8Mbps at a bit error rate (BER) of $<10^{-5}$ (we could not measure error rates below 10^{-5}) and a data rate of 4.0Mbps at a BER of 10^{-3}. Experimental results also demonstrate data transfer rates up to 300kbps in the opposite, i.e., downlink direction. Theoretical analysis of the bit error rate performance was also carried out. This analysis allowed us to theoretically predict and experimentally verify an important effect regarding the asymmetry of rising and falling edges that is inherent in impedance modulation and that contributes to bit errors. The link dissipates 2.5mW in the external system and only 100μW in the implanted system, making it among the most power-efficient inductive data links reported. Our link is compatible with FCC regulations on radiated emissions.

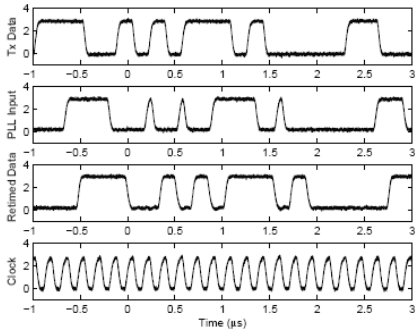


FIGURE 1: Uplink data transmission at 5.8Mbps with the coils 2cm apart.

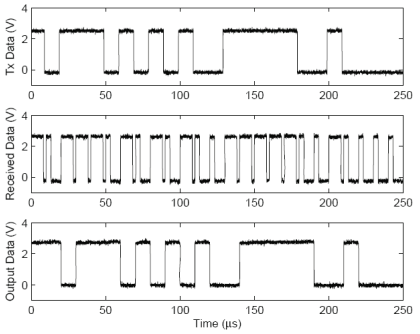


FIGURE 2: Downlink data transmission at 200kbps with the coils 2cm apart.

REFERENCES

[1] S. Mandal and R. Sarpeshkar, "Power-Efficient Impedance-Modulation Wireless Data Links for Biomedical Implants," *Biomedical Circuits and Systems, IEEE Transactions on,* vol. 2, pp. 301-315, 2008.

Low-power Circuits for Brain-machine Interfaces

R. Sarpeshkar, W. Wattanapanitch, S. Arfin, B. Rapoport, S. Mandal, M. Baker, M. Fee, S. Musallam, R. Andersen

Large-scale chronic multi-electrode neural recording and stimulation systems have emerged as an important experimental paradigm for investigating brain function. Experiments using such brain-machine interfaces (BMIs) have shown that it is possible to predict intended limb movements by analyzing simultaneous recordings from many neurons. These findings have suggested a potential approach for treating paralysis and other disorders and disabilities in humans. Chronic use of BMIs with large numbers of electrodes requires ultra-low-power operation so that the systems are miniature and implantable, heat dissipated in the brain is minimized, and repeated surgeries for battery replacement are unnecessary.

Currently, we are developing an ultra-low-power BMI system with applications for paralysis prosthetics, stroke, Parkinson's disease, epilepsy, prosthetics for the blind, and experimental neuroscience systems [1]. Our proposed system consists of a wireless hybrid analog-digital recording system that is capable of recording from neurons in the brain and a wireless neural stimulation system. Figure 1 shows an overall architecture of the recording system. It consists of low-power DAC-programmable analog circuits that are configured by external DSP. Depending on the user's choice, the system can be configured to report raw neural data from a selected set of electrodes, local field potential (LFP) data, or decoded motor parameters via a data telemetry uplink. Figure 2 shows the wireless neural stimulation system. The system consists of an external transmitter (not shown) controllable through a computer interface and a miniature, implantable wireless receiver-and-stimulator. The entire stimulation system weighs 0.6 g, occupies a footprint smaller than 1.5 cm2, and is capable of delivering biphasic current pulses to 4 addressable electrode sites at 32 selectable current levels ranging from 10 uA to 1 mA.

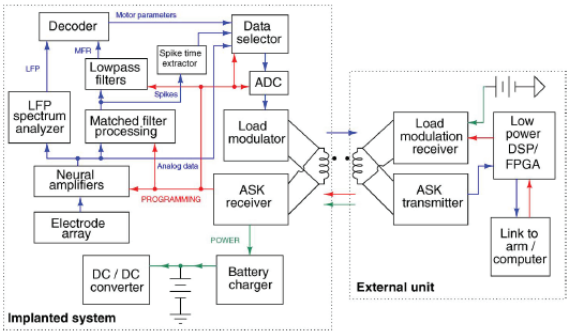


FIGURE 1: Block diagram of the hybrid analog-digital brain-machine interface system.

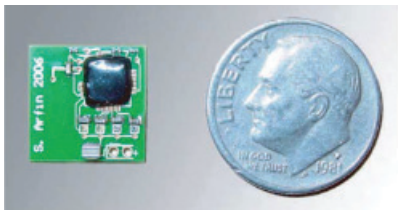


FIGURE 2: Protograph of the chip-on-board wireless neural stimulation system.

REFERENCES

[1] R. Sarpeshkar *et al*, "Low-Power Circuits for Brain-Machine Interfaces," *IEEE Transactions on Biomedical Circuits and Systems*, pp 173-183, Sept. 2008.

An Organic Thin-film Transistor Circuit for Large-area Temperature-sensing

D. He, I. Nausieda, K. Ryu, A. I. Akinwande, V. Bulović, C. G. Sodini
Sponsorship: SRC/FCRP C2S2, Hewlett-Packard, NSERC Fellowship

The organic thin-film transistor (OTFT) is a field-effect transistor technology that uses organic materials as the semiconductor. OTFTs have field-effect mobilities that are comparable to those of hydrogenated amorphous silicon TFTs, and OTFTs are compatible with large-area and mechanically-flexible substrates [1], [2]. The goal of this work is to demonstrate an integrated OTFT temperature-sensing circuit suitable for large-area and flexible substrates.

As shown in Figure 1, two important differences are observed between the OTFT's and the MOSFET's current-voltage characteristics when temperature is varied. First, the OTFT's current increases with temperature in both subthreshold and above-threshold regimes, whereas the MOSFET's above-threshold current decreases with temperature. Second, the OTFT's subthreshold slope is temperature independent over the measured range of -20 to 60°C, while the MOSFET's subthreshold slope is proportional-to-absolute-temperature (PTAT).

Because of these differences in temperature response, the OTFT temperature-sensing "ΔV_{BE} circuit" (Figure 2a) has a complementary-to-absolute-temperature (CTAT) response instead of an equivalent silicon circuit's PTAT response. The OTFT circuit is scaled to an array format to enable surface thermal sensing applications. As Figure 2b shows, the array consists of 3x3 temperature-sensing circuit cells of 1mm² each and is currently being characterized.

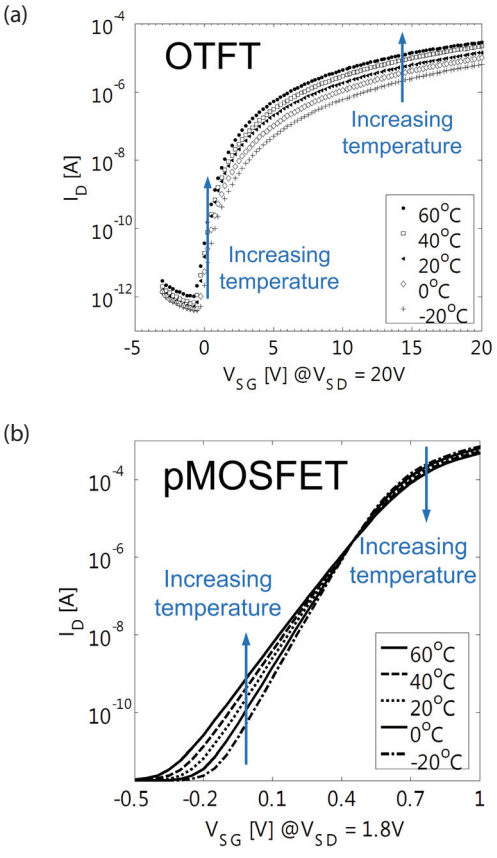


FIGURE 1: (a) The OTFT's (measured) and (b) pMOSFET's (BSIM3) current-voltage characteristics versus temperature.

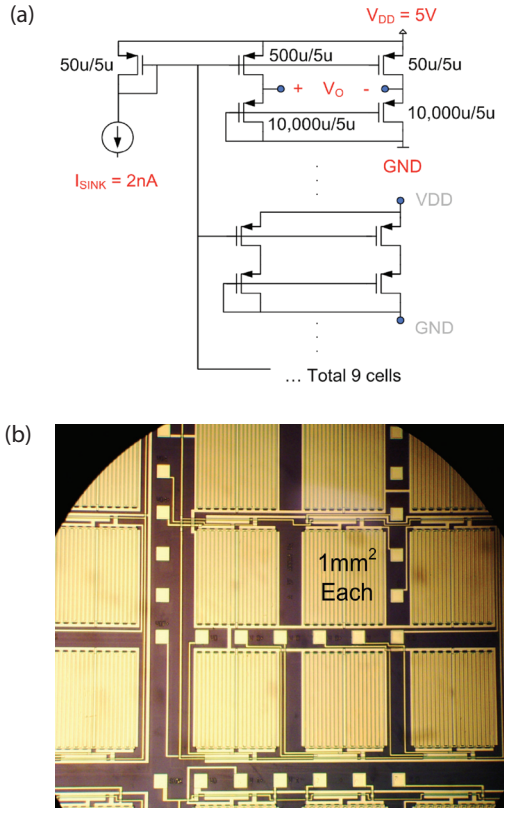


FIGURE 2: (a) The CTAT circuit array schematic and (b) die photo.

REFERENCES

[1] Y.Y. Lin, D.J. Gundlach, and T.N. Jackson, "High-mobility pentacene organic thin film transistors," *Device Research Conference Digest*, June 1996, pp. 80–81.

[2] I. Kymissis, C.G. Sodini, A.I. Akinwande, and V. Bulović, "An organic semiconductor based process for photodetecting applications," *IEEE International Electron Devices Meeting Technical Digest*, Dec. 2004, pp. 377–380.

Digital Phase-tightening for Millimeter-wave Imaging

K.M. Nguyen, C.G. Sodini
Sponsorship: SRC/FCRP C2S2

Millimeter-wave (MMW) imaging has potential applications such as collision-avoidance radar at 77GHz and concealed-weapons detection at 77GHz, 94GHz, and higher. This research investigates the challenges of designing an MMW imaging system. We envision an active imaging receiver that will consist of an array of 1000 antenna and per-antenna processor (PAP) units with an operating frequency of 77GHz [1]. Each PAP has digital logic that will estimate the phase and amplitude and reduce the data rate to the order of a kilohertz. A central processing unit (CPU) will perform digital beam-forming on the aggregated data from the array to achieve an expected frame rate of 10 fps. The 77-GHz input signal will be down-converted by a mixer with a 76-GHz local oscillator, generated by a PLL, to obtain an intermediate frequency (IF) of 1GHz. This signal is digitized by an analog-to-digital converter that is operating at 4.75GHz and is sent to the CPU.

Key blocks in the PAP being explored are the 76-GHz PLL and 4.75-GHz DLL. Since accurate beam-forming requires precise control of the phase over the array of elements, the PLL will be designed for minimal phase noise and power dissipation. The 76-GHz VCO used in the PLL is a cross-coupled LC tank design. The divider chain consists of nine divide-by-2 static frequency dividers created in emitter-coupled logic for the first six stages and CMOS logic for the lowest three stages. The highest frequency divider utilizes inductive peaking for increased operating frequency. A full PLL was designed in a 130-nm BiCMOS process. Test results showed a free-running oscillation frequency of 70GHz and gave improved understanding between modeling and experimental results. The next chip will contain a revised PLL and a phase tightening system, which will consist of a DLL, ADC, and digital logic to estimate the phase data. The ADC is clocked by the DLL, which outputs a clock signal at each of its delay cells. The phase-tightening system locks onto the IF signal's zero crossings by continually selecting the DLL output to clock the ADC.

REFERENCES

[1] A. Accardi, "Digital Compensation in Imaging Systems," Dissertation proposal, Massachusetts Institute of Technology, Cambridge, 2007.

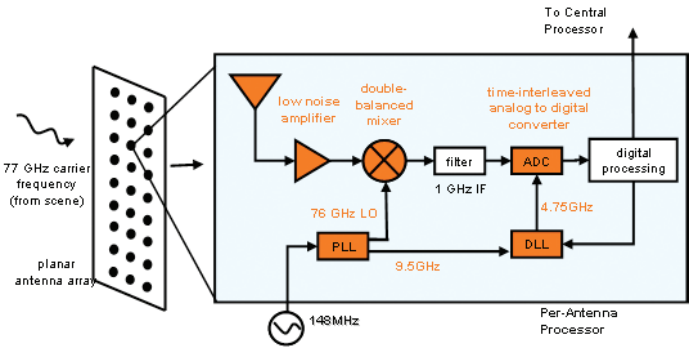


FIGURE 1: Block diagram of the MMW imaging system.

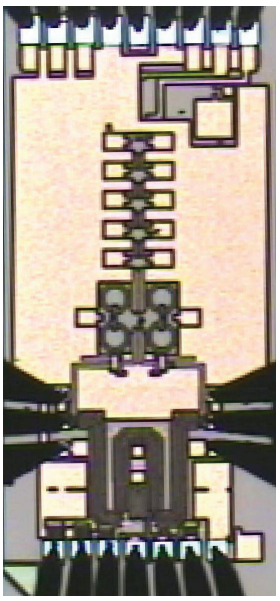


FIGURE 2: Die photo of 76-GHz PLL with on-wafer test probes.

Flip-chip Integrated Wideband Antennas for Millimeter-wave Passive Imaging

J. D. Powell, C. G. Sodini
Sponsorship: SRC/FCRP C2S2

The area of Millimeter-wave (MMW) system research and design has become increasingly popular in recent years, as advanced silicon processes have enabled integrated circuit operation in the MMW regime. Several applications exist for MMW design, including wireless communications at 60-GHz, collision-avoidance radar imaging at 77-GHz, and concealed-weapons detection imaging at 94-GHz and higher. This research focuses on a passive imager front-end that has been developed and tested for the application of concealed-weapons detection.

A key component of this research involves the design of a packaged antenna. A wideband Vivaldi-type design is used to achieve high gain and efficiency from 73-GHz to 105-GHz. The antenna was fabricated on a low-conductive dielectric constant material, RO4350B, at the MIT EML Laboratory. It is packaged onto the LNA bondpad terminals via gold solder bumps and silver epoxy and placed to maximize the distance from the die's ground plane. The antenna has a gain of approximately 8dB within the operating bandwidth and a typical efficiency of 80% [1],[2].

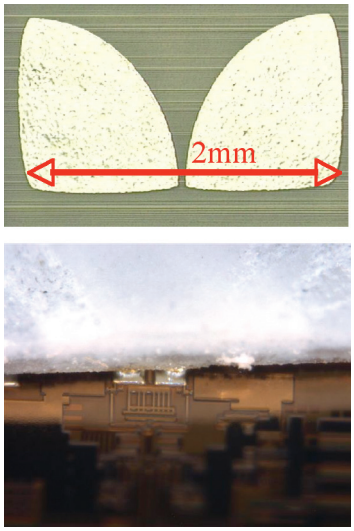


FIGURE 1: Photo of fabricated antenna and antenna mounted on LNA die using gold solder bumps.

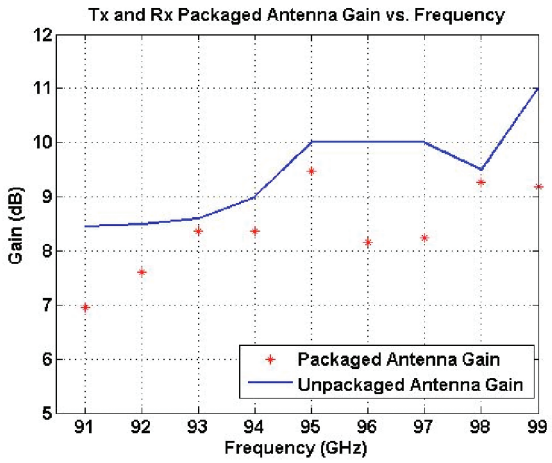


FIGURE 2: Measurement results for packaged versus unpackaged antenna gain.

REFERENCES

[1] J. D. Powell, "SiGe Receiver Front Ends and Flip-Chip Integrated Wideband Antennas for Millimeter-wave Passive Imaging," Ph.D. dissertation, Massachusetts Institute of Technology, Cambridge, 2008.

[2] J. D. Powell, H. Kim, and C. G. Sodini, "SiGe Receiver Front Ends for Millimeter-wave Passive Imaging," IEEE Transactions on Circuit Systems-I, vol. 56, no. 3, pp. 541-553, March 2009.

A Leadless, Long-term ECG Monitor for In-home Use

E. Winokur, C. G. Sodini

Sponsorship: Texas Instruments

With the escalating costs of hospital visits, clinicians are opting to use at-home monitoring devices to diagnose patients. Current ECG Holter monitoring devices typically have 24 - 48 hour memory and battery capacity [1]. With many patients experiencing intermittent heart problems that can occur once every week – month, the Holter monitor is not a good solution and an event recorder or loop recorder is required [2]. However, each of these recorders can only save up to a few minutes of ECG recordings. This leads to the loss of most of the data, which could be very important in alerting the user for the onset of future episodes. Therefore, we have developed a Holter monitor prototype with the goal of battery and memory capacity of two weeks. Fig. 1 shows a block diagram of the system.

We based the long-term monitor prototype around a Texas Instruments MSP430 low-power microcontroller which enables high computing power with very low power consumption. The prototype monitor, which is currently being designed, will be mounted on standard 3M 2560 Red Dot electrodes and fabricated on a flexible PCB substrate. Mounting the PCB directly to the electrodes will improve the SNR by an estimated 40 dB compared to using wired leads [3]. The monitor will be 'L' shaped with rounded corners and placed on the patient's chest. The 'L' shape will enable several mounting sites to be placed on the board which will allow the doctor to choose which measurement he would like to record. The monitor will have 320 Mbytes of FLASH memory which is enough to store two weeks of data sampled at 250 Hz continuously. Total power consumption of the system is estimated to be less than 8mW.

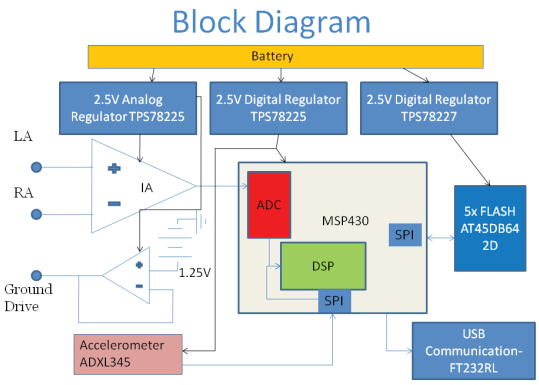


FIGURE 1: Block diagram of the ECG long-term Holter monitor system. The front end will use TI OPA333 and INA333 amplifiers and will have a bandwidth from 0.5 Hz to 125 Hz. 3 axis ADI accelerometer data will be sampled at 3Hz to help correlate activity level with the ECG recordings. The battery is a 3.7V 450 mAh Li-Pol cell from Cameron-Sino.

REFERENCES

[1] A. M. Abdulla. (2009, April 5, 2009). Holter monitor. *2009(April/21)*, pp. 1.

[2] M. A. Rockx, J. S. Hoch, G. J. Klein, R. Yee, A. C. Skanes, L. J. Gula and A. D. Krahn. (2005, Nov. 2005). Is ambulatory monitoring for "Community-acquired" syncope economically attractive? A cost-effective analysis of a randomized trial of external loop recorders versus holter monitoring. *AHJ 150(5)*, pp. 1065.e1-1065.e5.

[3] A. Searle and L. Kirkup, "A Direct Comparison of Wet, Dry and Insulating Bioelectric Recording Electrodes," *Physiol. Meas.*, vol. 21, pp. 271-283, 2000.

Energy Efficient On-Chip Equalized Interconnect

B. Kim, V. Stojanović

Sponsorship: SRC/FCRP IFC, Intel Corporation, CICS, SRC, Trusted Foundry

In recent high performance processor design, long distance interconnects became a serious bottleneck under tight power constraint [1]. Equalized on-chip interconnects have been presented significant improvement in performance without sacrificing too much power consumption [2,3].

This work presents further improvement of energy efficiency of equalized-interconnect by proposing two circuit techniques: 1) pre-distorted charge-injection (CI) feed-forward equalization (FFE); 2) trans-impedance (TIA) termination at receiver. Instead of using traditional analog subtraction, CI-FFE injects pre-computed the current value required for FFE into the channel while mitigating the nonlinearity of the driver. The non-linearity of the driver is statically compensated by pre-distorting FFE coefficients. The trans-impedance amplifier terminated at the receiver improves the bandwidth, signal amplitude, and reduces bias current.

A test-chip is fabricated in 90nm CMOS process and consumed about 0.4pJ/b running at 4Gb/s with vertical eye opening about 100mV and horizontal eye opening 50%UI differential peak-to-peak [4].

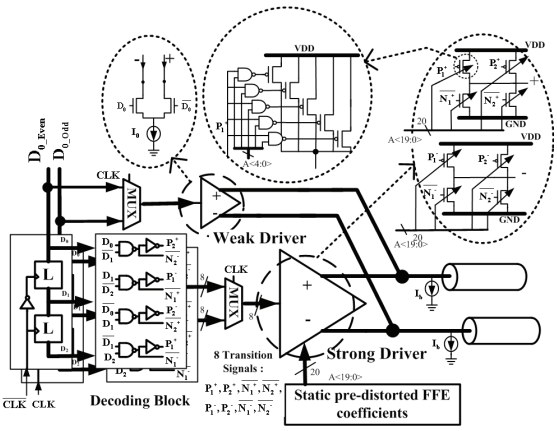


FIGURE 1: 3-tap Pre-distorted Charge-injection Feed-Forward Equalizing Transmitter

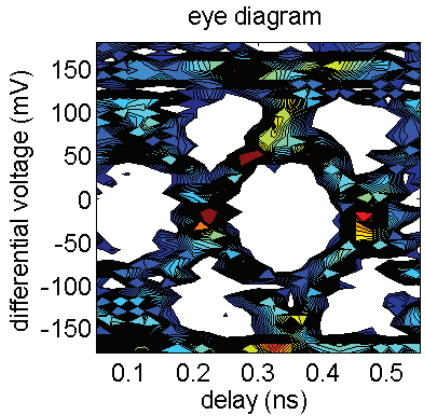


FIGURE 2: Measured eye diagram *in-situ*.

REFERENCES

[1] Kumar, R.; Zyuban, V.; Tullsen, D. M., "Interconnections in multi-core architectures: understanding mechanisms, overheads and scaling," in *Proc. 32nd International Symposium on Computer Architecture*, 2005.

[2] A.P. Jose, G. Patounakis and K.L. Shepard "Near speed-of-light on-chip interconnects using pulsed current-mode signaling," *VLSI Circuits, 2005. Digest of Technical Papers. 2005 Symposium on* no. SN -, pp. 108-111, 2005.

[3] Schinkel, D., Mensink, E., Klumperink, E.A., Tuijl, E. van and Nauta, B. "A 3-Gb/s/ch transceiver for 10-mm uninterrupted RC-limited global on-chip interconnects," *Solid-State Circuits, IEEE Journal of* vol. 41, no. 1 SN - 0018-9200, pp. 297-306, 2006.

[4] Kim, B. and Stojanović, V., "A 4Gb/s/ch 356fJ/b 10mm Equalized On-chip Interconnect with Nonlinear Charge-Injecting Transmit Filter and Transimpedance Receiver in 90nm CMOS Technology," in *Proc. International Solid-State Circuit Conference*, 2009.

A Fractionally Spaced Linear Receive Equalizer with Voltage-to-time Conversion

S. Song, B. Kim, V. Stojanović
Sponsorship: National Semiconductor, CICS

Based on voltage-to-time conversion technique [1-2], a pseudo-differential two-way-interleaved adaptive linear receive equalizer with two 2x-oversampled feed-forward taps has been designed in a 90-nm CMOS process. It integrates equalization and phase interpolation functions into one unit to simultaneously address inter-symbol-interference (ISI) cancellation and phase synchronization in a link receiver.

Due to the process speed limitation, the half-rate time interleaving technique is also applied (Figure 1). Four sampling phases (Φ_1- Φ_4) with 25% duty cycle are generated locally from Φ and Φ_- and another pair of quadrature clocks. A voltage-to-time (V2T) block converts the sampled signal into a delayed digital signal, transferring the sampled information into the time-domain. All four V2T converters are followed by a time-to-voltage (T2V) stage to realize summing, subtraction and multiplication. Equalizer tap weights are implemented as two programmable reference currents I_1 and I_2 biasing T2V blocks. Two slicers with tunable thresholds are added to sense the signs of the input signal and output error of the FSE, respectively, and to enable tap weight adaptation with external adaptive engine.

The design is fabricated in a 90-nm CMOS process. It operates at 4 Gbps with 8 mW power consumption and linearity of 4.3 effective bits at 1.2 V supply (Figure 2).

REFERENCES

[1] L. Brooks and H.-S. Lee, "A Zero-Crossing-Based 8b 200MS/s Pipelined ADC," *Solid-State Circuits Conference, 2007. ISSCC 2007. Digest of Technical Papers. IEEE International*, pp. 460-615, 2007.

[2] J. F. Bulzacchelli, M. Meghelli, S. V. Rylov, W. Rhee, A. V. Rylyakov, H. A. Ainspan, B. D. Parker, M. P. Beakes, Aichin Chung, T. J. Beukema, P. K. Pepeljugoski, L. Shan, Y. H. Kwark, S. Gowda and D. J. Friedman, "A 10-Gb/s 5-Tap DFE/4-Tap FFE Transceiver in 90-nm CMOS Technology," *Solid-State Circuits, IEEE Journal of*, vol. 41, pp. 2885-2900, 2006.

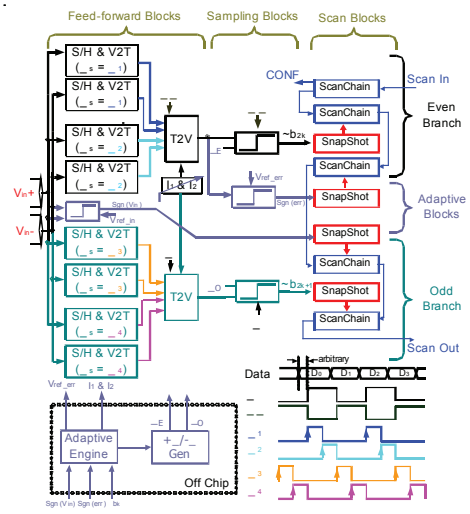


FIGURE 1: Block diagram of 2-tap 2xoversampled two-way time interleaved architecture. Scan-chain and snapshot are applied for ***in-situ*** link characterization.

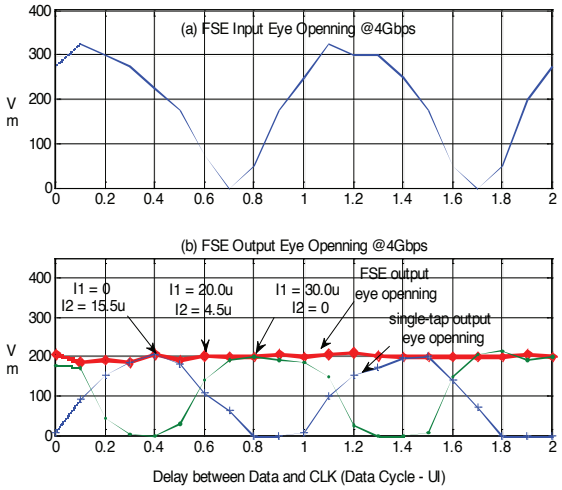


FIGURE 2: Input (a) and FSE output (b) eye opening vs. sampling phase.

Electronic Devices

Si Current-limiters based on Si Pillar Ungated FET for Field-emission Applications

Y. Niu, L. F. Velasquez-Garcia, A. I. Akinwande
Sponsorship: DARPA

We used vertical silicon ungated field-effect transistors (FETs) as current limiters to individually ballast field-emitter arrays of density. The device structure, shown in Figure 1, consists of silicon or carbon nanofiber (CNF) emission tips that are individually connected in series with high-aspect-ratio silicon pillars (1μm x 1μm x 100μm). The device structure provides a simple solution to three problems that have plagued field emission arrays: emission current uniformity, emission current stability, and reliability.

The ungated FETs are designed as high-aspect-ratio silicon pillars to achieve velocity saturation of carriers and obtain current source-like characteristics. The Si pillar ungated FETs are connected in series with field emitter tips to limit current in each field emitter in spite of tip radii variation/distribution. To provide rigorous characterization of the ungated FET behavior, we made a test structure that exposed selected numbers of columns. Also to achieve optimal dynamic output resistance of a current limiter, silicon pillar ungated FETs were fabricated on n-type substrates with 150-200 Ω-cm, 20-40 Ω-cm and 4-6 Ω-cm resistivity. Figure 2 is an example of current-voltage characteristics obtained on silicon pillar ungated FETs fabricated on a 20-40 cm resistivity. Process and device simulations were also conducted to solidify our experimental results.

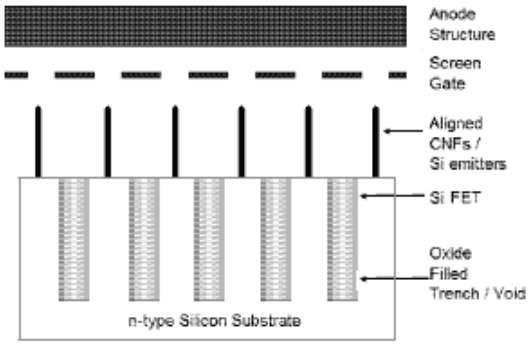


FIGURE 1: Device structure FEAs are formed on top of Si columns (FETs). Each column holds one emitter. The drain of the FET is connected to the emitter of the FE, i.e., node floating. Voltage is distributed between FEA and FET.

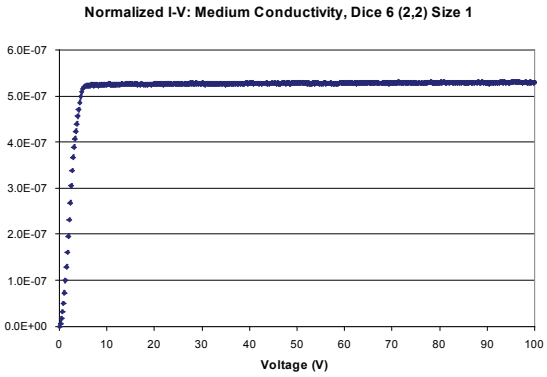


FIGURE 2: The FET characterization data show current saturation is achieved. The columns have dopant concentrations of 1x1015 cm-3, 2x1014 cm-3, and 2x1013 cm-3.

REFERENCES

[1] L. F. Velasquez-Garcia, B. Adeoti, Y. Niu, and A.I. Akinwande, "Uniform High Current Field Emission of Electrons from Si and CNF FEAs Individually controlled by Si Pillar Ungated FETs," *IEEE IEDM,* 2007, pp. 599-602.

[2] C. Canali, G. Majni, R. Minder, and G. Ottaviani, "Electron and Hole Drift Velocity Measurements in Silicon and Their Empirical Relation to Electric Field and Temperature," *IEEE Trans.Electron Devices,* vol. ED-22, pp. 1045-1047, 1975.

[3] B. T. Murphy, "Unified Field-Effect Transistor Theory Including Velocity Saturation," *IEEE Journal of Solid-State Circuits,* Jun. 1980, pp. 325-327.

[4] J. Baek, M.S. Shur, K. W. Lee, and T. Vu, "Current-Voltage Characteristics of Ungated GaAs FET's," *IEEE Transactions on Electron Devices,* Nov. 1985, pp. 2426-2430.

[5] H. J. Boll, J. E. Iwersen, and E. W. Perry, "High-speed current limiter," *IEEE Trans. Electron Devices*, vol. ED-13, pp. 904-907, Dec. 1966.

[6] H. Takemura, Y. Tomihari, N. Furutake, F. Matsuno, M. Yoshiki, N. Takada, A. Okamoto and Soichiro Miyano "A Novel Vertical Current Limiter Fabricated with a Deep Trench Forming Technology for Highly Reliable Field Emitter Arrays," NEC Corporation.

Semiconductor and Insulator Engineering for the Improvement of Organic Thin-Film Transistors

M. A. Smith, A. I. Akinwande
Sponsorship: GEM Ph.D. Engineering Fellowship, Office of the Dean for Graduate Students

The potential uses for electronic solid state devices are endless. As organic semiconductor-based devices can easily be scaled to large areas and fabricated on mechanically compliant and non-planar surfaces at low temperatures, they can lead to a more profound realization of the possibilities that solid state technologies offer [1].

To realize organic semiconductor-based devices as a pervasive complement to Si CMOS devices, the electrical performance of organic semiconductor devices must be improved. In particular, the operating voltage must reduce while the current and the on-current to off-current ratio increase. The device of interest is a pentacene-based organic thin-film transistor (OTFT). Delocalized ð-bonded electrons enable semiconducting behavior in pentacene [1]. To make useful circuits, key device parameters such as threshold voltage, subthreshold slope, and on-current to off-current ratio have to be reproducible. Ultimately, these device parameters are related to pentacene thin-film quality (grain size, growth modes, and material phases), which affects carrier mobility.

Conventional methods of device fabrication have been used to address performance issues with limited success. This work will address these issues through insulator and semiconductor engineering. Initial efforts will concentrate on engineering the gate insulator by using a high dielectric constant material. Specifically, BZN ($Bi_{1.5}Zn_{0.8+x}Nb_{1.3-x}O_7$) is a paraelectric pyrochlore system that boasts a high dielectric constant, low dielectric loss, and low co-firing temperature, making it a viable insulator for improving OTFT performance and enabling advanced circuit design [2]. Later phases of this work will focus on engineering the semiconductor deposition. Enhancements to standard evaporative deposition techniques will be explored by in situ coupling of new forms of energy to control pentacene thin-film morphology and defects.

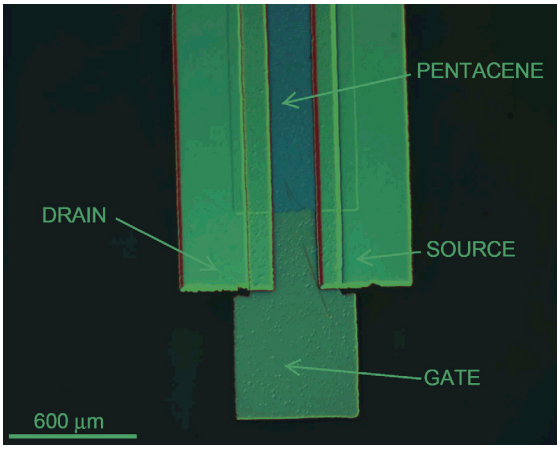


FIGURE 1: Pentacene OTFT top view micrograph

REFERENCES:

[1] M. Kitamura and Y. Arakawa, "Pentacene-based organic field-effect transistors," *Journal of Physics-Condensed Matter,* vol. 20, May 2008.

[2] Y. Choi, I. D. Kim, H. L. Tuller, and A. I. Akinwande, "Low-voltage organic transistors and depletion-load inverters with high-K pyrochlore BZN gate dielectric on polymer substrate," *IEEE Transactions on Electron Devices,* vol. 52, pp. 2819-2824, Dec 2005.

High-performance Cold Cathodes for Sub-mm-wave Compact Sources

L. F. Velásquez-García, Y. Niu, S. Guerrera, A. I. Akinwande
Sponsorship: DARPA

The continued demand for very wideband communications and increased need for wireless channel capacity have led to the exploration of new regions of operation that will exploit the upper millimeter-wave spectral range. The broad minimum that occurs in atmospheric absorption between 200GHz and 300 GHz is largely under-utilized because of a lack of high-bandwidth and high-power amplifiers in this frequency range that are compact and efficient. The core of proposed vacuum amplifier technology is a field-emitter-array (FEA) cathode. Due to the exponential dependence of the emitted current on the emitter tip radius [1], emission currents are extremely sensitive to tip radii variation. In addition, research has shown that nm-sized emitter tips have a distribution with long tails [2]. Therefore, spatial variation of tip radius results in the spatial variation of the emission currents and hence the current density. The variation also results in non-uniform turn-on voltages even when the tips are located next to each other. Moreover, at a given voltage only a small fraction of the tips in an FEA emit because the sharper tips burn out early, before the duller tips emit, resulting in under-utilization of the FEA (Figure 1). Attempts to increase the emission current by increasing the voltage often result in burnout and shifting of the operating voltage to higher voltages. Spatial non-uniformity can be substantially reduced if arrays of emitters are ballasted [3]. Ungated FETs are ideal to individually ballast each emitter because they behave like current sources and can be fabricated with high emitter density FEAs [4]. Limiting the current from each emitter makes it possible to prevent destructive emission from the sharper tips while allowing higher overall current emission because of the emission of the duller tips. Using the ungated FET individual ballasting technology, we have demonstrated more than 600 mA of emission with no damage to the cathode (Figure 2).

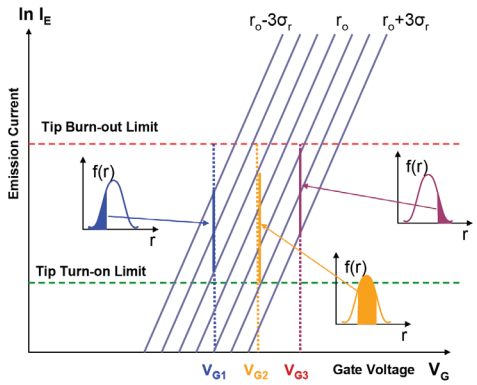


FIGURE 1: Emission current I_E versus gate voltage V_G for varying tip radii r. The tip radius has a distribution with variation σ and mean r_o. The emitter current falls within the turn-on limit (controlled by the noise floor) and the burn-out limit (due to ohmic heating). For a constant gate bias, only a small percentage of the tips contributes to the total emission current.

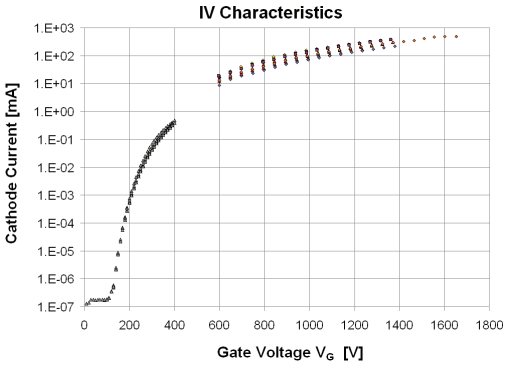


FIGURE 2: The DC (low-current) and pulsed (high current) IV characteristics of a 1-million field emitter array. More than 600 mA of current were measured with no damage to the cathode.

REFERENCES

[1] R. Gomer, *Field Emission and Field Ionization*, American Institute of Physics, New York, 1961.

[2] M. Ding, G. Sha, and A. I. Akinwande, "Silicon Field Emission Arrays With Atomically Sharp Tips: Turn-On Voltage and the Effect of Tip Radius Distribution", *IEEE Transactions on Electron Devices*, Vol 49, No. 12, Dec. 2002, pp. 2333 – 2342.

[3] H. Takemura, Y. Tomihari, N. Furutake, F. Matsuno, M. Yoshiki, N. Takada, A. Okamoto, and S. Miyano, "A novel vertical current limiter fabricated with a Deep-trench-forming technology for highly reliable field emitter arrays", *Technical Digest of the IEEE International Electron Device Meeting*, Dec. 1997, pp. 709-712.

[4] L. F. Velásquez-García, B. Adeoti, Y. Niu and A. I. Akinwande, "Uniform High Current Field Emission of Electrons from Si and CNF FEAs Individually Controlled by Si Pillar Ungated FETs", *Technical Digest IEEE International Electron Device Meeting*, Washington DC, USA, Dec. 2007, pp. 599 – 602.

Reproducible Lithographically Patterned Metal-oxide Transistors for Large-area Electronics

A. Wang, B. Yaglioglu, C. G. Sodini, V. Bulović, A. I. Akinwande
Sponsorship: SRC/FCRP C2S2

Metal-oxide-based field-effect transistors (FETs) have been demonstrated with higher charge-carrier mobilities, higher current densities, and faster response performance than amorphous silicon FETs, which are the dominant technology used in display backplanes [1], [2]. Because the optically transparent semiconducting oxide films can be deposited at near-room temperatures, these materials are compatible with future generations of large-area electronics technologies that require flexible substrates [3]. Our project aims to develop a low-temperature, scalable lithographic process for metal oxide-based FETs that can be integrated into large-area electronic circuits.

While any single demonstrated transistor may have excellent characteristics, circuit design using these FETs is impossible without the capability to reproducibly fabricate FETs with uniform characteristics. Previously, we demonstrated top-gate, fully lithographic FETs of varying channel lengths on 100-mm glass wafers with a sputtered ZnO:In_2O_3 channel layer, using an organic polymer, parylene, as the gate dielectric and indium-tin-oxide (ITO) for source/drain contacts. Because of process non-uniformities, however, FET turn-off voltages (V_{OFF}) across a wafer and between wafer lots varied by as much as ±10V. By modifying the process to deposit semiconductor and protective dielectric together without breaking vacuum, the FET uniformity across wafers was improved; the standard deviation of V_{OFF} decreased to <1V across three subsequently-processed wafer lots. Figure 1 shows a photograph of a 100-mm glass after fabrication was completed; current-voltage characteristics for a device fabricated in the improved process are shown in Figure 2. This baseline process can provide a platform for the design of oxide FET-based circuits, as well as for studying the underlying device physics of metal-oxide FETs.

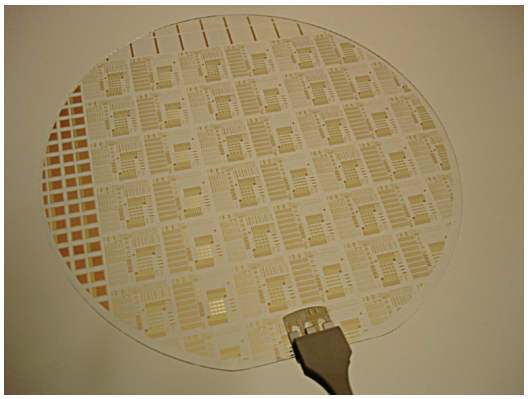


FIGURE 1: A 100-mm glass wafer with lithographically patterned metal-oxide field-effect transistors. Device uniformity can be examined by comparing transistors of the same geometry from different die across the wafer.

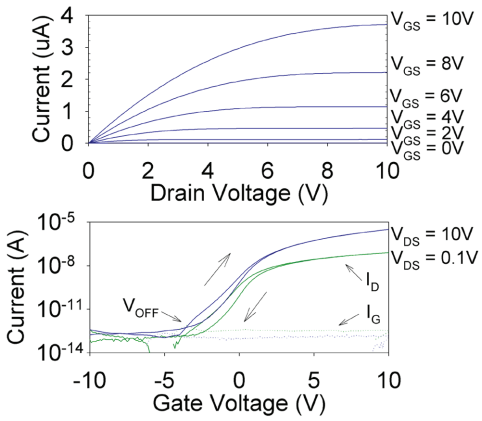


FIGURE 2: Current-voltage characteristics of lithographically patterned FET (W/L = 100mm / 100mm). Output curves are plotted in the top graph; double-swept transfer curves taken in saturation and triode regions are plotted on the bottom. The turn-off voltage, V_{OFF}, is -4V.

REFERENCES

[1] R.L. Hoffman, B.J. Norris, and J.F. Wager, "ZnO-based transparent thin-film transistors," *Applied Physics Letters*, vol. 82, no. 5, pp. 733-735, Feb. 2003.

[2] K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, and H. Hosono, "Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors," *Nature*, vol. 432, pp. 488-492, Nov. 2004.

[3] E. Fortunato, P. Barquinha, A. Pimentel, A. Goncalves, A. Marques, L. Pereira, and R. Martins, "Fully transparent ZnO thin-film transistor produced at room temperature," *Advanced Materials*, vol. 17, pp. 590-594, Mar. 2005.

High-electron-mobility Germanium MOSFETs: The Effect of n-type Channel Implants and Ozone Surface Passivation

J. Hennessy, D. A. Antoniadis
Sponsorship: SRC/FCRP MSD

Germanium n-channel devices have historically shown poor performance due to an asymmetric distribution of interface states that degrade electrostatic behavior and carrier mobility. In this work, we demonstrate two methods for improving the performance of Ge n-MOSFETs: ozone surface passivation and n-type ion-implantation. Figure 1 shows the interface state density (D_{it}) extracted near the middle of the bandgap by the conductance method for germanium samples receiving *in-situ* exposure to a high concentration of ozone immediately prior to Al_2O_3 gate deposition. Both n-type and p-type samples that received ozone treatment show a significant reduction in D_{it} compared to samples that received a standard wet clean only. This technique has also been shown to result in D_{it} reduction near both band edges and enhanced electron and hole mobility [1]. Previous work has demonstrated enhanced electron mobility for phosphorus-implanted Ge n-MOSFETs [2]. Figure 2 shows the effective electron mobility of Ge n-MOSFETs that received channel implants of arsenic or antimony in addition to ozone surface passivation prior to gate deposition. Devices receiving a 4×10^{12} cm^{-2} dose show a significant increase in electron mobility, particularly at low inversion densities, but also a degraded subthreshold slope and increased off-state current, indicating some buried-channel-like behavior. Devices receiving a 1×10^{12} cm^{-2} implant dose show little degradation in subthreshold slope but maintain a significant enhancement in mobility compared to un-implanted devices [1].

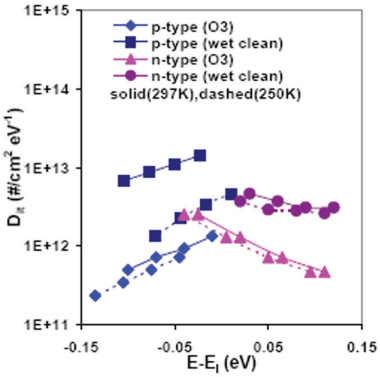


FIGURE 1: The D_{it} near the middle of the bandgap for ALD Al_2O_3 on O3-treated germanium substrates

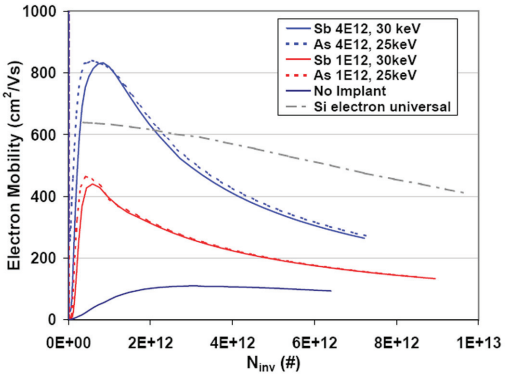


FIGURE 2: Effective electron mobility (split-CV) for As and Sb implanted germanium n-MOSFETs.

REFERENCES

[1] J. Hennessy and D. A. Antoniadis, "High Electron Mobility Germanium MOSFETs: Effect of n-type Channel Implants and Ozone Passivation," in *Proc. 67th Annual Device Research Conference*, 2009, to be published.

[2] A. Ritenour, J. Hennessy, and D. A. Antoniadis, "Investigation of carrier transport in germanium MOSFETs with WN/Al_2O_3/AlN gate stack," *IEEE Electron Device Letters*, vol. 28, no. 8, pp. 746-749, Aug. 2007.

Si/SiGe Tunneling Transistors

H. Lee, O. Nayfeh, L. Gomez, J. L. Hoyt, D. A. Antoniadis
Sponsorship: DARPA

The tunneling field-effect transistor (TFET) is interesting as a promising candidate for future complementary metal-oxide-semiconductor (CMOS) technology due to its potential for low-voltage operation. To successfully compete with conventional MOSFETs, it is important to decrease the sub-threshold swing (SS) and improve the drive current to reduce the power requirements. Theoretically the sub-threshold swing of TFETs could be scaled down to below 60 mV/dec at room temperature due to the band-to-band tunneling (BTBT) mechanism of operation. Optimization of tunneling current is complex since it depends on several parameters such as doping concentration and profile abruptness of the source, gate oxide thickness, and low band-gap material [1]. In this work, planar-heterojunction TFETs with Si/strained SiGe have been fabricated with two different nominal Ge concentrations (40 % and 70 %) and with gate oxide thicknesses of 2.5 and 3.5nm. Biasing conditions have been utilized in order to observe the different tunneling injection mechanism such as N-channel TFET (NTFET) and P-channel TFET (PTFET). The measurement has been done in NTFET mode by using an N+ bias (V_{N+} > 0) condition and a negative gate bias (see inset of Figure 1). The comparison of NTFET I-V characteristics between 70 % Ge and 40 % Ge content structures is shown in Figure 1. A device with 70 % Ge content displays an improved drive current and SS compared to a 40% Ge NTFET due to the reduction in tunneling barrier width and high mobility. Work is in progress with laser spike annealing (LSA) in order to improve performance by reducing Ge out-diffusion during implant activation. Figure 2 shows the comparison of NTFETs with varying oxide thickness. The device with the thinner gate oxide has improved drive current. This trait is due to the improved coupling of the gate potential to the channel [2].

REFERENCES

[1] O.M. Nayfeh, C. N. Chleirigh, J. Hennessy, L. Gomez, J. L. Hoyt, and D.A. Antoniadis, "Design of Tunneling Field-Effect Transistors using Strained-Silicon/Strained-Germanium Type-II Staggered Heterojunction," IEEE Electron Device Letters, vol. 29, no. 9, pp. 1074-1077, Sep. 2008

[2] W. Y. Choi, J. Y. Song, J. D. Lee, Y. J. Park, and B.-G. Park, "Tunneling field-effect transistors (TFETs) with subthreshold swing (SS) less than 60 mV/dec," IEEE Electron Device Letters, vol. 28, no. 8, pp. 743-745, Aug. 2007.

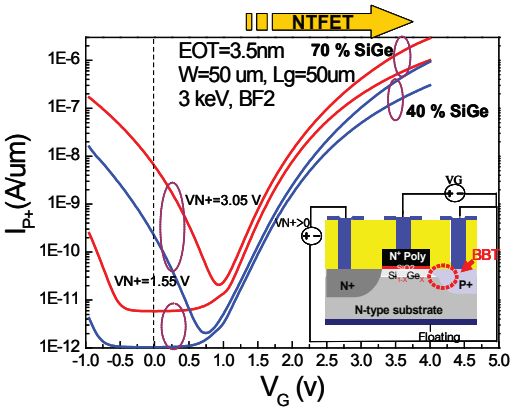


FIGURE 1: Measured transfer characteristics (drain current, I_{P+} versus V_G) for NTFETs with 40 % SiGe and 70 % SiGe. Increasing Ge content improves the drive current and sub-threshold swing. The inset shows a cross-sectional view of the fabricated TFET and an experimental bias setup condition for creating the NTFET operation mode.

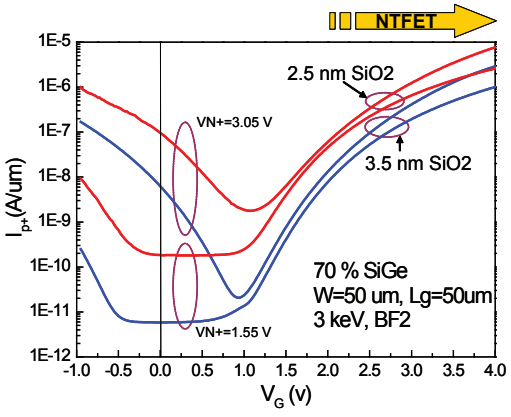


FIGURE 2: Measured transfer characteristics (drain current, I_{P+} versus V_G) for NTFETs with 2.5- and 3.5-nm-thick gate oxides.

Impact of Uniaxial Strain and Channel Orientation on Band-to-band Tunneling in Si/SiGe Heterostructures

O. M. Nayfeh, L. Xie, J. A. del Alamo, J. L. Hoyt, D. A. Antoniadis
Sponsorship: SRC/FCRP MSD, DARPA

Heterostructure tunneling field effect transistors (HTFETs) have potential for extremely low voltage operation (<0.3 V) [1]. These devices make use of the large gate-controlled band-to-band tunneling (BTBT) efficiency in Si/SiGe heterostructures due to the reduced energy gap of the material [2]. It is important to understand the physics of BTBT with varying channel orientations and applied additional mechanical uniaxial stress so as to design and engineer more optimal future devices that may encounter these conditions intentionally or unintentionally. Figures 1 and 2 show select measurements (I-V) of a Si/SiGe BTBT device with varying channel orientation and applied mechanical uniaxial compressive strain.

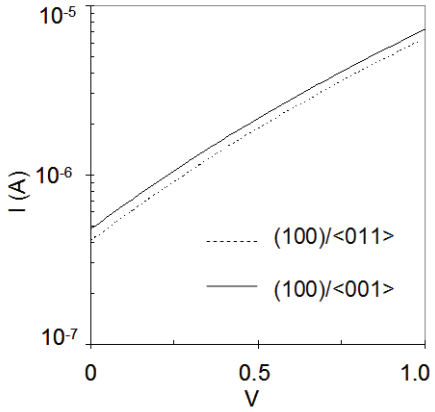


FIGURE 1: The Si/SiGe BTBT current for <001> and <001> channel orientations on (100) wafer.

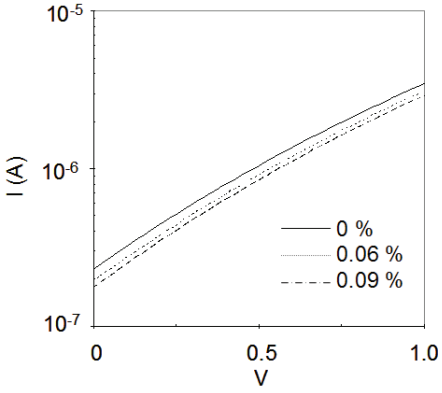


FIGURE 2: The Si/SiGe BTBT current for varying levels of applied mechanical uniaxial compressive strain.

REFERENCES

[1] O.M. Nayfeh, C. Ni Chleirigh, J. Hennessy, L. Gomez, J.L. Hoyt and D.A. Antoniadis, "Design of Tunneling Field Effect Transistors using Strained-Silicon/Strained-Germanium Type II Staggered Heterojunctions," *IEEE Electron Device Letters*, vol. 29, no.9, pp. 1074-1077, 2008.

[2] O.M. Nayfeh, C. Ni Chleirigh, J.L. Hoyt and D.A. Antoniadis "Measurement of Enhanced Gate-Controlled Band-To-Band Tunneling in Highly Strained Silicon-Germanium Diodes," IEEE Electron Device Letters, vol. 29, no.5, pp. 468-470 (2008)

Nonvolatile Memory Devices with Nanoparticle/High-k Dielectric Tunnel-barrier Engineering

O. M. Nayfeh, J. Hennessy, D. A. Antoniadis, K. Mantey, M. H. Nayfeh
Sponsorship: SRC/FCRP MSD

Silicon-nanoparticle-based nonvolatile memory devices using uniformly delivered colloidal nanoparticles [1] are candidate replacement candidates for traditional polysilicon flash memory [2], [3]. Future devices are envisioned to require the use of high-k dielectrics for achieving suitable nonvolatile memory characteristics [2]. In this work we make use of novel heterojunctions formed between silicon nanoparticles and high-k dielectrics to design and construct more optimal nonvolatile memory devices using tunnel barrier engineering. Figure 1 shows a cross-sectional TEM of silicon nanoparticles embedded in an atomic-layer-deposited high-k dielectric (Al_2O_3). Figure 2 shows a select capacitance-voltage (C-V) hysteresis measurement of the device.

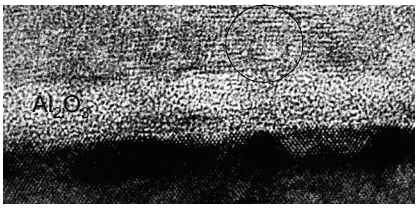


FIGURE 1: Example XTEM, a constructed device showing silicon nanoparticles (2.9 nm, circled) embedded in ALD-deposited Al_2O_3.

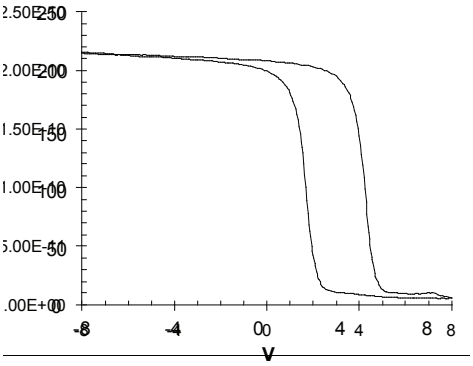


FIGURE 2: Capacitance-voltage (C-V) hysteresis characteristics of the device.

REFERENCES

[1] O.M. Nayfeh, D.A. Antoniadis, K. Mantey, and M.H. Nayfeh "Uniform Delivery of Silicon Nanoparticles on Device Quality Substrates using Spin-Coating from Isopropyl Alcohol Colloids, " Accepted for Publication in *Applied Physics Letters*(2009)

[2] O.M. Nayfeh, D.A. Antoniadis, K. Mantey, and M.H. Nayfeh, "Memory effects in metal-oxide semiconductor capacitors incorporating dispensed highly monodisperse 1 nm Si nanoparticles," *Applied Physics Letters* , Volume 90, 153015, (2007)

[3] O.M. Nayfeh, "Nonvolatile Memory Devices with Colloidal 1.0 nm Silicon Nanoparticles: Principles of Operation, Fabrication, Measurements, and Analysis ", PhD dissertation, MIT, Cambridge, MA, 2008

Exciplex Transistors

J. Lee, C. L. Mulder, M. A. Baldo
Sponsorship: NRI/INDEX

Excitons, bound pairs of electrons and holes, mediate the interconversion of charges and photons and thus can be used for an efficient interconnect between electronic circuits and optical communication. The ability to guide excitons in space can lead to an excitonic switch that directly routes an optical signal. Recently, High et al. demonstrated an excitonic transistor using indirect excitons formed in AlGaAs/GaAs coupled quantum wells at a temperature of 1.4K [1]. The much larger binding energy of excitons in organic semiconductors could enable excitonic transistors at room temperature. Furthermore, by exploiting spin-disallowed transitions in organic materials, room temperature excitons can last up to milliseconds, more than sufficient to enable exciton propagation over large distances and the operation of sample circuits.

In this work we aim to demonstrate an exciton transistor based on organic semiconductors that can operate at room temperature. Exciplexes, indirect electron-hole pairs situated on adjacent molecules, are interesting because they are spatially oriented with a defined electron-hole spacing. The exciplex energy can be controlled by applying electric fields. We propose to guide exciplexes using the energy gradient determined by external electric fields (See Figure 1). In Figure 2, we show that by changing the voltage bias over a 4,4',4"-tris-(3-methylphenylphenylamino)triphenylamine (m-MTDATA)/bathocuproine (BCP) heterojunction, the energy of the exciplexes can be changed over 40meV, well above thermal energy at room temperature. We also observe that long-lived exciplexes can be created with a lifetime of several microseconds at room temperature in the phosphorescent system of N,N'-diphenyl-N,N'-bis(3-methyl-phenyl)-l,l'biphenyl-4,4'diamine (TPD)/iridium(III) bis(4,6-difluorophenylpyridinato-N,C2')-picolinate (Firpic). These results open a promising route toward the spatial manipulation of exciplexes in organic semiconductors.

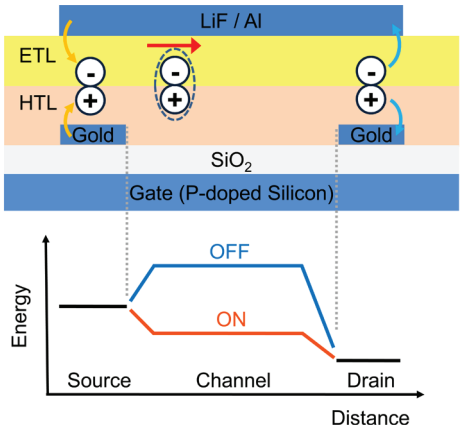


FIGURE 1: The device structure of the organic exciplex transistor and its energy profile under the operating condition. We control exciplex fluxes by modulating the gate bias and, thus, the potential barrier. The source creates exciplexes by injecting electrons and holes. The drain detects the exciplex fluxes by separating and extracting them with high reverse biases.

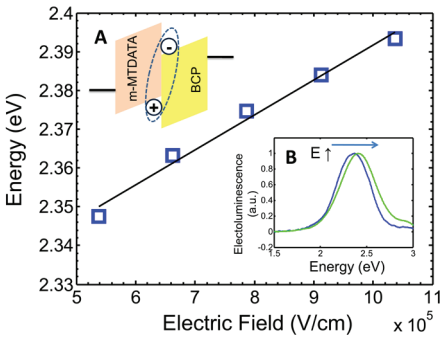


FIGURE 2: The control of the exciplex energy by an external electric field. The exciplex energy is changed over 40meV in an organic heterojunction of m-MTDATA and BCP. Inset (A): the organic heterojunction diode that exhibits exciplex emission. Inset (B): the electroluminescence spectra with low and high electric fields.

REFERENCES

[1] A. A. High, E. E. Novitskaya, L. V. Butov, M. Hanson, and A. C. Gossard, "Control of exciton fluxes in an excitonic integrated circuit," *Science*, vol. 321, pp. 229-231, July 2008.

Modeling of Deep-reactive Ion-etch Variation

J. O. Diaz, H. K. Taylor, D. S. Boning
Sponsorship: Sandia National Laboratories

Our modeling work with deep-reactive ion-etching (DRIE) has provided effective models to account for wafer-, die-, and feature-level non-uniformities [1]-[3]. The variation observed has been explained by spatial and temporal differences in the amount of F radical species at the wafer surface and their limited flux into features [4]. Despite our previous success integrating wafer- and die-level models, fundamental incompatibilities between these and most feature-level models had prevented us from integrating them together. We have revised our modeling methods to eliminate model compatibility issues. On the wafer- and die-levels, our new approach uses a simple electrical network analogue (Figure 1) to predict the time-evolving concentration of the etchant species available to the features. This prediction is used to provide estimates of the average etch rate in different regions within the wafer. The direct compatibility with the existing feature-level semi-physical models provides the flexibility to easily incorporate future effect-modeling enhancements such as sidewall etching and tapering. The model can also be tuned to specific tool-dependent etching characteristics and etch "recipes" by the fitting of parameters extracted from etch-depth measurements of wafers with pre-determined patterns. We are currently interested in unifying this model into a CAD tool capable of optimizing MEMS fabrication by accurately depicting the tradeoff between etching speed and uniformity in DRIE, which requires selecting and using the best feature-level model available. Additionally, we would like to expand current feature-level models to correctly account for the main sidewall effects relevant to the reliability of MEMS devices.

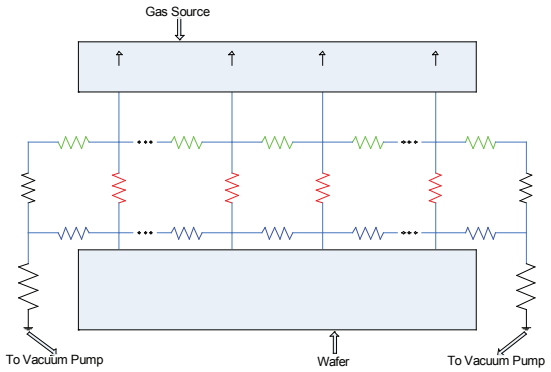


FIGURE 1: The electrical equivalent network used for DRIE wafer- and die-level modeling. In it, voltage corresponds to F radical concentration while current corresponds to radical flux in a given direction.

REFERENCES

[1] H. K. Taylor, H. Sun, T. F. Hill, A. Farahanchi and D. S. Boning, "Characterizing and predicting spatial nonuniformity in the deep reactive ion etching of silicon," *J. Electrochem. Soc.* 153, C575–85 (2006).

[2] T. Hill, H. Sun, H. K. Taylor, M. A. Schmidt, and D. Boning, "Pattern Density Based Prediction for Deep Reactive Ion Etch (DRIE)," *Tech. Digest of 2004: Hilton Head Solid-State Sensors and Actuators Workshop,* Hilton Head Island, SC, 2004.

[3] A. Farahanchi, "Characterization and Modeling of Pattern Dependencies and Time Evolution in Plasma Etching". Master's Thesis, Massachusetts Institute of Technology, Cambridge, 2008.

[4] R.A. Gottscho, C.W. Jurgensen, and D.J. Vitkavage, "Microscopic uniformity in plasma etching," *J. Vac. Sci. Technol.* B, vol. 10, pp. 2133–2147, 1992.

Modeling of Electrochemical-mechanical Polishing (ECMP)

W. Fan, J. Johnson, D. S. Boning
Sponsorship: SRC/SEMATECH Engineering Research Center for Environmentally Benign Semiconductor Manufacturing

Electrochemical mechanical polishing (ECMP) is an emerging technology in semiconductor processes, used for Cu interconnecting layer planarization. In previous work, our group proposed a non-ohmic ECMP model to understand the exponential dependence of current on overpotential at the electrode/electrolyte interface and to calculate the Cu removal rate [1]. Based on electrochemical theory and process physics, the model has been well improved and extended to 3D accounting for lateral voltage/current distribution and Cu-layer resistance change during the process. The calculation is simplified by using equivalent circuit elements to simulate the electrochemical reaction.

As Figure 1(a) shows, the model captures the electrochemical reactions occurring at surfaces of both the wafer and the polishing pad using equivalent diode elements, and the lateral coupling distribution in the electrolyte is modeled using resistive elements.. Assuming that single-wafer rotation time is much shorter than total polishing time, radial time-averaged current density distributions on the wafer surface are calculated due to multiple voltage zones (Figure 1(b)). From the simulation result, we conclude that the model computes the current density of the chemical reaction in the water surface effectively (Figure 2(a)). Figure 2(b) shows the radial averaged current density, which is proportional to the instantaneous removal rate. Current work is seeking to calculate the Cu thickness evolution during the process and extract model parameters to fit experiment data.

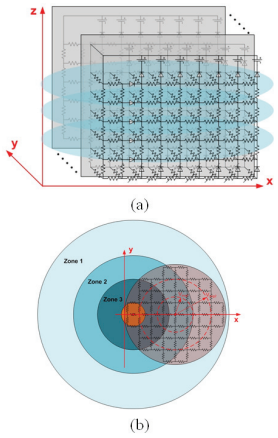


FIGURE 1: (a) Framework of the 3D ECMP model. The top voltage source level is a pad and the bottom variable resistors level is a Cu wafer. The electrolyte in the middle is simulated by pure resistors. The overpotential at electrolyte and wafer/pad surface is characterized by diodes. (b) Top view of pad showing multiple voltage zones and Cu wafer position. The wafer is connected to the ground via the contact point in the pad's center. From the wafer's center to its edge, the radial average current density is calculated along the red dashed circles.

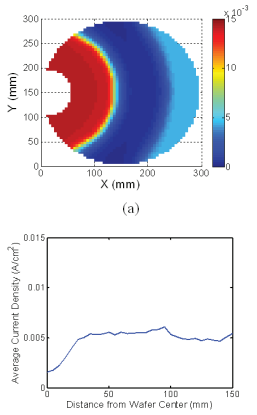


FIGURE 2: (a) The distribution of the current density of the chemical reaction on the wafer surface (A/cm^2) in the beginning of the process. The pad voltage zone settings are V_1=2V, V_2=1V, and V_3=3V. The blank area in the wafer image is the part under the contact point where no chemical reaction occurs. (b) The instantaneous current density along the wafer radius at the beginning of process. The removal rate and removal amount in each time step can be calculated with the current density.

REFERENCES

[1] Z. Li, D. Truque, D. Boning, R. Caramto, and C. Borst, "Modeling wafer level uniformity in electrochemical-mechanical polishing (ECMP)," *Advanced Metallization Conference*, Albany, NY, Oct. 2007.

Stability of Metal Oxide-based Field-effect Transistors

B. Yaglioglu, A. Wang, K. Ryu, C. Sodini, A. I. Akinwande, V. Bulović
Sponsorship: Hewlett-Packard, DARPA

The main goal of this research is to combine a low-temperature budget fabrication method with scalable processes such as sputter deposition to realize oxide channel field-effect transistors (FETs) on glass or flexible plastic substrates. Oxide-based transistors offer an attractive alternative to commercially used amorphous Si transistors due to their high mobility values (~10-20cm²/Vs vs ~1cm²/Vs) [1-3]. Field-effect mobility, sub-threshold slope, and threshold voltage of FETs are the main parameters that are characterized for circuits. However, reliability of properties needs to be also addressed before these devices take their place in large-area electronic applications.

In this study we test the stability of FETs that have a polymer dielectric, parylene, and an amorphous oxide semiconductor, zinc indium oxide. The devices are processed lithographically at low temperatures (T ≤ 100 ºC). Figure 1 shows a typical transfer characteristics curve representing device performance. The inset gives the distribution of the threshold voltage across a 4-inch wafer. In Figure 2, the change in I-V characteristics is shown under a prolonged gate bias stress. The gate bias is interrupted at fixed times to record the transfer characteristics of the transistor at a drain bias of V_D=1V. Preliminary results of I-V tests show a positive shift in the threshold voltage. Two possible mechanisms that are originally proposed for similar shifts in amorphous Si FET's are metastable state generation in the semiconductor and charge trapping in the dielectric [4]. Stability experiments at different temperatures and bias gate voltages are conducted to understand the instability mechanisms in these hybrid (inorganic/organic) devices.

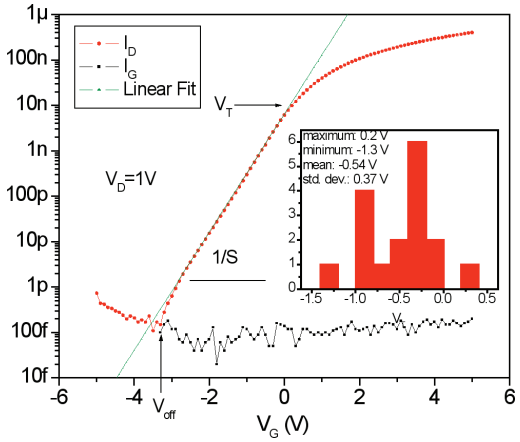


FIGURE 1: Transfer characteristics of a W/L=100µ/100µ transistor. Data are taken from -5V to 5V with 0.1V steps while V_D= 1V. The distribution of threshold voltage collected from 17 devices on different dies across the wafer is given in the inset.

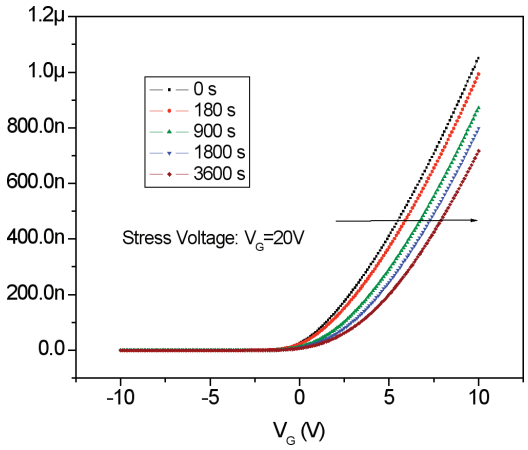


FIGURE 2: The V_G-I_D curve of a transistor as a function of stress time. The stress measurement is interrupted every 180s to measure the transfer characteristics. Measurements after 3min, 15min, 30min, and 1h are included to show the shift in the characteristics.

REFERENCES

[1] P.F. Carcia, R.S McLean, M.H. Reilly, and G. Nunes, "Transparent ZnO thin film transistors fabricated by rf magnetron sputtering," *Applied Physics Letters*, vol. 82, no. 7, pp. 1117-1119, Feb. 2003

[2] N.L. Dehuff, E.S. Kettenring, D. Hong, H.Q. Chiang, J.F. Wager, R.L. Hoffman, C.H. Park, and D.A. Keszler, "Transparent thin film transistors with zinc indium oxide channel layer," *Journal of Applied Physics*, vol. 97, no. 6, pp. 064505:1-5, Mar. 2005.

[3] H. Kumomi, K. Nomura, T. Kamiya, and H. Hosono, "Amorphous oxide channel TFTs," *Thin Solid Films*, vol. 516, no. 7, pp.1516-1522, Feb. 2008.

[4] M.J. Powell, C. van Berkel, and J R. Hughes, "Time and temperature dependence of instability mechanisms in amorphous silicon thin-film transistors," *Applied Physics Letters*, vol. 54, no.14, pp. 1323-1325, Jan. 1989.

Electrical Reliability of GaN HEMTs on Si Substrates

S. Demirtas, J. A. del Alamo
Sponsorship: ARL MURI

GaN High Electron Mobility Transistors (HEMT) are very promising devices for high power, high frequency applications due to the unique properties of the GaN system. However, their reliability is limited even when grown on traditional substrates such as SiC, which has a relatively good match with the GaN lattice. Recently, Si has emerged as a very attractive alternative to SiC substrates due to its low cost, availability and well-known characteristics. The disadvantage of using a Si substrate is the increased lattice and thermal mismatch with GaN. This brings new reliability concerns. In our work, we have carried out systematic reliability experiments on industrial devices from our collaborators Nitronex Corporation and Triquint Semiconductor to understand the mechanisms of electrical degradation of GaN HEMTs on Si.

One of the consequences of growing GaN-on-Si is an increased number of traps and other electrical defects. This is observable in fresh HEMTs. Figure 1 compares current transients observed in virgin GaN-on-Si and GaN-on-SiC devices after a 1 second pulse of -10V at the gate. The purpose of such a short pulse is to "pump" electrons into the traps which get negatively charged and hence suppress the 2DEG in the channel, causing a sudden decrease in drain current. As time goes on, these electrons will be detrapped from these states allowing the current to "recover" to its original value before the pulse. As the number of traps increase, more electrons will be trapped in these states and the initial current collapse is larger. In our experiments we monitor I_{Dlin}, which is the drain current at V_{DS}=0.5 V and V_{GS}=1 V. Our experiments show a higher current collapse and a slower recovery in devices on a Si substrate when compared to devices on a SiC substrate. Clearly this shows that the higher mismatch between the GaN heterostructure and the Si substrate causes more traps than on a SiC substrate.

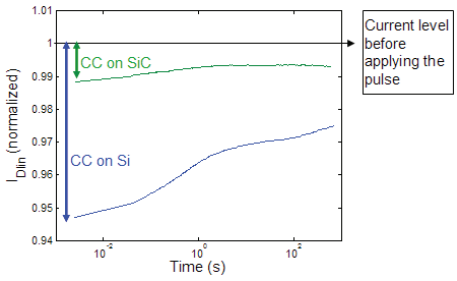


FIGURE 1: Comparison of current transients in fresh GaN-on-Si and GaN-on-SiC HEMTs after the application of 1 second pulse of value -10V at the gate. The current transient curves are normalized to the uncollapsed values of I_{Dlin}. Note the larger current collapse in GaN-on-Si HEMT due to increased number of traps caused by the larger substrate mismatch.

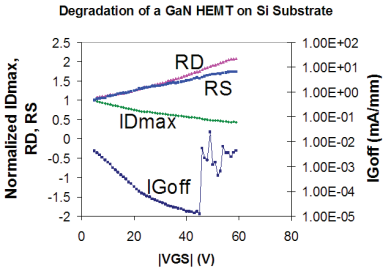


FIGURE 2: Output of the characterization suite utilized in our research for a typical electrical stress experiment. In this stress test, V_{DS}=0V and constant whereas V_{GS} is stepped from -5V to -60V by 1V every 10 seconds. R_D and R_S increase whereas I_{DMAX} decreases with increased stress. I_{GOFF} exhibits a decrease first until the critical voltage for degradation is reached where it increases by almost three orders of magnitude.

Our approach to the reliability testing of GaN-on-Si HEMTs is similar to that followed in [1] and [2]. We perform electrical stress experiments under a variety of conditions. An automated benign characterization suite monitors important figures of merit (FOM) of the devices such as maximum drain current (I_{DMAX}), gate leakage current (I_{GOFF}), drain and source resistances (R_D, R_S) throughout the experiment. Measurements of FOM take place at predefined intervals and the stress is interrupted during these measurements. Figure 2 shows the output of the characterization suite for I_{DMAX}, I_{GOFF}, R_D and R_S for a GaN-on-Si HEMT. In this test, V_{DS}=0 V and constant whereas V_{GS} is stepped from -5 V to -60 V by 1 V steps every 10 seconds. This is a typical case where R_D and R_S increase and I_{DMAX} decreases with increased stress. I_{GOFF} first decreases due to increased trapping with stress until it experiences an almost three orders of magnitude increase around a stress voltage of 45 V. This increase is permanent and the voltage that this occurs is referred to the critical voltage for I_{GOFF} degradation, V_{CRIT}. This is the key signature of degradation due to the inverse piezoelectric effect.

REFERENCES

[1] J. Joh, "Degradation Mechanisms of GaN High Electron Mobility Transistors," SM thesis, MIT, 2007.
[2] A. A. Villanueva, "Electrical reliability of RF power GaAs PHEMTs," SM thesis, MIT, 2003.

RF Power CMOS for Millimeter-wave Applications

U. Gogineni, J. A. del Alamo
Sponsorship: SRC, Intel PhD Fellowship, IBM

Radio frequency (RF) power amplifiers are core components of almost all wireless systems. Traditionally III-V, SiC, or SiGe devices have been used in power amplifiers because of their ability to deliver high power and operate at high frequencies. Recently there has been an increased interest in using Si CMOS for designing single-chip integrated systems for operation in the millimeter-wave regime. Specific applications in this regime include wireless LAN and collision-avoidance radar. A key concern in using CMOS for these applications is the inability of CMOS to yield high-efficiency power amplifiers with power levels over 10 mW in the 60-80 GHz regime. In our work, we are investigating the fundamental limitations of using Si CMOS in power amplifiers and exploring options for device optimization with the goal of enhancing the millimeter-wave power-handling ability of Si CMOS.

Previous research in our group at MIT into the RF power performance of 65-nm and 90-nm Si CMOS devices [1], [2] has shown that the optimum device width that delivers the maximum power at any frequency (shown as open diamonds in Figure 1) scales down with increasing frequency. The effective cut-off frequency for power (frequency at which the output power drops below 10 mW) can be extrapolated to be around 20 GHz for 65-nm CMOS. Peak PAE and output power are strongly correlated to the maximum oscillation frequency (f_{max}) [1] and hence the decrease in output power for wide devices can be attributed mainly to a decrease in f_{max}.

To explain the f_{max} degradation in wide devices, small-signal equivalent circuits were extracted from the s-parameters measured on devices with different widths. The results show that the intrinsic parameters such as the transconductance (g_m) and intrinsic capacitances (C_{gs} and C_{gd}) are constant across width, but the extrinsic parasitic resistances (R_D and R_G) increase with increasing width. In this work, device width is increased by wiring multiple unit cells (each containing 24 fingers of 2 mm width) in parallel. The additional wiring between the cells results in higher parasitic resistances for the wider devices. Hence, the key to enabling CMOS for millimeter-wave power applications is a parasitic-aware approach to designing wide devices.

Several test structures with optimized parasitics have been designed and implemented on IBM's 65-nm and 45-nm CMOS technologies. Some of the design ideas being explored include (a) alternate ways of connecting elemental devices in parallel, and (b) use of multiple levels and thicker levels of metal to reduce interconnect resistance.

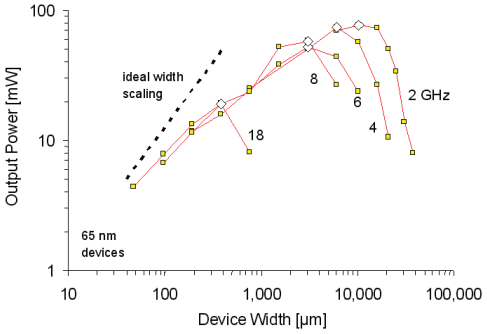


FIGURE 1: Maximum power (at peak PAE) vs. MOSFET width at different frequencies for 65-nm devices (V_{dd} =1 V) [1].

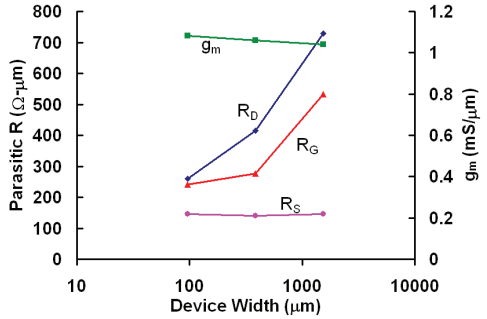


FIGURE 2: Normalized transconductance and parasitic resistances vs. device width for 65-nm devices (V_{dd}=1V, I_D=100mA/mm).

REFERENCES

[1] J. Scholvin, D.R. Greenberg, and J.A. del Alamo, "Fundamental power and frequency limits of deeply-scaled CMOS for RF power applications," in *Proceedings of International Electron Device Meeting 2006*, pp. 217-220.

[2] J. Scholvin, D.R. Greenberg, and J.A. del Alamo, "Performance and limitations of 65-nm CMOS for integrated RF power applications," in *Proceedings of International Electron Device Meeting 2005*, pp. 369-372.

Quantum Capacitance in Scaled-Down III-V HEMTs

D. Jin, J. A. del Alamo
Sponsorship: SRC/FCRP MSD, Intel Corporation

As Si CMOS fast approaches the end of the roadmap, finding a new transistor technology that would allow the extension of Moore's law has become a technical problem of great significance. Among the various candidates that are being contemplated, III-V-based Field-Effect Transistors represent a very promising technology due to the outstanding electron-transport properties of III-V compound semiconductors. In particular, InGaAs-based High-Electron-Mobility Transistors (HEMTs) fabricated at MIT exhibit great logic performance and constitute an excellent test bed to explore a future III-V CMOS technology [1].

In order to improve the logic performance of HEMTs, the barrier thickness needs to continue to scale down so as to maintain electrostatic integrity and enhance gate capacitance. However, as the barrier thickness approaches a few nanometers in thickness, the gate capacitance does not increase as much as expected as a result of the finite inversion-layer capacitance. This limit comes from two main contributions: finite quantum capacitance [2] and the centroid capacitance. The first one originates in the extra energy required to create a two-dimensional electron gas (2DEG) in a quantum well due to the finite density of states. The second one is related to the shape of the charge distribution in the inversion layer [3]. In scaled-down III-V HEMTs, due to the small effective mass of electrons in the channel, these two effects conspire to seriously limit the overall gate capacitance of the device and limit its current driving capability. Correct understanding of these effects and accurate modeling are essential to predicting the logic performance characteristics of future scaled III-V FETs.

In this research, we model the gate capacitance of HEMTs (Figure 1) and compare it with experimental measurements on devices fabricated at MIT (Figure 2). Using a one-dimensional Poisson-Schrodinger solver (Nextnano), we show that the overall gate capacitance of HEMTs can be modeled precisely as the series combination of an insulator capacitance and the inversion-layer capacitance. This one consists of a parallel combination of the contributions of each occupied electron subband. For each sub-band, the inversion-layer capacitance consists of the quantum capacitance (C_{Q_i}) and the centroid capacitance (C_{cent_i}), which are connected in series (Figure 1). We have performed S-parameter measurements and extracted the gate-capacitance characteristics of InGaAs HEMT structures with 4-nm barrier thickness in the linear regime [4]. The measurements agree very well with the modeled capacitance (Figure 2).

Our model suggests that in the operational range of these devices, the quantum capacitance significantly lowers the overall gate capacitance of the device. This research suggests that it is important to explore new ways to increase the quantum capacitance in order to develop scaled down III-V FETs with superior logic characteristics.

REFERENCES

[1] D-H. Kim and J.A. del Alamo, "Scaling behavior of $In_{0.7}Ga_{0.3}As$ HEMTs for Logic" *International Electron Devices Meeting Technical Digest*, pp. 837-840, Dec 2006

[2] S. Luryi, "Quantum capacitance devices" *Applied Physics Letter*, vol. 52, pp. 501-503, Feb 1988.

[3] H. S. Pal, J. D. Cantley, S. S. Ahmed, and M. S. Lundstrom, "Influence of Bandstructure and Channel Structure on the Inversion Layer Capacitance of Silicon and GaAs MOSFETs" *IEEE Transactions on Electron Devices*, vol. 55, pp. 904-908, Mar 2008

[4] D-H. Kim, to be published

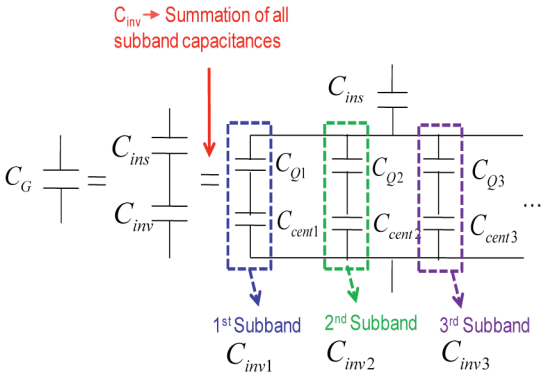


FIGURE 1: The gate-capacitance model used in this work. For each subband, the inversion-layer capacitance is the series of the quantum capacitance and the centroid capacitance.

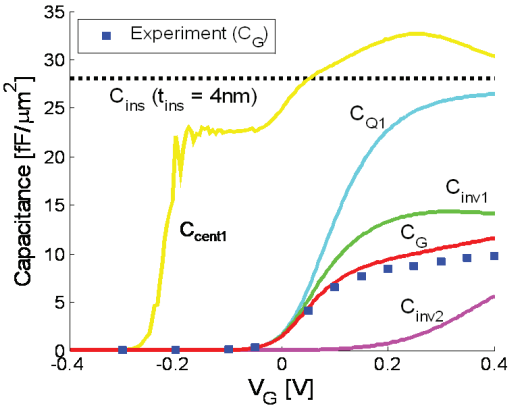


FIGURE 2: Experimental and modeled gate capacitance of 4-nm barrier thickness InGaAs HEMTs in the linear regime as a function of applied gate voltage. The 1st electron subband dominates in the HEMTs' operational range. The quantum capacitance severely brings down the overall gate capacitance.

RF Reliability of GaN High-electron-mobility Transistor

J. Joh, J. A. del Alamo in collaboration with TriQuint Semiconductor
Sponsorship: Army Research Laboratory (contract # W911QX-05-C-0087)

Thermally accelerated RF life tests (RFLT) are widely accepted as the most reliable ways to evaluate the lifetime of RF amplifiers in the field. However, RF life tests require a relatively complicated setup and an accurately determined and controlled device channel temperature, which is sometimes very difficult to achieve. The situation is particularly complex for high-power density technologies such as GaN high-electron-mobility transistors (HEMTs) or high-voltage GaAs-based devices. Also, in terms of understanding the physics of degradation, RFLT is somewhat cumbersome because a change in RF output power can result from a variety of different causes.

In order to overcome these complexities, DC life tests (DCLT) are often preferred due to their simplicity. In addition, during DCLT, better insight into failure mechanisms can be obtained by monitoring changes in various DC parameters such as the maximum drain current, I_{Dmax}, and the threshold voltage,V_T [1]. Though simple to implement, DC life tests have several limitations. First, the choice of stress bias conditions is not obvious. Second, DC life tests can at most only hope to emulate the DC conditions of the RF amplifier and not the impact of the RF waveform. Thus, they can be immune to some types of degradation (e.g., RF breakdown degradation) that could be present only under RF conditions. Third, DC life tests may not predict the lifetime under RF conditions if degradation of a wrong DC parameter that is irrelevant to RF power degradation is chosen as a failure criteria. It is then of great importance to establish a correlation between the degradation that is produced during DCLT and RFLT [2].

In this work, using TriQuint's X-Band GaN HEMT technology, we study how DC and RF figures of merit degrade during DC and RF stresses. Unlike conventional RF life tests in which only RF output power, P_{out}, and quiescent DC current, I_{DQ}, are monitored, we incorporated a characterization suite that extracts several DC parameters such as I_{DSS} (drain current at V_{GS}=0) and V_T in the RFLT. Under RF stress, it was found that I_{DSS} is a better indicator of P_{out} degradation than I_{DQ} (Figures 1 and 2). Similarly, during DCLT in which we regularly measure RF performance figures of merit, I_{DSS} degradation was found to correlate well with a drop in P_{out}. Other DC figures of merit such as I_{DQ} or V_T did not show a clear correlation with P_{out}. Also, we found that due to the larger voltage swing beyond the DC bias point, which prevails under large RF power input, RF stress can degrade GaN HEMTs much more than DC stress does even at the same V_{DS} and device channel temperature. In particular, the gate current can seriously degrade under RF stress, with a serious impact on P_{out}.

With this understanding of the correlation between DC and RF degradation, we can focus on DC figures of merit in DCLT that are more relevant to real RF output power degradation. This focus will help us understand physical degradation mechanisms of GaN HEMTs. Also, we can better design DC stress experiments that can accurately predict RF reliability.

REFERENCES

[1] J. Joh and J. A. del Alamo, "Mechanisms for electrical degradation of GaN high-electron mobility transistors," *IEEE IEDM Tech. Digest*, pp. 415-418, 2006.

[2] J. Joh, J. A. del Alamo, U. Chowdhury, and J. L. Jimenez, "Correlation between RF and DC reliability in GaN high electron mobility transistors," *ROCS Workshop Proceedings*, pp. 185-188, 2008.

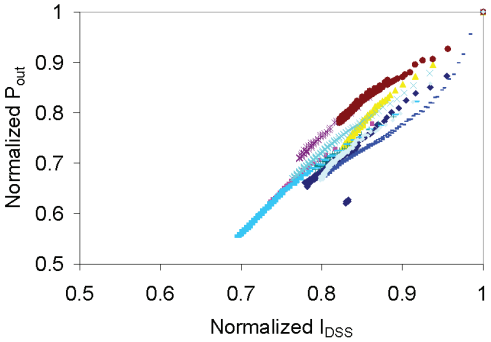


FIGURE 1: Correlation between degradation in P_{out} and I_{DSS} for 10 different devices from a single wafer.

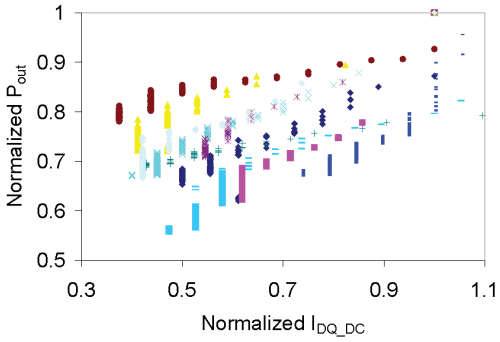


FIGURE 2: Correlation between degradation in P_{out} and I_{DQ_DC} for the same experiment in Figure 1.

Inverted-type InGaAs HEMTs for Logic Applications

T.-W. Kim, D. H. Kim, J. A. del Alamo
Sponsorship: SRC/FCRP MSD, Intel Corporation

As conventional CMOS scaling approaches the end of the roadmap, III-V-based FETs are seriously being considered as an alternative logic technology [1]. For any new device technology to take over the CMOS roadmap, electrical characteristics superior to those of Si CMOS are required in terms of performance (ON current and OFF current) and short-channel effects (evaluated through subthreshold swing and DIBL, among other figures of merit) at the required device dimensions [2]. The III-V high-electron-mobility transistor (HEMT) represents an excellent model system to study issues of relevance in future III-V MOSFETs. In order to gracefully scale into the deep sub-100-nm range, the barrier thickness (a wide bandgap semiconductor in the case of a HEMT) needs to be scaled down into the few-nm range. At MIT we are investigating InAlAs/InGaAs HEMTs with reduced InAlAs barrier thickness by three-step gate-recess process [3] and Pt-sinking-gate technology [4]. A drawback of a reduced barrier thickness is a large gate leakage current. In order to counteract this, we are currently investigating inverted-type InAlAs/InGaAs HEMTs where there are no dopants in the InAlAs barrier above the channel. The expected trapezoidal-shaped barrier should significantly reduce the gate leakage current level.

We have fabricated 30-nm gate-length inverted-type InAlAs/InGaAs HEMTs on InP substrate. The heterostructure was designed to have Si delta-doping layers both above and below the channel. In the intrinsic region of the device, the dopants are removed from the top barrier through a three-step gate recess process. In this way, a barrier thickness of 5 nm was achieved. Figure 1 shows the subthreshold characteristics of representative 30-nm inverted-type InGaAs HEMTs with typical conventional InGaAs. The inverted HEMTs exhibit a reduction in gate leakage current of around an order of magnitude when compared with conventional devices of similar dimensions. In addition, they show excellent short-channel effect characteristics with S = 66 mV/dec and DIBL = 80 mV/V. Figure 2 shows I_{ON}/I_{OFF} ratio as a function of gate length. The I_{ON}/I_{OFF} ratio of the inverted HEMTs is nearly 10^5 at V_{DD} = 0.5 V and it is fairly constant as the device scales down in size. These results reveal the benefits of the trapezoidal-shaped energy barrier under the gate. Unfortunately, there are drawbacks to this device design. These devices show a larger source resistance than conventional devices because of the high tunneling resistance associated with the higher energy barrier of the cap/barrier/channel region. The transconductance of 30-nm devices is 1.05 S/mm at V_{DS}=0.5 V and the source resistance is 0.39 Ω·mm, as extracted by the gate current injection method. For a process optimization, we hope to improve the performance of 30-nm inverted-type InAlAs/InGaAs HEMTs by reducing the parasitic resistances through a new ohmic contact scheme.

REFERENCES

[1] J. del Alamo and D.-H. Kim, "Beyond CMOS: Logic Suitability of InGaAs HEMTs," in *Indium Phosphide & Related Materials(IPRM)Proceeding*, pp. 14-18, May 2006.

[2] J. del Alamo and D.-H. Kim, "InGaAs CMOS: a "Beyond-the-Roadmap" Logic Technology?" in *Device Research Conference (DRC) Proceeding.*, pp. 201-202, June 2007.

[3] D.-H. Kim and J. del Alamo, "30-nm Pseudomorphic HEMTs on an InP Substrate With a Current-Gain Cutoff Frequency of 628 GHz," *IEEE Electron Device Letters, Vol. 29, No. 8, Aug. 2008.*

[4] D.-H. Kim and J. del Alamo, "30 nm E-mode InAs PHEMTs for THz and Future Logic Applications," in *Int. Electron Devices Meeting (IEDM) Tech. Dig.*, pp. 719-722, Dec. 2008.

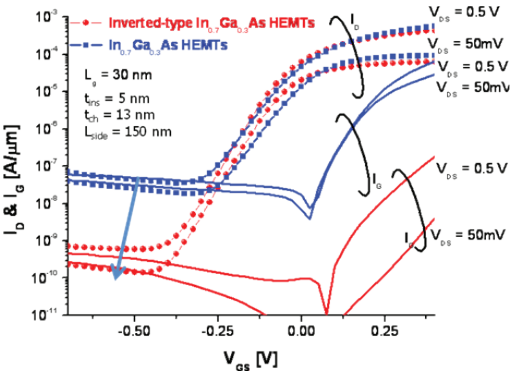


FIGURE 1: Subthreshold characteristics of inverted-type InGaAs HEMTs with conventional type InGaAs and channel normal HEMTs.

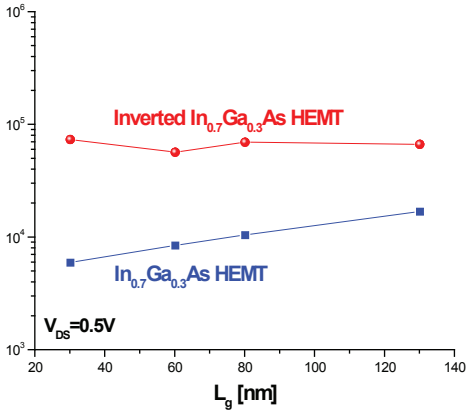


FIGURE 2: The I_{ON}/I_{OFF} ratio of inverted-type InGaAs HEMT and conventional InGaAs HEMTs as a function of gate length.

Impact of Strain on the Characteristics of InGaAs HEMTs

L. Xia, J. A. del Alamo
Sponsorship: SRC/FCRP MSD

With the incorporation of mechanical strain into the channel of Si MOSFETs, electron and hole mobilities have been improved by 2x and 3x, respectively, as compared with their unstrained counterparts [1], [2]. Just as with Si, it is of interest to study the impact of strain on the transport characteristics of InGaAs, a material that is currently receiving a great deal of attention as a post-Si CMOS logic technology. Our work studies the impact of strain on the electrostatics and transport properties of InGaAs High Electron Mobility Transistors (HEMTs).

We have fabricated a chip-bending apparatus that allows us to apply either tensile or compressive uniaxial strain to a small chip while conducting electrical measurements. Chips with size down to 2 mm x 4 mm can be accommodated. The strain level can be as high as +/-0.4%.

By applying unaxial strain to an n-channel InGaAs HEMT, we found that the threshold voltage shifts linearly with the applied strain, up to about 30 mV, as shown in Figure 1. This shift is due to the introduction of piezoelectric charge into the device due to in-plane strain and a change of the Schottky barrier height due to the hydrostatic pressure component. The linear regime transconductance also changes with strain. The underlying mechanism for this change is likely to be a combination of change in the electrostatic characteristics of the InGaAs quantum well and the mobility of 2DEG.

In parallel, we are fabricating our own p-channel III-V FETs in an effort to study the impact of mechanical strain on hole transport. We have developed a fabrication process for strain-free p-type $Al_{0.42}Ga_{0.58}As$/GaAs HEMTs. The saturation current and maximum transconductance of a 2-μm-long HEMT are 22 mA/mm and 16 mS/mm (at V_{DS}=-2 V), respectively. Figure 2 shows the output characteristics. However, the devices suffer from excessive gate leakage current that prevents them from being completely turned off. After solving this problem, we will be able to experimentally study the strain impact on p-channel III-V-based device performance.

REFERENCES

[1] J. R. Hwang, J. H. Ho, S. M. Ting, T. P. Chen, Y. S. Hsieh, C. C. Huang, Y. Y. Chiang, H. K. Lee, L. Ariel, T. M. Shen, G. Braithwaite, M. Currie, N. Gerrish, R. Hammond, A. Lochtefeld, F. Singaporewala, M. Bulsara, Q. Xiang, M. R. Lin, W. T. Shiau, Y. T. Loh, J. K. Chen, S. C. Chien, F. Wen, "Performance of 70 nm strained-silicon CMOS devices", Digest of Technical Papers. 2003 Symposium on, 2003, pp. 103-104.

[2] L. Washington, F. Nouri, S. Thirupapuliyur, G. Eneman, P. Verheyen, V. Moroz, L. Smith, X. Xiaopeng, M. Kawaguchi, T. Huang, K. Ahmed, M. Balseanu, X. Li-Qun, S. Meihua, K. Yihwan, R. Rooyackers, M. Kristin De, R. Schreutelkamp, "pMOSFET with 200% mobility enhancement induced by multiple stressors", Electron Device Letters, IEEE 27 (2006) 511-513.

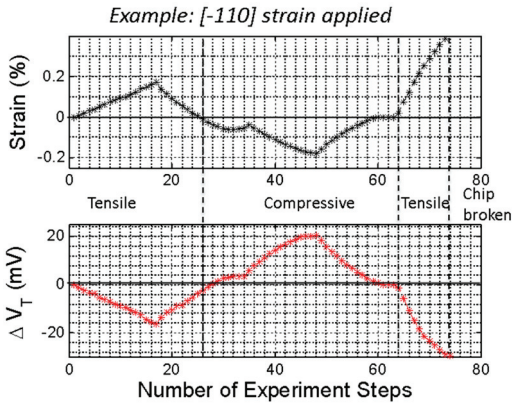


FIGURE 1: Threshold voltage (V_T) shift of n-type $Al_{0.23}Ga_{0.77}As$ / $In_{0.15}Ga_{0.85}As$ HEMT under strain. The V_T is defined as V_{GS} when I_{DS} = 1 mA/mm. Strain is applied parallel to the channel direction [-110].

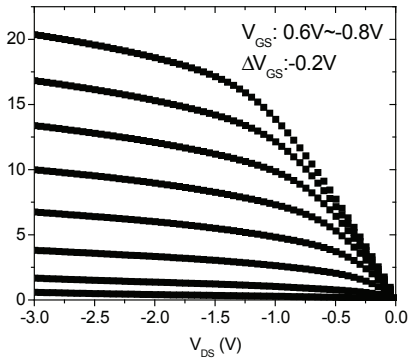


FIGURE 2: Output characteristics of p-type $Al_{0.42}Ga_{0.58}As$/GaAs HEMT. The gate length is 2 µm.

Advanced Substrate Engineering: Integration of InP Lattice Constant on Si

L. Yang, E. A. Fitzgerald
Sponsorship: SRC/FCRP MSD

Integration of the InP lattice constant with Si CMOS platforms is motivated by the monolithic interconnection of III/V optoelectronic and electronic devices with the highly integrated Si logic. However, integration of InP on Si requires a comprehensive solution that addresses lattice mismatch, thermal expansion mismatch, IV/III-V integration, and alloy engineering challenges.

We investigated III/V graded (Ñ) buffer on 6° offcut GaAs substrate in combination with 6° offcut Ge on Insulator (GOI) substrate to integrate InP on Si. First, we chose 6° offcut GOI as the substrate to accommodate the antiphase disorder in the IV/III-V integration [1] and established excellent GaAs epitaxy on the substrate with proper surface preparation. Then we investigated two paths to integrate InP on 6° offcut GaAs: GaAs/Ñ$In_xGa_{1-x}As$/Ñ$In_yGa_{1-y}P$/InP as shown in Figure 1 and GaAs/Ñ$GaAs_{1-x}Sb_x$/InP as shown in Figure 2. For the GaAs/Ñ$In_xGa_{1-x}As$/Ñ$In_yGa_{1-y}P$/InP path, we demonstrated the integration of InP on 6° offcut GaAs with a threading dislocation density (TDD) of $7.9x10^6$ /cm². The total Ñ$In_xGa_{1-x}As$/Ñ$In_yGa_{1-y}P$ buffer thickness is 4.0 um, which should be thin enough to avoid the cracking problem that can be caused by the thermal expansion mismatch between InP and Si. However, it was demonstrated that $GaAs_{1-x}Sb_x$ can be grown with compositions in the range of solid immiscibility [2]. We investigated GaAs/Ñ$GaAs_{1-x}Sb_x$/InP path to get InP lattice constant on 6° offcut GaAs. Ñ$GaAs_{1-x}Sb_x$ was gradually graded from GaAs to $GaAs_{0.51}Sb_{0.49,}$ which is lattice-matched to InP, and InP was deposited on top. The interface of $GaAs_{0.51}Sb_{0.49}$/InP still needs to be optimized to get good quality InP layer. For the next step, we will further optimize the GaAs/Ñ$GaAs_{1-x}Sb_x$/InP path and combine InP on GaAs together with GaAs on GOI to realize the integration of InP on Si.

REFERENCES

[1] S. M. Ting and E. A. Fitzgerald, "Metal-organic chemical vapor deposition of single domain GaAs on Ge/Ge_xSi_{1-x}/Si and Ge substrates," *Journal of Applied Physics*, vol 87, pp.2618-2628, March 2000.

[2] M. J. Cherng, G. G. Stringfellow, and R. M. Cohen, "Organometallic vapor phase epitaxial growth of $GaAs_{0.5}Sb_{0.5}$," *Applied Physics letters*, vol 44, pp.677-679, Jan. 1984.

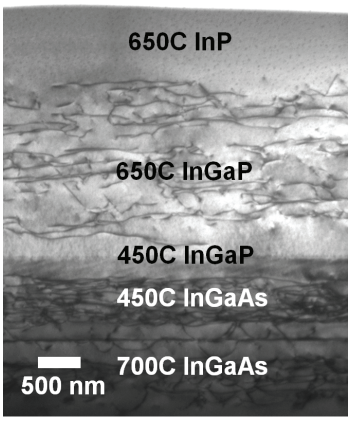


FIGURE 1: An XTEM of 6° offcut GaAs/ÑInx$Ga_{1-x}As$/Ñ$In_yGa_{1-y}P$/InP.

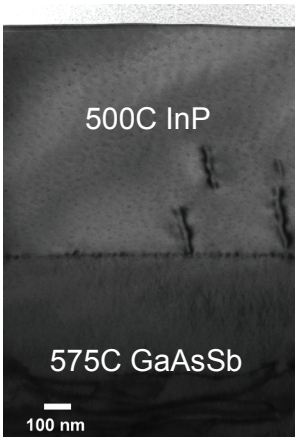


FIGURE 2: An XTEM of 6° offcut GaAs/Ñ$GaAs_{1-x}Sb_x$/InP.

Characteristics of Selectively Grown Ge-on-Si Photodiodes

N. DiLello, J. Yoon, M. Kim, J. Orcutt, J. L. Hoyt
Sponsorship: SRC student fellowship, DARPA

Germanium is a promising candidate for use in CMOS-compatible photodiodes. Its strong absorption in the 1.55-μm range and relative ease of integration on silicon substrates make it suitable for telecommunications systems and other high-speed electronic photonic integrated circuits. Important figures of merit for these photodiodes are the reverse leakage current and the responsivity. To reduce power consumption and improve the signal-to-noise ratio, the diodes must have a low leakage current in reverse bias and a high responsivity. This study has investigated the leakage current and responsivity of germanium photodiodes selectively grown by low-pressure chemical vapor deposition (LPCVD) using an Applied Materials epitaxial reactor.

To fabricate these diodes, germanium was grown selectively in oxide windows on a p+ Si substrate. The wafers then received an *in-situ* cyclic anneal to reduce the threading dislocation density. The wafers were subsequently implanted with phosphorus to create a vertical *pin* junction and contacted with metal. In this study, the Ge thickness was either 1 μm or 2 μm. The current vs. voltage characteristics for 100-μm square devices show that the dark current is ~250 nA at -1 V for both of these samples, as indicated in Figure 1. It has previously been noted that the threading dislocation density of Ge-on-Si films decreases with increasing thickness, indicating that film quality is better for thicker samples [1]. This suggests that Ge film quality is not the limiting factor in this case and more study is needed to further characterize the dark current. Figure 2 shows the responsivity vs. wavelength plot for both 1-μm- and 2-μm-thick samples. At -1 V and 1550 nm, the 1-μm sample and 2-μm sample have responsivities of 0.23 A/W and 0.46 A/W respectively. This 2x increase in responsivity is consistent with the increase in Ge thickness.

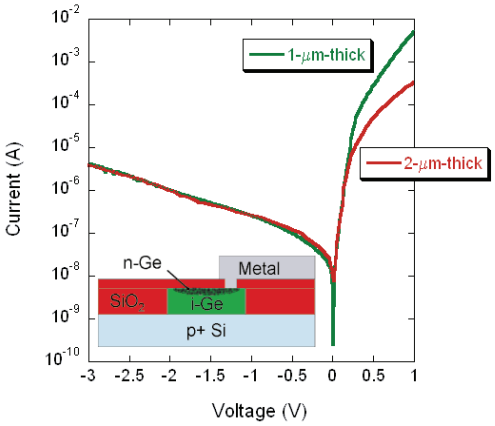


FIGURE 1: Current vs. voltage for a 1-µm-thick (green) sample and a 2-µm-thick (red) Ge sample. The dark current in reverse bias is virtually the same for both samples, suggesting that something other than material quality is limiting the leakage. Both devices are 100 µm square. Inset: Cross-sectional schematic diagram of a Ge-on-Si photodiode.

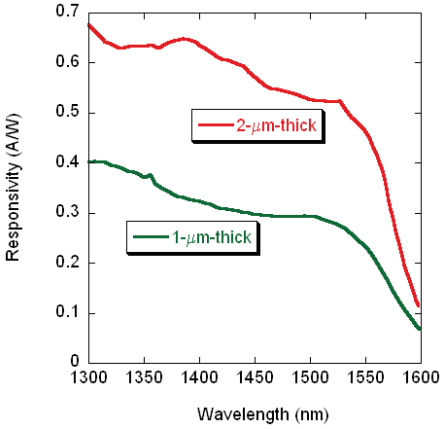


FIGURE 2: Responsivity as a function of wavelength for a 1-µm-thick (green) sample and a 2-µm-thick (red) Ge sample measured at a bias of -1 V. At 1550 nm, the responsivity of the thin sample is half of the responsivity of the thick sample. Both devices are 100 µm square.

REFERENCES

[1] M. Kim, O. Olubuyide, J. Yoon, and J.L. Hoyt, "Selective Epitaxial Growth of Ge-on-Si for Photodiode Applications," *ECS Transactions*, vol. 16, issue 10, pp. 837 – 847, 2008.

Scaled SiGe-channel p-MOSFETs on Insulator

L. Gomez, P. Hashemi, J. L. Hoyt
Sponsorship: SRC/FCRP MSD, MIT Lemelson Presidential Fellowship

Scaling of CMOS-device dimensions alone can no longer provide the necessary current drive enhancements required to continue historic performance gains. Strained-Si, SiGe, and Ge are under investigation as Si replacement technologies due to their enhanced carrier-transport properties [1]-[3]. Biaxial compressive strained-$Si_{0.45}Ge_{0.55}$ p-MOSFETs with gate lengths down to 65 nm have been fabricated to explore the merits of a strained-$Si_{0.45}Ge_{0.55}$ channel. Care was taken to avoid process steps that might alter or eliminate the strain in the channel. Hole mobility and velocity have been extracted and are benchmarked against a comparable Si control device. The dR/dL mobility extraction method was employed to determine the mobility of scaled p-MOSFETs with gate lengths in the range of 65-150nm [4]. Devices in this gate length range are observed to exhibit a 2.4x hole effective mobility enhancement over the Si hole universal mobility. Three velocity extraction methods were employed and the velocity characteristics of scaled strained-$Si_{0.45}Ge_{0.55}$ p-MOSFETs have been documented [5], [6]. A velocity enhancement is observed in stained-$Si_{0.45}Ge_{0.55}$ p-MOSFETs over control devices with a similar gate length and DIBL. The velocity enhancement is in the range of 1.1-1.3x. This enhancement is observed to increase with increasing proximity to the source injection point. Band structure and ballistic velocity calculations suggest that a substantial enhancement in velocity can be expected with the incorporation of Ge into the channel and the addition of uniaxial stress [7], [8]. Simulations predict that a moderate amount of Ge (e.g., $Si_{0.45}Ge_{0.55}$) coupled with -5 GPa of uniaxial stress can provide a velocity enhancement of 4.3x. This velocity is nearly two-fold larger than what Si is expected to provide with an equivalent amount of uniaxial stress.

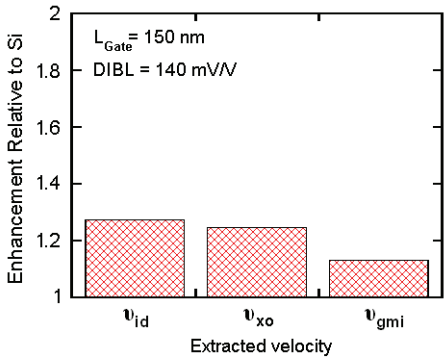


FIGURE 1: The enhancement relative to the Si control for the average υ_{id}, υ_{gmi}, and υ_{xo} extracted hole velocities. The strained-$Si_{0.45}Ge_{0.55}$ p-MOSFETs exhibit an enhancement over Si control devices ranging from 1.13-127x. All devices have an average L_{Gate} = 150 nm and DIBL = 140 mV/V.

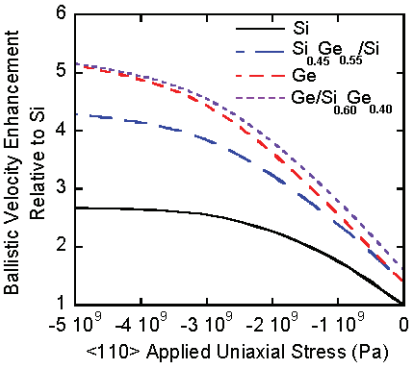


FIGURE 2: The simulated ballistic velocity enhancement relative to relaxed Si with applied compressive uniaxial stress for Si, biaxial compressive strained-$Si_{0.45}Ge_{0.55}$ pseudomorphic to relaxed-Si ($Si_{0.45}Ge_{0.55}$/Si), Ge, and biaxial compressive strained-Ge pseudomorphic to relaxed-$Si_{0.6}Ge_{0.4}$ (Ge/$Si_{0.6}Ge_{0.4}$). Simulations were performed using nextnano³ and FETtoy [7], [8].

REFERENCES

[1] S.W. Bedell, A. Majumdar, J.A. Ott, J. Arnold, K. Fogel, S.J. Koester, and D.K. Sadana, "Mobility Scaling in Short-Channel Length Strained Ge-on-Insulator P-MOSFETs," *IEEE Electron Device Letters*, vol. 29, no. 7, pp. 811-813, July 2008.

[2] S. Thompson, N. Anand, M. Armstrong, C. Auth, B. Arcot, M. Alavi, P. Bai, J. Bielefeld, R. Bigwood, J. Brandenburg, M. Buehler, S. Cea, V. Chikarmane, C. Choi, R. Frankovic, T. Ghani, G. Glass, W. Han, T. Hoffmann, M. Hussein, P. Jacob, A. Jain, C. Jan, S. Joshi, C. Kenyon, J. Klaus, S. Klopcic, J. Luce, Z. Ma, B. Mcintyre, K. Mistry, A. Murthy, P. Nguyen, H. Pearson, T. Sandford, R. Schweinfurth, R. Shaheed, S. Sivakumar, M. Taylor, B. Tufts, C. Wallace, P. Wang, C. Weber, and M. Bohr, "A 90 nm logic technology featuring 50 nm strained silicon channel transistors, 7 layer Cu interconnects, low k ILD, and 1 μm² SRAM Cell," in *IEDM Tech. Dig.*, 2002, pp. 61-64.

[3] M.L. Lee and E.A. Fitzgerald, "Optimized strained Si/strained Ge dual-channel heterostructures for high mobility P- and N-MOSFETs," in *IEDM Tech. Dig.*, 2003, pp. 18.1.1- 18.1.

[4] K. Rim, S. Narasimha, M. Longstreet, A. Mocuta, and J. Cai, "Low field mobility characteristics of sub-100 nm unstrained and strained Si MOSFETs," in *IEDM Tech. Dig.*, 2002, pp. 43.

[5] A. Lochtefeld and D.A. Antoniadis, "On Experimental Determination of Carrier Velocity in Deeply Scaled NMOS: How Close to the Thermal Limit?," *IEEE Electron Device Letters*, vol. 22, no. 2, Feb. 2001.

[6] A. Khakifirooz and D.A. Antoniadis, "Transistor Performance Scaling: The Role of Virtual Source Velocity and Its Mobility Dependence," in *IEDM Tech. Dig.*, 2006, pp. 1-4.

[7] nextnano³, NEXTNANO, Munich, Germany, 2007. Available: http://www.nextnano.de/

[8] FETtoy 2.0, nanoHUB, Purdue University, West Lafayette, IN, 2008. Available: https://nanohub.org/tools/fettoy/wiki

Uniaxial Strained-Si Gate-all-around Nanowire FETs

P. Hashemi, L. Gomez, J. L. Hoyt
Sponsorship: SRC/FCRP MSD, IBM Fellowship

Multi-gate device architectures such as tri-gate or Gate-all-around (GAA) nanowire (NW) MOSFETs are promising candidates for aggressively scaled Si-based CMOS due to their excellent electrostatics, low power consumption, and immunity to short channel effects [1], [2]. However, several effects such as quantum mechanical confinement effects and the non-ideality of the NW sidewalls play a significant role in degrading the performance of these devices. As a result, strain engineering of the Si NW channel is critical to improve device performance.

In this work, GAA strained-Si NW n-MOSFETs were fabricated using a top-down approach and their intrinsic and extrinsic performance was measured. Figure 1 shows a sample cross-section transmission electron microscopy image of a GAA strained-Si n-MOSFET, looking down the axis of the nanowires in the device channel, showing parallel nanowires with diameter ~ 8 nm, and LTO gate dielectric. Mobility of the GAA nanowires was extracted by measuring the intrinsic gate-channel capacitance using the split-CV method, after subtracting the parasitic capacitance measured on neighboring structures without NWs. The channel intrinsic conductance was corrected for series resistance. Figure 2 shows the electron effective mobility vs. average inversion charge density for ~49 nm-wide strained-Si GAA NWs, measured by both the 2-FET method and split CV, demonstrating excellent agreement between the two mobility extraction techniques. Universal (100) mobility and the mobility of planar SOI and SSDOI (t=8.7nm, close to the average thickness of strained-Si NW) and unstrained-Si NWs (W_{NW}=44nm) are also shown for comparison. The strained-Si nanowire shows mobility enhancement over universal, thin-body planar SOI and SOI NW devices (with the slightly smaller width of ~44nm).

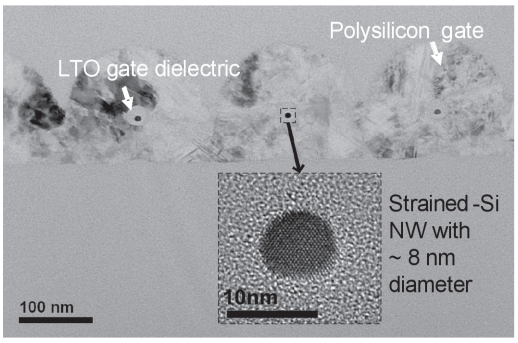


FIGURE 1: Cross-section transmission electron microscopy image of a GAA strained-Si n-MOSFET, looking down the axis of the nanowires in the device channel, showing parallel nanowires with diameter ~ 8 nm, and LTO gate dielectric [3].

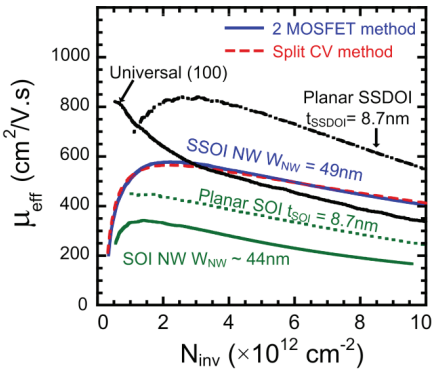


FIGURE 2: Low-field electron mobility (μ_{eff}) vs. average charge density (N_{inv}) of GAA strained-Si nanowire (W_{NW} = 49nm) measured by the split-CV and 2-FET methods. The μ_{eff} for the widest unstrained-Si nanowire (W=44nm), planar SOI, SSDOI (t=8.7nm), and universal are shown for comparison [4].

REFERENCES

[1] B. Doyle *et al.* "Tri-Gate Fully-Depleted CMOS Transistors: Fabrication, Design and Layout," in *VLSI Symp. Tech. Dig.*, 2003, pp. 133-134.

[2] S.-D. Suk *et al.* "High Performance 5nm radius Twin Silicon Nanowire MOSFET (TSNWFET): Fabrication on Bulk Si Wafer, Characteristics, and Reliability," in *IEDM Tech. Dig.*, 2005, pp. 735-738.

[3] P. Hashemi, L. Gomez, and J.L. Hoyt, "Gate-All-Around N-MOSFETs with Uniaxial Tensile Strain-Induced Performance Enhancement Scalable to Sub-10-nm Nanowire Diameter," *IEEE Electron Device Lett.*, vol. 30, no. 4, pp. 401-403, April 2009.

[4] P. Hashemi, L. Gomez, M. Canonico, and J.L. Hoyt "Electron Transport in Gate-All-Around Uniaxial Tensile Strained-Si Nanowire n-MOSFETs," in *IEDM Tech. Dig.*, 2008, pp. 865-868.

A Superconductivity Switch Constructed in an EuS/Al/EuS Sandwich Structure

G. X. Miao, C. H. Nam, C. A. Ross, J. S. Moodera
Sponsorship: NSF, ONR

Superconductivity is known to be tunable with spin-polarized carriers as the excess spins suppress the spin singlet state of Cooper pairing [1]. In this work we attempt to use a magnetic insulator to generate net spin accumulations in a thin superconducting Al layer. It was shown that the exchange interaction between the conduction electrons and the first ferromagnetic layer can lead to large spin-dependent variation in the superconducting transition temperatures [2]. We take advantage of such properties and show that large Zeeman splitting is indeed generated inside the thin Al layer, and that the Al film can be driven back and forth between its normal state and superconducting state with an external field, leading to virtually infinite magnetoresistance (Figure 1). When the lateral dimension of the structure is reduced (for example, see structures in Figure 2), we start to see very complicated magnetic responses, as a result of the domain wall formation and propagation. Our current study focuses mainly on the effect of domain walls on superconductivity and the use of nanoconstrictions in tuning the resulted magnetoresistance.

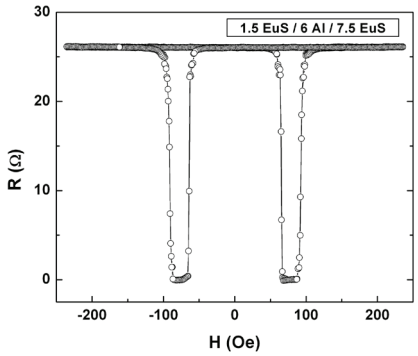


FIGURE 1: Illustration of the superconducting switch behavior in an unpatterned sandwich sample with the structure (in nm): glass/1 Cr/ 1.5 EuS/6 Al/7.5 EuS/15 Al_2O_3.

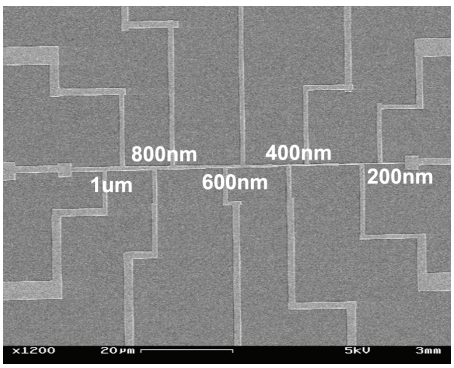


FIGURE 2: An SEM image of e-beam patterned nanostrips. A single lift-off step is used in its fabrication.

REFERENCES

[1] G. X. Miao, K. S. Yoon, T. S. Santos, J. S. Moodera, "Influence of spin-polarized current on superconductivity and the realization of large magnetoresistance," *Physical Review Letters*, vol. 98, pp. 267001:1-4, June 2007.

[2] P. G. de Gennes, "Coupling between ferromagnets through a supercnducting layer," *Physics Letters*, vol. 23, pp. 10-11, Oct. 1966.

Charge Transport Studies in Single-crystal Organic Field-effect Transistors

K. V. Raman, J. S. Moodera
Sponsorship: ONR, KIST

The research is motivated by the current development in the field of organic electronics [1]. Organic materials provide cheap, low-cost, mechanically flexible, and chemically tunable devices with performances comparable to or even better than amorphous Si. Also, these materials possess relatively good spin-transport properties [2-4], generating significant interest in these materials.

We have investigated charge transport in single crystals of organic semiconductor (OS), rubrene, with ferromagnetic electrode (FM) viz Co in addition to the conventional Au electrodes. Unlike that of gold, the surface stability of these electrodes to air is crucial and requires smart processing and fabrication steps to have clean FM-OS interfaces. A thin layer of Al (~ 6-10Å, grown at low temperature (80K)) was used to protect the Co surface and was found to give lower contact resistance. On exposure to air, an Al_2O_3 layer is formed that serves as a good tunnel barrier for charge injection. Figure 1 shows the four terminal-transfer characteristics of our FET devices. A mobility of $2cm^2/V\text{-}s$ is reported with the observation of source-drain current saturation at higher gate bias, attributed to the strong columbic interactions of the polaron charge carriers in the accumulation layer. Such effects have been reported before in high -dielectrics like Ta_2O_3 [5]. However, our results show that by considerably increasing the charge density (in our case by having large gate capacitance $C_i \sim 35nF/cm^2$), these effects show up. To further confirm the origin of such effect to the intrinsic nature of charges in rubrene, measurements were performed using Au electrodes, as shown in Figure 2, showing similar results. This work tries to gain fundamental understanding of the complex charge-transport mechanisms in organic materials and also for the proposed research goal of injection-spin information in these materials.

We would like to acknowledge Professor Marc Baldo (EECS) and his graduate student Carlijn Mulder for helping us use their organic growth facility.

REFERENCES

[1] S.R. Forrest, "Ultra-thin Organic Films Grown by Organic Molecular Beam Deposition and Related Techniques," Chem. Rev., vol. 97, pp. 1793-1896, 1997.

[2] Z. H. Xiong, Di Wu, Z. Valy Vardeny & Jing Shi, "Giant magnetoresistance in organic spin-valves," Nature, vol. 427, pp. 821-824, 2004.

[3] T.S. Santos, J. S. Lee, P. Migdal, I.C. Lekshmi, B. Satpati, and J. S. Moodera, "Room-temperature tunnel magnetoresistance and spin-polarized tunneling through an organic semiconductor barrier," Phys. Rev. Lett., vol. 98, 016601, 2007.

[4] Ö. Mermer, G. Veeraraghavan, T. L. Francis, Y. Sheng, D. T. Nguyen, M. Wohlgenannt, A. Köhler, M. K. Al-Suti, and M. S. Khan, "Large magnetoresistance in nonmagnetic π-conjugated semiconductor thin film devices ," Phys. Rev. B, vol. 72, 205202, 2005.

[5] S Fratini et al, "Current saturation and Coulomb interactions in organic single-crystal transistors," New J. Phys., vol. 10, 033031, 2008.

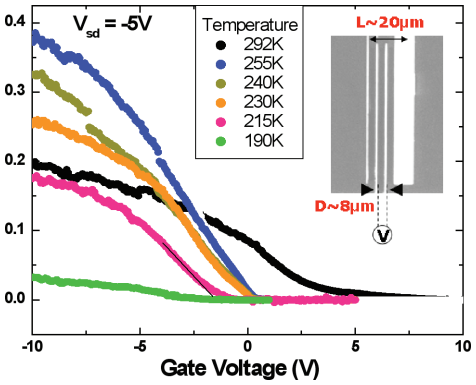


FIGURE 1: Surface conductivity vs gate voltage measured at different temperatures for Co/Al electrodes. Inset shows the 4-terminal electrode geometry (L– channel length, D- distance between the sense leads). Current saturation at high gate bias is observed and becomes stronger at lower temperatures.

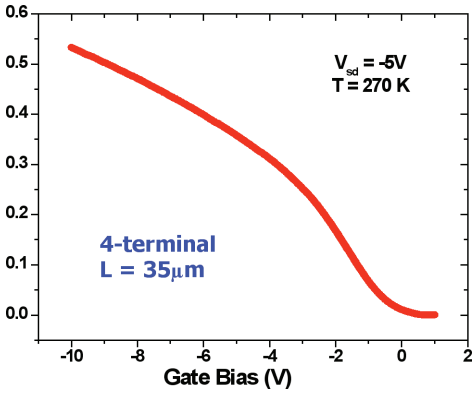


FIGURE 2: Surface conductivity vs. gate bias measured using Au electrodes. Current saturation is confirmed to originate due to the intrinsic nature of charge-carriers in rubrene.

Silicon and Silicon-Germanium Magnetic-tunneling-emitter Bipolar Transistors

M. van Veenhuizen, D. Choi, J. Chang, Y.-H. Xie, J. Moodera
Sponsorship: DARPA, KIST-MIT

We investigate a novel approach to spin-injection, based on the bipolar junction transistor, that has the potential to generate the large spin-currents inside the silicon needed to make functional spin-devices. Specifically, we employ the tunneling-emitter bipolar transistor with the emitter contact being a ferromagnet, as a spin-injection device. Tunneling-emitter bipolar transistors with a metallic emitter have been fabricated before [1], but never with the metal being a ferromagnet. We have successfully fabricated working transistors out of silicon, and Figure 1 shows an SEM micrograph of a device [1]. We find, however, that the current gain is very low, as seen in Figure 2 [2]. As we describe in [2], this can be attributed to recombination at the oxide-silicon interface due to the imperfect tunnel-barrier. Our current focus is on improving the tunnel-barrier quality. In addition, we are working on integrating this spin-injection device into a silicon-germanium heterostructure in order to inject spin into a silicon quantum well. The high-mobility quantum well has a very long spin-coherence length and the 2d confinement allows for the fabrication of functional spin-devices, as for instance the Datta-Das transistor [3].

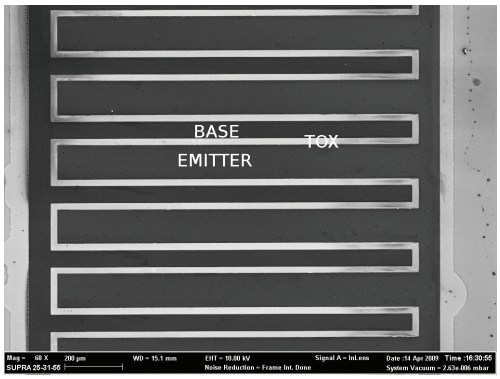


FIGURE 1: An SEM micrograph of a tunneling-emitter bipolar transistor. The base and emitter contacts consist of alternating long stripes, separated by a thermal oxide (TOX). The emitter consists of a ferromagnet/tunnel-barrier stack; for this device, iron/magnesium-oxide.

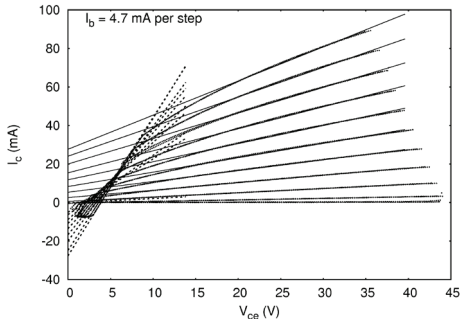


FIGURE 2: Collector current versus collector-emitter voltage for different base currents for the device shown in Figure 1 [1]. The current gain h_{FE} of the device is only slightly above 1. Also shown are fits to the initial and final slopes. The substantial final slope value is a result of the very thin base width, approximately 1000 Å.

REFERENCES

[1] H. Kisaki, "Tunnel transistor," PROC IEEE, vol. 61, pp. 1053-1055, 1973
[2] M. van Veenhuizen, J. Chang, J. Moodera, "Fabrication and analysis of Fe/MgO/Silicon tunneling emitter bipolar transistors", submitted to Journal of Applied Physics
[3] S. Datta and B. Das, "Electronic analog of the electro-optic modulator," Appl. Phys. Lett., vol. 56, pp. 665-668, 1990

AlGaN/GaN Nanowire HEMTs

M. Azize, T. Palacios
Sponsorship: ONR

The high-frequency performance of $Al_xGa_{1-x}N$/GaN high-electron-mobility transistors (HEMTs) has rapidly increased in recent years. Transistors with current gain cut-off frequencies (f_T) above 160 GHz and power gain cut-off frequencies (f_{max}) of more than 200 GHz have been reported [1], [2], which enables the use of these devices in power amplifiers for mm-wave applications. In spite of these excellent results, the frequency performance of these devices is still far from its theoretically limit. Access resistances as well as short channel effects are currently limiting this performance. In this project, we are developing nanowire-based nitride HEMTs to overcome these limitations and to explore the maximum frequency of nitride devices [3].

Our work is based on the top-down fabrication of GaN nanowires on AlGaN/GaN structures grown by metallorganic chemical vapor deposition (MOCVD) on Si substrates. E-beam lithography is used to fabricate define nanowires with diameters (d) in the 30-200 nm range. After patterning of the nanowire, the sample is etched in a Cl_2-based dry-etching systems. Figure 1 shows a scanning electron micrograph of a typical device with $Al_xGa_{1-x}N$/GaN nanowires fabricated between the drain and source contacts. Preliminary measurements of these devices show an important improvement in the contact resistance as the nanowire diameter is decreased down to 50 nm (Figure 2), as well as negligible degradation in the transport properties. These low-contact resistances, in combination with the high electrostatic integrity and material quality of nanowire structures, are expected to render excellent frequency performance.

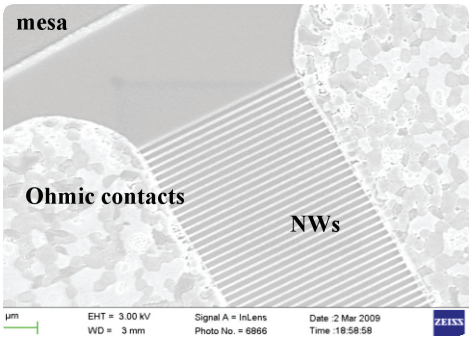


FIGURE 1: Scanning electron microscopy of AlGaN/GaN nanowires between two ohmic contacts. The diameter and the pitch of the nanowires are 60 nm and 170 nm, respectively.

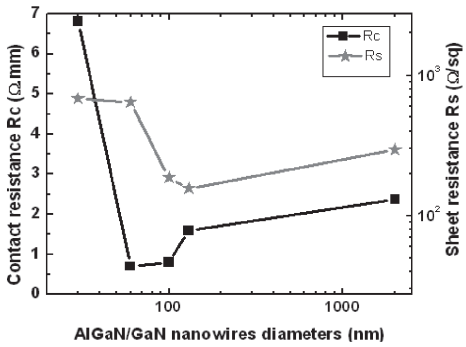


FIGURE 2: Contact and sheet resistances as function of the AlGaN/GaN nanowire diameter.

REFERENCES

[1] M. Higashiwaki, T. Mimura and T. Matsui, "30-nm-Gate AlGaN/GaN Heterostructure Field-Effect Transistors with a Current-Gain Cutoff Frequency of 181 GHz," *Japanese Journal of Applied Physics*, vol 45 pp. 1111-1113, 2006.

[2] T. Palacios, A. Chakraborty, S. Heikman, S. Keller, S. P. DenBaars, and U. K. Mishra, "AlGaN/GaN high electron mobility transistors with InGaN back-barriers," *IEEE Electron Device Letters*, vol 27, pp. 13–15, 2006.

[3] Y.Li, J.Xiang, F.Qian, S.Gradecak, Y.Wu, H.Yan, D.A. Blom, and C. M. Lieber, "Dopant-Free GaN/AlN/AlGaN Radial Nanowire Heterostructures as High Electron Mobility Transistors," *Nanotechnology Letters*, vol. 6, pp 1468–1473, 2006.

Seamless On-wafer Integration of GaN HEMTs and Si(100) MOSFETs

J. W. Chung, J. Lee, E. L. Piner, T. Palacios
Sponsorship: DARPA YFA, SRC/FCRP IFC, KFAS

The integration of III-V compound semiconductors and silicon (100) CMOS technologies has been a long-pursued goal. A robust low-cost heterogeneous integration technology would make the outstanding analog and mixed-signal performance of compound semiconductor electronics available on an as-needed basis to realize key functions on VLSI chips that are difficult to implement in Si technology. The GaN-based devices are one of the best candidates for the integration with Si. While Si electronics has shown unsurpassed levels of scaling and circuit complexity, GaN devices offer excellent high-frequency/power performance as well as outstanding optoelectronic properties. The ability to combine these two material systems in the same chip and in very close proximity would allow unprecedented flexibility for advanced applications. In this project, we demonstrate the first on-wafer integration of AlGaN/GaN high-electron-mobility transistors (HEMTs) with Si(100) MOSFETs.

The key enabling technology is the fabrication of a *Si(100)-GaN-Si(100) virtual substrate* (Figure 1) through a wafer bonding and etch-back process described in [1]. On this substrate, a standard Si MOSFET was first fabricated. Then, the top Si layer was locally removed, exposing the AlGaN surface, and GaN HEMT devices were fabricated in those regions (Figure 2). It should be highlighted that in our technology, the Si devices are fabricated on Si(100) without any miscut and following a conventional Si process flow. Due to the very high thermal stability of GaN, the Si process did not affect the electrical properties of the embedded GaN layer.

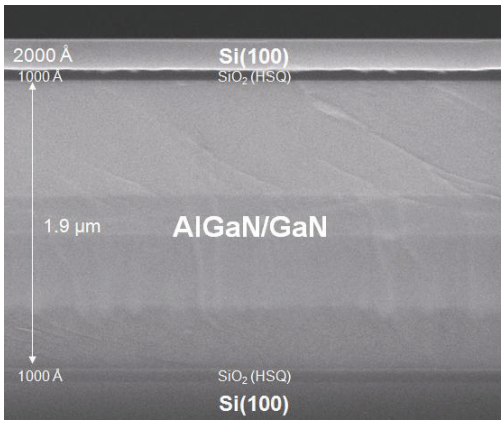


FIGURE 1: A cross-section scanning electron microscope (SEM) image of *Si(100)-GaN-Si(100) virtual substrate* through the layer transfer technology described in [1].

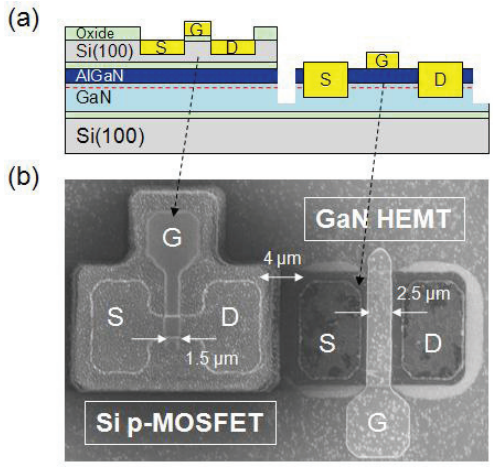


FIGURE 2: a) A cross-section schematic of fabricated Si p-MOSFETs and GaN HEMTs. b) A top SEM view of the fabricated transistors.

REFERENCES

[1] J. W. Chung, J. Lee, E. L. Piner, and T. Palacios, "Seamless on-wafer integration of GaN HEMTs and Si(100) MOSFETs," to be presented at *67th Annual Device Research Conference*, University Park, PA, Jun. 2009.

AlGaN/GaN Vertical Power Transistors

B. Lu, T. Palacios
Sponsorship: Deshpande Center for Technological Innovation, MIT Energy Initiative

Due to the high critical electric field (more than 3MV/cm) and high density and mobility 2-dimensional electron gas (2DEG) induced by polarization charges, AlGaN/GaN transistors have attracted great interest for use in high-power electronics. As shown in Figure 1, AlGaN/GaN high-electron-mobility transistors (HEMTs) have already exceeded the theoretical performance limit of Si power transistors and they are approaching the limit of SiC.

Most AlGaN/GaN HEMTs are horizontal devices [1]. However, in high voltage applications, vertical transistors are highly preferred due to their lower parasitic inductance, higher blocking voltage, and smaller size. There have been several reports on GaN vertical transistors such as the current aperture vertical electron transistor (CAVET) [2] and the vertical trench gate GaN MOSFET [3], but they all suffer from either high leakage current or poor channel mobility. Moreover, they were fabricated on expensive bulk GaN substrate, which makes their commercialization very challenging.

In this project, we are developing a new approach to fabricate vertical AlGaN/GaN power transistors based on substrate removal and wafer-transfer technology. These new devices combine the excellent transport properties of horizontal transistors with the high power-handling capability of vertical devices. In addition, these new devices provide at least a 10-fold reduction in fabrication cost. Figure 2 shows the I-V curves of our first generation vertical AlGaN/GaN transistors

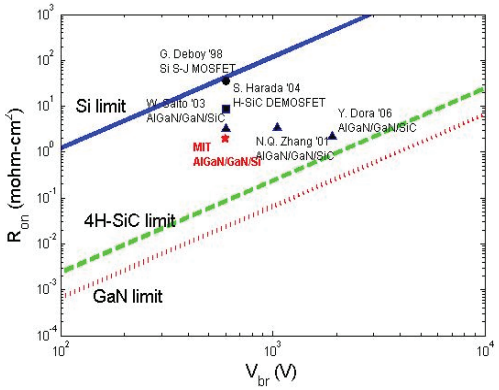


FIGURE 1: Blocking voltage (V_{br}) vs. on resistance (R_{on}) for Si, 4H-SiC and GaN with experimental data comparing the state-of-art Si super-junction MOSFET, SiC DEMOSFET, and AlGaN/GaN HEMTs.

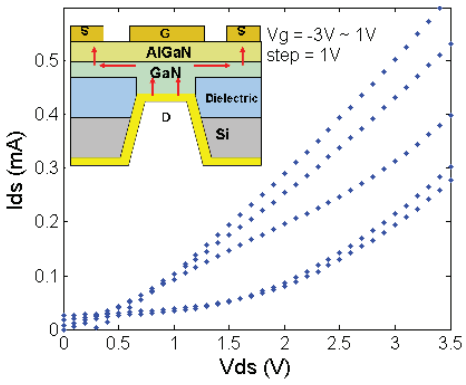


FIGURE 2: The V_{ds} - I_{ds} curve of our first-generation vertical AlGaN/GaN transistor and a schematic of the current flow in the transistor.

REFERENCES

[1] Y. Dora, A. Chakraborty, L. McCarthy, S. Keller, S. P. Denbaars, and U. K. Mishra, "High breakdown voltage achieved on AlGaN/GaN HEMTs with integrated slant field plates," IEEE Electron Device Lett., vol. 27, no. 9, pp. 713-715, Sep. 2006.

[2] S. Chowdhury, B. L. Swenson, and U. K. Mishra, "Enhancement and Depletion Mode AlGaN/GaN CAVET with Mg-Ion-Implanted GaN as Currrent Blocking Layer," IEEE Electron Device Lett., vol. 29, no. 6, June 2008.

[3] H. Otake, K. Chikamatsu, A. Yamaguchi, T. Fujishima, and H. Ohta, "Vertical GaN-Based Trench Gate Metal Oxide Semiconductor Field-Effect Transistors on GaN Bulk Substrates," The Japan Society of Applied Physics, Applied Physics Express 1, (2008) 011105.

AlGaN/GaN Vertical Power Transistors

B. Lu, T. Palacios
Sponsorship: Deshpande Center for Technological Innovation, MIT Energy Initiative

AlGaN/GaN high-electron-mobility-transistors (HEMTs) have attracted great interests for use in high-power electronics, due to their high critical electric field and high density and high mobility 2-dimensional electron gas (2DEG) induced by polarization of the AlGaN/GaN material system [1]. As shown in Figure 1, AlGaN/GaN high-electron-mobility transistors (HEMTs) have already exceeded the theoretical performance limit of Si power transistors and they are approaching the limit of SiC.

Most AlGaN/GaN HEMTs are horizontal devices [2]. However, in high voltage applications, vertical transistors are highly preferred due to their lower parasitic inductance, higher blocking voltage, and smaller size. There have been several reports on GaN vertical transistors such as the current aperture vertical electron transistor (CAVET) [3] and the vertical trench gate GaN MOSFET [4], but they all suffer from either high leakage current or poor channel mobility. Moreover, they were fabricated on expensive bulk GaN substrate, which makes their commercialization very challenging.

In this project, we are developing a new approach to fabricate vertical AlGaN/GaN power transistors based on substrate removal and wafer-transfer technology. These new devices combine the excellent transport properties of horizontal transistors with the high power-handling capability of vertical devices. In addition, these new devices provide at least a 10-fold reduction in fabrication cost. Figure 2 shows the I-V curves of our first generation vertical AlGaN/GaN transistors

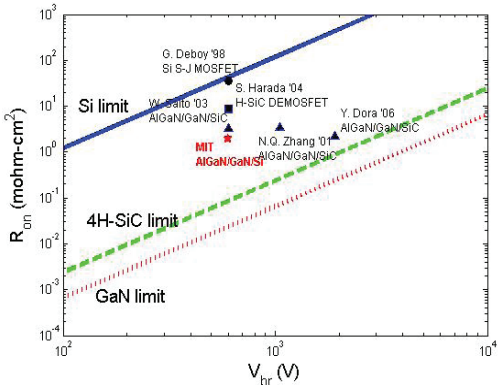


FIGURE 1: Blocking voltage V_B vs. on resistance R_{on} for Si, 4H-SiC and GaN with experimental data comparing the state-of-art Si super-junction MOSFET, SiC DEMOSFET, and AlGaN/GaN HEMTs.

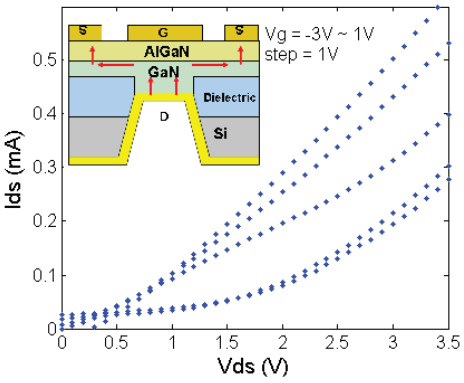


FIGURE 2: The V_{ds} - I_{ds} curve of our first-generation vertical AlGaN/GaN transistor and a schematic of the current flow in the transistor.

REFERENCES

[1] O. Ambacher, B. Foutz, J. Smart, J. R. Shealy, N. G. Weimann, K. Chu, M. Murphy, A. J. Sierakowski, W. J. Schaff, and L. F. Eastman, R. Dimitrov, A. Mitchell, and M. Stutzmann, "Two dimensional electron gases induced by spontaneous and piezoelectric polarization in undoped and doped AlGaN/GaN heterostructures", J. Appl. Phys., vol. 87, no. 1, Jan. (2000)

[2] Y. Dora, A. Chakraborty, L. McCarthy, S. Keller, S. P. Denbaars, and U. K. Mishra, "High breakdown voltage achieved on AlGaN/GaN HEMTs with integrated slant field plates," IEEE Electron Device Lett., vol. 27, no. 9, pp. 713-715, Sep. 2006.

[3] S. Chowdhury, B. L. Swenson, and U. K. Mishra, "Enhancement and Depletion Mode AlGaN/GaN CAVET with Mg-Ion-Implanted GaN as Currrent Blocking Layer," IEEE Electron Device Lett., vol. 29, no. 6, June 2008.

[4] H. Otake, K. Chikamatsu, A. Yamaguchi, T. Fujishima, and H. Ohta, "Vertical GaN-Based Trench Gate Metal Oxide Semiconductor Field-Effect Transistors on GaN Bulk Substrates," The Japan Society of Applied Physics, Applied Physics Express 1, (2008) 011105.

Self-aligned AlGaN/GaN HEMTs

O. I. Saadat, J. W. Chung, T. Palacios
Sponsorship: M/A-COM, ONR

Applications like anti-collision car radars and point-to-point wireless transmitters stand to benefit greatly from the development of compact solid-state amplifiers at frequencies above 30 GHz. The AlGaN/GaN HEMTs are uniquely suited for such applications because of their high electron velocity, current density, and critical electric field. To increase the frequency performance of these devices, it is important to reduce not only the gate length but also the source and drain access resistances by minimizing the distances between the source and gate and the drain and gate contacts, respectively [1]. We are currently developing a new fabrication technology to self-align the gate contact to the ohmic contacts to minimize these distances.

In order to fabricate self-aligned HEMTs, T-shaped gates, like the one shown in Figure 2a, are fabricated by using e-beam lithography. Then, these gates are used as a shadow mask for a blanket ohmic metal deposition, which is then followed by the 870°C anneal. A proposed structure is shown in Figure 2b. This technology requires that the gate survives the standard ohmic annealing at 870°C. However, AlGaN/GaN HEMTs are normally fabricated with gate stacks composed of Ni-Au-Ni, which are not able to survive the ohmic metal anneal [2]. Therefore, in this project we have developed a new gate stack technology that can survive the 870°C ohmic anneal thanks to a combination of high-k gate dielectrics and tungsten, a refractory metal.

The new gate stacks developed in these process are also able to improve the transport properties of the AlGaN/GaN transistors. We studied the effect of different dielectrics on device performance by fabricating and testing W-dielectric HEMTs with Al_2O_3 and HfO_2 of different thicknesses along a W-dielectric HEMT with combination of a thin Ga_2O_3 interface layer with 12 nm of HfO_2. As shown in Figure 1, these devices have up to 20% higher transconductance than a standard HEMT with a Ni-Au-Ni gate stack. Due to the reduced gate leakage, positive gate voltages can be applied and drain current densities of up to 960 mA/mm can be achieved, which is a 40% improvement over a standard HEMT with a Ni/Au/Ni gate.

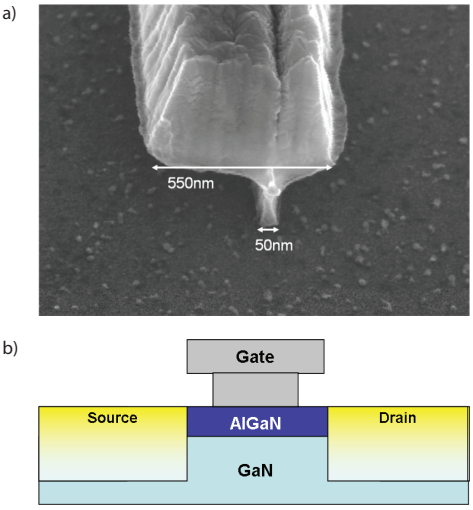


FIGURE 1: a) Scanning electron micrograph of an AlGaN/GaN HEMT with a 50-nm Ni/Au/Ni gate fabricated at MTL. b) Proposed structure with T-shaped gate and blanket ohmic metal deposition.

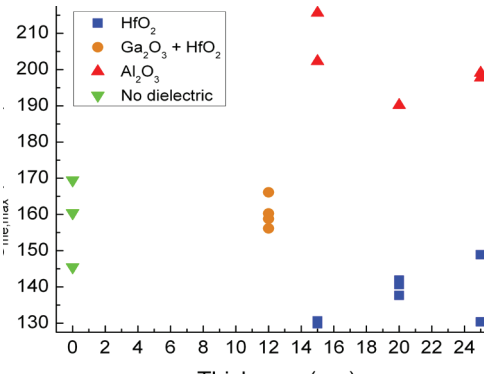


FIGURE 2: Transconductance vs. thickness for different dielectric thicknesses. Devices with the W-dielectric gate stack have up to 20% higher transconductance than devices with the standard Ni-Au-Ni gate stack.

REFERENCES

[1] P.J. Tasker and B. Hughes, "Importance of source and drain resistance to the maximum fT of Millimeter-Wave MODFET's," *IEEE Electron Device Letters*, vol. 10, no. 7, pp. 291-293, July 1989.

[2] T. Palacios, A. Chakraborty, S. Rajan, C. Poblenz, S. Keller, S. P. DenBaars, J. S. Speck, and U. K. Mishra, "High-Power AlGaN/GaN HEMTs for Ka-Band Applications," *IEEE Electron Device Letters*, vol. 26, no. 11, pp.781-783, Nov. 2005

New Technologies for High-frequency GaN Transistors

H. Wang, T. Palacios
Sponsorship: ONR

The development of compact solid-state transistors at frequencies in the THz range (300 GHz-3 THz) can open the door to many exciting applications. THz imaging, concealed-weapon detection, ultra-high-speed point-to-point wireless transmitters, and highly efficient radars for the military are only a few of the many applications that would benefit from these devices. In this project, we explore new device structure and fabrication techniques to enable such transistors and related applications.

The GaN-based high-electron-mobility transistors (HEMTs) are one of the most promising options for power amplification and high-speed operations at frequencies above 150 GHz [1]. Reducing the gate length is crucial for increasing high-frequency performance; however, it becomes increasingly difficult to fabricate ultra-short gate-length devices. The smallest transistor gate reported in the literature for a HEMT is 22 nm [2]. In this project, we aim to shrink the gate length to sub-10 nm dimensions.

In parallel to the conventional method of defining small T-shape gates by using electron beam lithography, we also use carbon nanotubes (CNT) gates (Figure 1) as transistor gates. Single-wall CNTs can combine diameters as small as 2 nm [3] with very low resistivity.

In addition to the gate length, the distance between the gate and the channel is a critical dimension that strongly affects the frequency performance of transistors. Conventional AlGaN/GaN HEMTs need a relatively thick layer of AlGaN (>20 nm) to induce sufficient electrons in the channel. In this project, we use InAlN and AlN as the barrier layers. Both materials allow sub-10 nm gate-channel separation while providing high electron concentration. A recent InAlN/GaN HEMT with an 8.9-nm InAlN barrier, L_g=100 nm and L_{ds}=2.5 μm, fabricated in MTL shows current densities above 2.3 A/mm (Figure 2) at V_G=+2 V.

REFERENCES

[1] T. Palacios, A. Chakraborty, S. Heikman, S. Keller, S.P. DenBaars, and U.K. Mishra, "AlGaN/GaN high electron mobility transistors with InGaN back-barriers," IEEE Electron Device Letters, vol. 27, no. 1, Jan 2006, pp. 13-15.

[2] S. Bentley, X. Li, D.A.J. Moran, and I.G. Thayne, "Fabrication of 22 nm T-gates for HEMT applications," *Microelectronic Engineering*, vol 85, Issues 5-6, June 2008, pp. 1375-1378.

[3] J. Kong, H. T. Soh, A. M. Cassell, C. F. Quate, and H. Dai, "Synthesis of individual single-walled carbon nanotubes on patterned silicon wafers," *Nature,* 395, 878-881, Oct 1998.

[4] X. Wang, Y. Ouyang, X. Li, H. Wang, J. Guo, and H. Dai, "Room Temperature All Semiconducting sub-10nm Graphene Nanoribbon Field-Effect Transistors," *Physics Review Letters*, in press, arXiv:0803.3464v2.

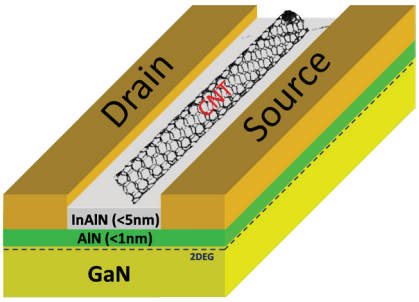


FIGURE 1: Envisioned HEMT with carbon nanotube gates. The effective gate length is much smaller than the diameter of the CNT due to its cylindrical shape.

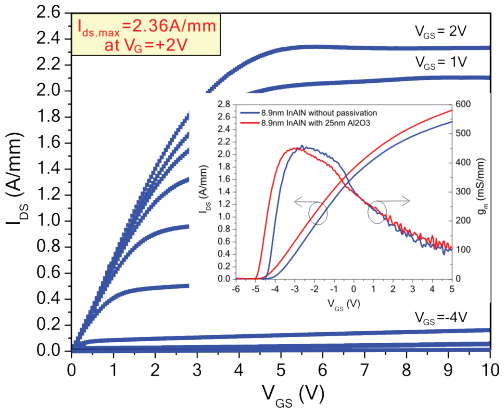


FIGURE 2: Current density (Ids) and transconductance (gm) of an InAlN HEMT with an 8.9-nm InAlN barrier, L_g=100 nm and L_{ds}=2.5 µm.

Generalized Drift-diffusion for Thermoelectrics

P. Santhanam, R. J. Ram
Sponsorship: DoD NDSEG, ONR, DARPA

To aid in the modeling and design of inhomogeneous thermoelectric elements with feature length-scales typical of micro-electronic devices, we have generalized the drift-diffusion (D-D) model to demonstrate the Seebeck effect. Since these new thermoelectric elements use the same semiconducting material-systems in similar ranges of doping and temperature as other electronic devices, the validity of the drift-diffusion framework remains, even as traditional models for thermoelectricity encounter challenges as modern nano-structuring techniques introduce features into thermoelectrics (TEs) on ever-shorter length-scales. Meanwhile, D-D models are substantially less computationally intensive than other valid techniques like direct Monte Carlo simulation of the Boltzmann Transport Equation (BTE) or quantum transport models. Beginning from the BTE and the Relaxation-Time Approximation, we have analytically re-derived a generalization of the traditional D-D equation that includes temperature-driven diffusion via a microscopically-defined Soret coefficient. We then solved this equation (see Figure 1) self-consistently with Poisson's equation to recover the Seebeck effect, thereby independently arriving at the previously-predicted [1] spatial variation of carrier-density within a homogeneously-doped semiconductor experiencing a temperature gradient and induced Seebeck voltage.

We also independently extended this model to include energy-dependent scattering [2], and further confirmed that both of these results align with the traditional theory as seen in Figure 2. Initial comparison of these findings with experimental data has been limited by the availability of data for materials with the simple bandstructure assumed in the simulation and direct measurements of the scattering parameter.

As the theoretical model is further validated, our attention turns to the modeling of inhomogeneous TE elements for thermal-to-electrical power conversion. Here the goal is to model both functionally-graded systems, whose parameters vary continuously from hot-side to cold, and segmented systems, which include interfaces between strongly differing material systems. In both types of inhomogeneous elements, however, the practical goal is to optimize the local material parameters for the expected operating temperature while ensuring compatibility between the operating points of various segments [3], [4].

Current investigations are underway into resolving the Peltier effect, another TE effect closely-related to the Seebeck effect, in the same theoretical and computational model. This work should permit the modeling and design of inhomogeneous elements for TE cooling, as the Seebeck effect does for power generation.

REFERENCES

[1] G. D. Mahan, "Density Variations in Thermoelectrics," *Journal of Applied Physics*, vol. 87, no. 10, pp. 7326-7332, Feb 2000.
[2] J. Cai and G. D. Mahan, "Effective Seebeck Coefficient in Semiconductors," *Physical Review B*, vol. 76, no. 075201, August 2006.
[3] G. J. Snyder, et. al., "Thermoelectric Efficiency and Compatibility," *Physics Review Letters*, vol. 91, iss. 14, no. 8301, October 2003.
[4] G. J. Snyder, "Application of the Compatibility Factor to the Design of Segmented and Cascaded Thermoelectric Generators," *Applied Physics Letters*, vol. 84, iss. 13, pp. 2436-2438, March 2004.

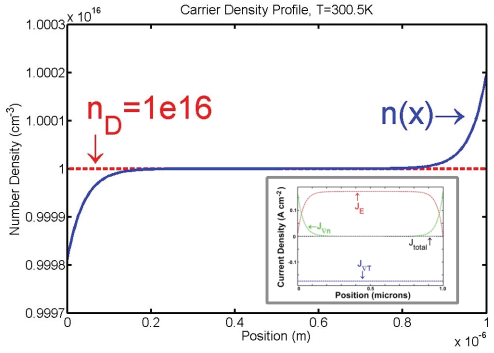


FIGURE 1: Spatial profile of carrier density for a solution in the computational generalized Drift-diffusion model. The associated source-specified current balance appears in the inset. This solution provides a real-space picture of microscopic thermoelectric transport and may form the basis for a new simulation technique useful for designing thermoelectric generators and coolers. The parameters for this simulation are taken from GaAs n-doped 1e16 cm^{-3} at 300K.

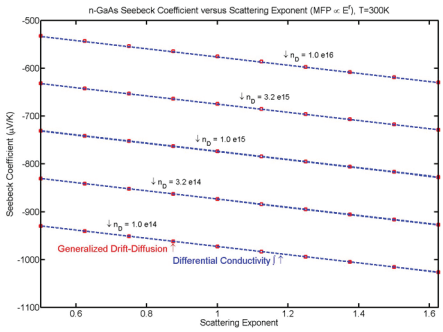


FIGURE 2: Comparison of the generalized Drift-diffusion model with calculations from the more common differential-conductivity model. Agreement is achieved for situations with energy-dependent relaxation time. Such systems hold promise for the improvement of thermoelectric efficiency. Experimental data is not presented for comparison because measurements of the scattering parameter r for these samples were not found.

Magnetic and Magnetoelectronic Memory and Logic

M. Mascaro, C. Nam, C. Garcia, D. Navas, B. Rasin, J. M. Florez, H. Koerner, V. Ng, C. A. Ross
Sponsorship: NRI INDEX program, NSF, Fulbright Fellowship

We are investigating the fabrication and magnetic properties of magnetic logic and memory devices. These consist of multilayer magnetoresistive ring-shaped structures as shown in Figure 1. The magnetic multilayers show giant magnetoresistance, in which the resistance is a function of the relative orientation of the magnetization directions in the magnetic layers. These small structures have potential uses in magnetic-random-access memories (MRAM), magnetic logic devices, and other magneto-electronic applications. Unlike that of conventional MRAM devices, the ring-shaped geometry of these devices allows for a complex response with multiple stable resistance states. This capability can be used for multi-bit memory and for programmable, non-volatile memory.

These devices are programmed using either a magnetic field or a current. Recently, we have been examining how the response of these structures depends on the magnitude of the magnetic field cycling. We found ranges of stable behavior where the response can be extremely uniform, and other field ranges where a variety of stochastic reversal paths occur. We have also shown that spin-polarized currents can reverse the devices in a low-power process. We are now exploring communication between these devices.

Simultaneously, we are exploring high-frequency behavior of magnetic nanostructures through giant magnetoimpedance. In GMI, the impedance of nanoscale structures varies dramatically with magnetic field and with frequency in the GHz range, and this variation can be used for sensitive magnetic field detection.

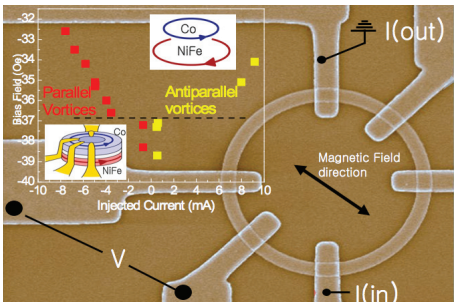
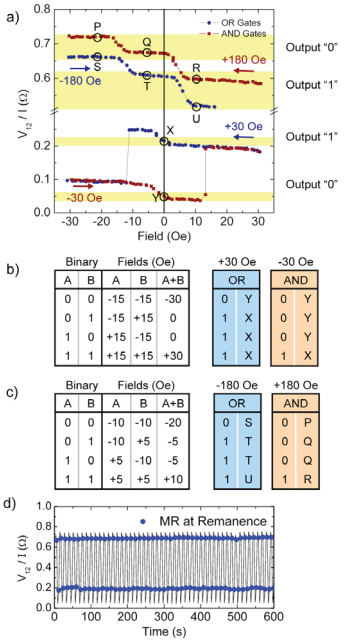


FIGURE 1: A magnetic ring made from Co/Cu/NiFe with diameter of 5 µm and several non-magnetic contacts overlaid. The inset shows the combination of current and magnetic field required to switch the ring from one magnetic state to another.



Binary A	Binary B	Fields (Oe) A	Fields (Oe) B	Fields (Oe) A+B	+30 Oe OR	-30 Oe AND
0	0	-15	-15	-30	0 Y	0 Y
0	1	-15	+15	0	1 X	0 Y
1	0	+15	-15	0	1 X	0 Y
1	1	+15	+15	+30	1 X	1 X

Binary A	Binary B	Fields (Oe) A	Fields (Oe) B	Fields (Oe) A+B	-180 Oe OR	+180 Oe AND
0	0	-10	-10	-20	0 S	0 P
0	1	-10	+5	-5	1 T	0 Q
1	0	+5	-10	-5	1 T	0 Q
1	1	+5	+5	+10	1 U	1 R

FIGURE 2: Electrical response of a magnetic ring tested under different field ranges, showing large resistance changes that can be used for logic operations.

REFERENCES

[1] F.J. Castaño, B.G. Ng, I.A. Colin, D. Morecroft, W. Jung, C.A. Ross, "Magnetoresistance of submicron multilayer Wheatstone bridges as a probe of magnetic reversal mechanism, J. Phys. D 41 132005 (2008).

[2] Chunghee Nam, B. G. Ng, F. J. Castaño, M. D. Mascaro and C. A. Ross, Current-driven vortex formation in a magnetic multilayer ring, Appl. Phys. Letts. 94, 082501 (2009)

Dual-threshold-voltage Organic Thin-film Transistors for Mixed-signal Integrated Circuits

I. Nausieda, K. Ryu, D. He, A. I. Akinwande, V. Bulović, C. G. Sodini
Sponsorship: SRC/FCRP C2S2, Martin Family Fellowship

Organic thin-film transistors (OTFTs) hold the potential for large-area, flexible electronics because their near-room-temperature processing enables them to be fabricated on plastic substrates. We have developed a low temperature (≤95°C) process to fabricate integrated OTFTs [1]. Designing circuits using OTFTs is challenging since only p-channel transistors are typically available. The OTFT technology limits noise margins in digital circuits due to the lack of an NMOS load, the location of the threshold voltage (V_T), and the availability of a single V_T device [2]. We have addressed this problem by creating a dual V_T process, with the addition of only one mask to pattern a second gate metal. We present positive noise margin inverters and a near rail-to-rail ring oscillator using a 3V supply. The ring oscillator output waveform is shown in Figure 1.

The dual V_T process enables analog integrated circuits. We demonstrate an uncompensated, two-stage operational amplifier with open loop gain of 36dB, unity gain frequency of ~7Hz, and common-mode rejection ratio (CMRR) of 20.1dB. The dual V_T op amp has 30x better gain * -3dB frequency product than a single V_T implementation and uses a 5V power supply. The op-amp frequency response is pictured in Figure 2.

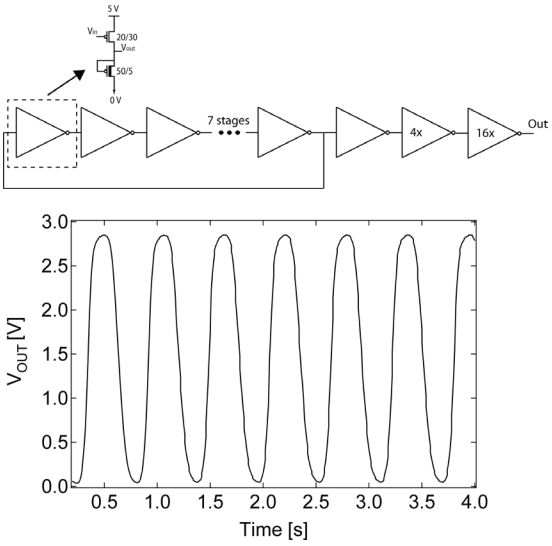


FIGURE 1: Schematic of 11-stage ring oscillator and buffer (top). A 1.7 Hz output transient, indicating an inverter propagation delay of 27 ms.

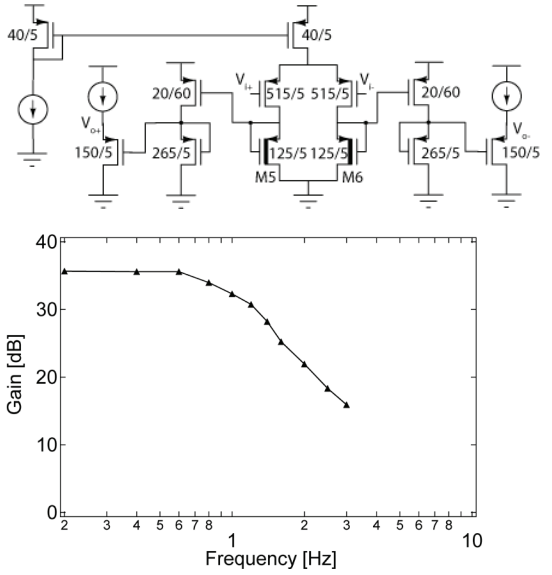


FIGURE 2: Schematic of op-amp (top). Open loop frequency response of dual V_T operational amplifier, indicating 2 poles (bottom).

REFERENCES

[1] I. Nausieda, K. Ryu, I. Kymissis, A.I. Akinwande, V. Bulović, C.G. Sodini, "An organic active-matrix imager," *IEEE Transactions on Electron Devices*, vol.55, pp. 527-532, Feb. 2008.

[2] E. Cantatore, T.C.T. Geuns, G. Gelnick, E. van Veenendaal, A.F.A. Gruijthuijsen, L. Schrijnemakers, S. Drews, D.M de Leeuw, "A 13.56-MHz RFID system based on organic transponders," *IEEE Journal of Solid-State Circuits*, vol.42, pp.84-92. Jan. 2007.

Effects of Bias Stress in Organic Thin-film Transistors

K. Ryu, I. Nausieda, D. He, A. I. Akinwande, V. Bulović, C. G. Sodini
Sponsorship: SRC/FCRP C2S2

Organic transistor technology holds the promise of large-area flexible electronics and integration of various sensors and actuators on a single substrate [1]. However, current-voltage (I-V) characteristics of organic transistors are known to change with the application of prolonged voltages [2]. Such change, termed the bias-stress effect, leads to operational instability, which limits the usable lifetime of the circuit. The bias-stress effect must be understood and minimized to enable the use of organic transistors in functional applications. In this work, we present a method to accurately measure the bias-stress effect and a model that predicts the effect at different stress conditions. The model provides physical insight into the mechanisms causing the bias-stress effect and an estimate of the expected lifetime of the transistor. It also provides a means to determine the operating region that minimizes the bias-stress effect.

To measure the bias-stress effect and no other degradation effects, we characterize pentacene OTFTs that have no measurable change by storage in nitrogen ambient. We demonstrate that the after-stress I-V characteristics can be accurately described by the initial I-V characteristics and a shift in applied gate voltage, ΔV. Based on this observation, we characterize the bias-stress effect with ΔV. We measure ΔV at different gate and drain bias (V_{SG} and V_{SD}) and stress times. Measurements with different V_{SD} at fixed V_{SG} stress show that ΔV decreases with increasing drain bias or current, indicating that gate field and channel carriers, not drain current, are responsible for the stress effect. We report that ΔV saturates independent of the V_{SG} stress. We propose a simple carrier-trapping rate model that results in a stretched-exponential equation that accurately describes the observed ΔV behavior with respect to stress times. The model suggests that the bias-stress effect is caused by trapping of the channel carriers. The bias-stress effect saturates due to a constant number of trap sites, unlike in a-Si:H TFTs, where the trap sites are continually created until there are no more channel carriers [3]. The saturation of the bias-stress effect independent of the V_{SG} stress is reported for the first time in organic transistors.

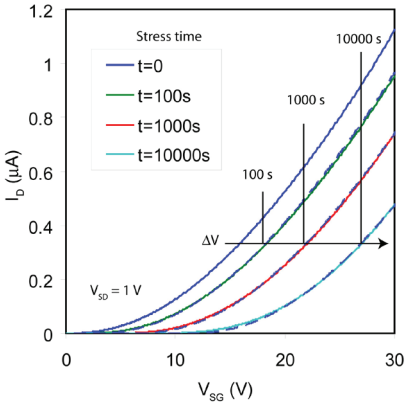


FIGURE 1: Transfer characteristics after bias stress at V_{SG} = 30 V, V_{SD} = 1 V at varying stress time, t. The dashed line shows the shifted transfer characteristics of the unstressed device (t = 0 s).

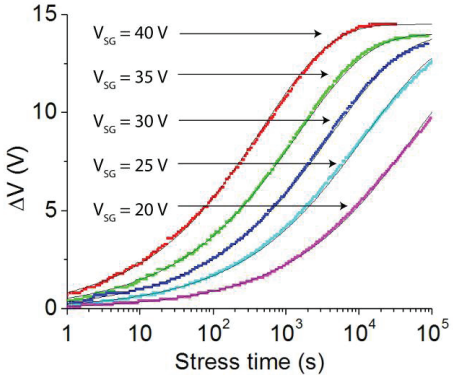


FIGURE 2: Measured stress time-dependence of the induced ΔV for different gate bias-stress conditions (colored dots) and the stretched-exponential fit made to the data (solid lines).

REFERENCES

[1] I. Nausieda, K. Ryu, I. Kymissis, A.I. Akinwande, V. Bulović, C.G. Sodini, "An organic active-matrix imager," *IEEE Transactions on Electron Devices*, vol.55, pp. 527-532, Feb. 2008.

[2] S. J. Zilker, C. Detcheverry, E. Cantatore, and D. M. de Leeuw, "Bias stress in organic thin-film transistors and logic gates," *Appl. Phys. Lett.* 79, 1124, Aug. 2001.

[3] W. B. Jackson, J. M. Marshall, M. D. Moyer, "Role of hydrogen in the formation of metastable defects in hydrogenated amorphous silicon," *Phys. Rev. B*, 39, pp. 1164 – 1179, 1989.

Materials Reliability in GaN-based Devices

P. Makaram, J. A. del Alamo, T. Palacios, C. V. Thompson
Sponsorship: DURINT

GaN-based devices, traditionally used for light-emitting diodes [1], [2], are becoming very attractive for high-power, high-frequency applications for a variety of radar and communication applications [3]. Of particular interest are AlGaN/GaN-heterostructure-based high-electron-mobility transistors (HEMTs). Even though there has been intensive research done to improve these devices [4], their reliability is still a key issue and failure mechanisms are not well understood. The GaN films are typically in a high state of stress due to lattice and thermal mismatch. This state can lead to voiding and/or cracking that, in turn, leads to failure. Moreover, the piezoelectric properties of GaN couple with high electric fields to add to the complexity of the mechanical stress state. The goals of this project are to identify the material failure mechanisms for GaN-based devices, to develop reliability model to predict the lifetimes, and develop testing and lifetime projection methodologies.

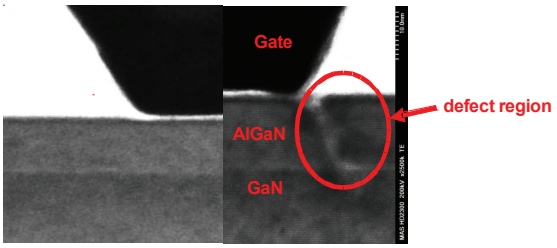


FIGURE 1: (left) A TEM image of a fresh device. (right) A TEM image of a degraded device [5].

REFERENCES:

[1] S. Nakamura and G. Fasol. The Blue Laser Diode. Springer-Verlag, Berlin, pg 343, 1997.
[2] T. Mikai, M. Yamada and S. Nakamura. Japanese Journal of Applied Physics, 38:3976, 1999.
[3] H.Okamura "Present Status and Future Prospect of Widegap Semiconductor High-Power Devices", Japanese Journal of Applied Physics, 45, pp. 7565-7586, 2006
[4] P. Saunier, C. Lee, A. Balistreri, D. Dumka, J. L. Jimenez, H. Q. Tserng, M. Y. Kao, P. C. Chao, K. Chu, A. Souzis, I. Eliashevich, S. Guo, J. del Alamo, J. Joh, and M. Shur, "Progress in GaN performances and reliability," in Proc. IEEE DRC , pp. 35–36. Jun. 2007
[5] J.L. Jimenez, Chowdhury, Balistreri, Lee, Saunier, Chao, Hu, Chu, Immorlica, del Alamo, Joh and Shur, "Failure Analysis of X-Band GaN FETs." , ROCS Workshop, 2006.
[6] J. Joh, L. Xia and J.A. Del Alamo, "Gate current degradation mechanisms of GaN high electron mobility transistors", IEEE International Electron Devices Meeting, IEDM, December 2007.

Effects of Active Atomic Sinks and Reservoirs on the Reliability of Cu/low-k Interconnects

F. L. Wei, C. S. Hau-Riege (AMD), A. P. Marathe (AMD), T. Chookajorn, C. V. Thompson
Sponsorship: Intel Corporation, AMD, SRC

Experiments using Cu/low-*k* interconnect tree structures have been used to characterize the rate and mechanisms of electromigration-induced voiding (Figure 1a) and extrusion (Figure 1b) [1], [2]. Kinetic parameters were extracted from resistance versus time data, giving $(Dz^*)_{0,eff} = 3.9 \times 10^{-10}$ m²/s and $z^* = 0.40 \pm 0.12$. Using these values, the evolution of stress in each of the interconnect tree segments could be calculated and correlated with the rate of void or extrusion growth and the failure times for all test configurations. It was demonstrated that segments that serve as atomic sinks and reservoirs for the failing segments affect the lifetime by modifying the conditions for stress-induced migration. Reservoirs can lead to increased lifetimes, while sinks can lead to reduced lifetimes. Quantitative predictions of the times required for failure for Cu/low-*k* interconnect trees as a function of the effective bulk elastic modulus of the interconnect system, *B*, are made. As the Young's modulus of the inter-level dielectric (ILD) films decreases, *B* decreases; additionally, the positive effects of reservoirs are diminished and the negative effects of sinks are amplified [1]. Analyses of extrusion-failure show that sparsely packed, intermediate-to-wide interconnect lines are most susceptible to electromigration-induced extrusion damage, and that extrusion failures are favored by ILDs with low stiffness, low elastic moduli, and thin liners. The latter are needed in future interconnect systems.

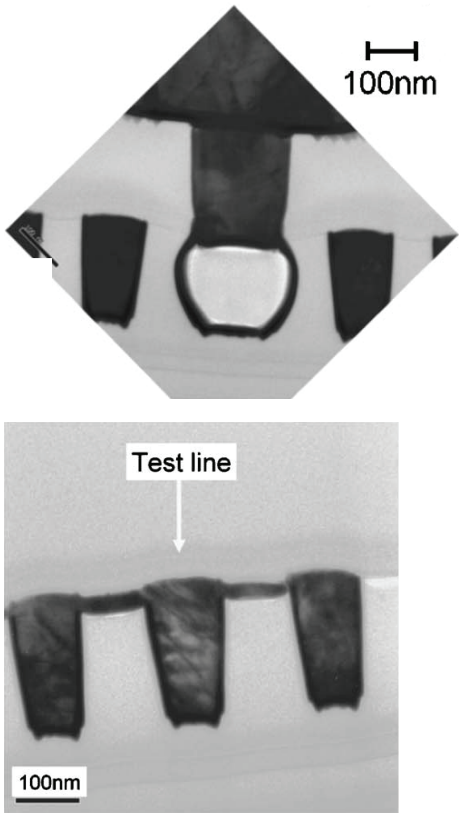


FIGURE 1: (a) Cross-sectional electron microscope image of the cathode end of a Cu/low-k interconnect for which electromigration-induced tensile stress led to void formation and growth and ultimately an open-circuit failure. (b) Cross-sectional electron microscope image of the anode end of a Cu/low-k interconnect for which electromigration-induced compressive stress led to extrusion of Cu at the Cu/capping-layer interface and ultimately short-circuit failure.

REFERENCES

[1] S. Al Kuran, "The prospects for GaAs MESFET technology in dc-ac voltage conversion," in *Proc. Fourth Annual Portable Design Conference*, 1997, pp. 137-142.

Energy

Organic Solar Cells with Graded Exciton-dissociation Interfaces

T. D. Heidel, D. Hochbaum, J. Lee, M. A. Baldo
Sponsorship: DOE

With a theoretical efficiency similar to conventional inorganic photovoltaics (PV) and the potential to be manufactured inexpensively over large areas, organic semiconductor technology offers a promising route to ubiquitous solar energy generation [1]. However, despite significant improvements in efficiency in recent years, additional progress is still needed before organic photovoltaics can compete with other photovoltaic technologies [2]. Organic heterojunction PVs suffer from recombination of separated charges at the exciton-dissociation interface [3]. Ultimately, this recombination limits the efficiency of organic PVs. Device structure modifications represent one of the most promising routes to higher efficiency.

In our work, we reduce the recombination of separated electrons and holes at the exciton-dissociation interface by introducing an additional thin interfacial layer sandwiched between the active semiconductor layers. The interfacial layer in this architecture creates a cascade energy structure at the exciton-dissociation interface as shown in the inset of Figure 1. Previous efforts to add an interfacial layer in organic PVs have suffered due to poor materials selection [4], [5] Reducing recombination losses yields increases in both open circuit voltage (V_{OC}) and short-circuit current (J_{SC}) leading to higher power-conversion efficiencies, as illustrated in Figure 1. We are studying how the energy level alignment of the interfacial layer impacts recombination and developing criteria for optimal interface material design and selection.

As illustrated in Figure 2, we find that devices with too thin an interfacial layer demonstrate limited improvements in charge collection due to partial layer coverage. Conversely, devices with interfacial layers that are too thick suffer from carrier-transport problems in the interfacial layers. Determining the optimal interfacial layer thickness promises to give greater insight into the physical mechanism of charge-carrier recombination at the exciton dissociation interface in organic PVs.

REFERENCES

[1] Forrest, S.R., *The limits to organic photovoltaic cell efficiency.* MRS Bulletin, 2005. **30**(1): p. 28-32.

[2] Martin A. Green, K.E.Y.H.W.W., *Short Communication Solar cell efficiency tables (version 33).* Progress in Photovoltaics: Research and Applications, 2009. **17**(1): p. 85-94.

[3] Peumans, P., A. Yakimov, and S.R. Forrest, *Small molecular weight organic thin-film photodetectors and solar cells.* Journal of Applied Physics, 2003. **93**(7): p. 3693-3723.

[4] Sista, S., et al., Enhancement in open circuit voltage through a cascade-type energy band structure. Applied Physics Letters, 2007. **91**(22): p. 3.

[5] Kinoshita, Y., T. Hasobe, and H. Murata, Control of open-circuit voltage in organic photovoltaic cells by inserting an ultrathin metal-phthalocyanine layer. Applied Physics Letters, 2007. **91**(8): p. 3.

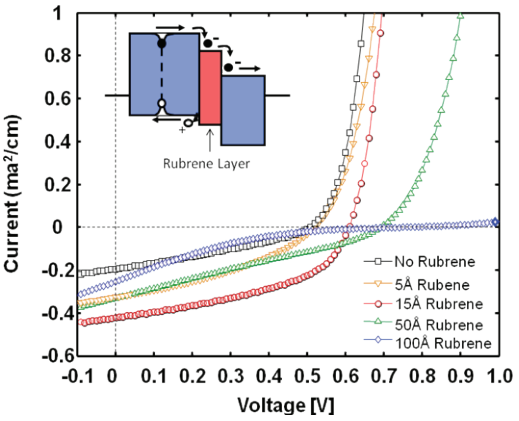


FIGURE 1: Current–Voltage characteristics for devices with and without a Rubrene interfacial layer. Devices with a thin layer of Rubrene at the exciton-dissociation interface exhibit increased short-circuit current and increased open-circuit voltage. However, at large interfacial layer thicknesses, the current decreases.

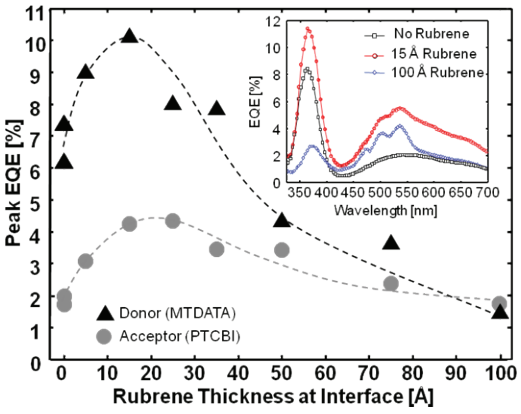


FIGURE 2: Devices with thin interfacial layers exhibit higher external quantum efficiencies. The optimal layer thickness is approximately 15Å. The interfacial layer reduces recombination of separated charges at the exciton-dissociation interface.

Luminescent Solar Concentrators for Energy-harvesting in Displays

C. L. Mulder, H. Kim, M. A. Baldo
Sponsorship: DOE

We present linearly polarized luminescent solar concentrators (LSCs) optimized for energy-harvesting in displays. Current methods to increase the contrast ratio of displays mostly use combinations of linear polarizers to absorb and dissipate incident light. Incidentally, the polarizers also absorb 50% of the light emitted by the display. The inherently absorptive surface of the display, together with the ever-increasing area of televisions and displays in mobile electronics, makes them interesting candidates for energy-harvesting [1]. In this project, we propose to replace the purely absorptive polarizers in displays with two linearly polarized luminescent concentrators (LSCS) [2] (Figure 1a). Conventional polarizers employ aligned molecules that absorb strongly along the long axis of the molecules or polymer strands (see for instance Figure 1b for aligned Coumarin 6 dye molecules). Our device will introduce into the polarizer light-emitting molecules that re-emit the captured photons into the waveguide. These photons travel to the edges of the waveguide by total internal reflection, whereby they are collected by solar cells. This geometry will allow for the solar cells to be placed only in the frame of the display, leaving the entire front surface available for the display.

Figure 2 shows preliminary results for a linearly polarized LSC based on a rod-shaped dye molecule, Coumarin 6, that is aligned in the plane of the substrate using a nematic–liquid-crystal matrix. As can be observed, the optical quantum-efficiency of these films, defined as the fraction of the photons incident on the face of the waveguide versus the number of photons emitted from the edges, is 30%, limited presently by relatively weak absorption. Another 20% of the photons are emitted from the face of the sample, which might hamper the contrast ratio of a display. We propose to use infrared dyes to circumvent this effect.

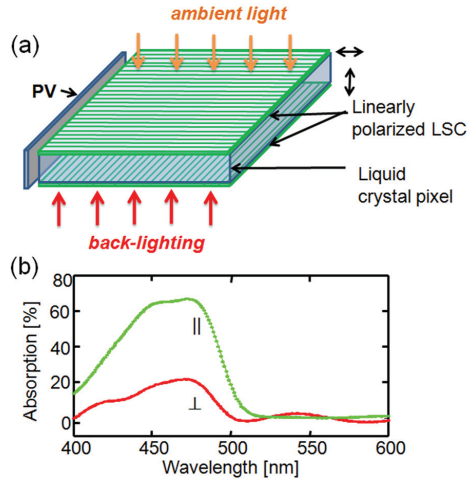


FIGURE 1: (a) A schematic representation of linearly polarized luminescent solar concentrators (LSC) for energy-harvesting in displays. (b) Preliminary results for the absorption of aligned rod-shaped Coumarin 6 dye molecules showing a strong anisotropy between the absorption along the long axis (green) of the molecule and the short axis (red).

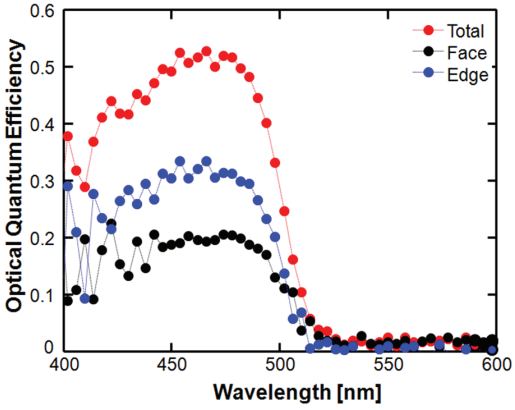


FIGURE 2: The optical quantum efficiency, defined as the fraction of the photons incident on the face of the luminescent concentrator that is emitted from the edge for a linearly aligned system. Only 70% of the incident photons were absorbed for this device.

REFERENCES

[1] C.-J. Yang. T.-Y. Cho, C.-L. Lin and C.-C. Wu, "Energy-recycling high-contrast organic light-emitting devices", *Journal of the Society for Information Display*, vol. 16, pp. 691-694 , June 2008.

[2] J.S. Batchelder, A.H. Zewail, and T. Cole , "Luminescent solar concentrators. 2: Experimental and theoretical analysis of their possible efficiencies", *Applied Optics*, vol. 20, pp. 3733-3754, Nov. 1981.

High-pressure Chemistry: Converting Gases to Liquids for Energy Applications

J. Keybl, K. F. Jensen
Sponsorship: BP

We have designed a microreactor platform to study homogeneous chemical reactions at high temperatures (<400°C) and pressures (<100 bar). Microreactor technology has allowed the study of chemical reactions to move from a laboratory-scale batch process to a micro-scale continuous process. This shift leverages the numerous benefits of the micro scale, such as enhanced heat and mass transfer and reduced reactant volumes. Advancements in packaging, coupled with the high mechanical strength of silicon, have allowed these reactions to be carried out at increasingly higher pressures and temperatures. Our microreactor design is based on fabrication principles originally developed for MEMS, specifically lithography, deep reactive ion etching, silicon nitride deposition, and anodic bonding. The microreactor consists of a one-meter-long serpentine 400-μm-wide channel. A halo-etched hole is present to aid thermal isolation between the heated reactor section and the cooled mixing section (see Figure 1). High-pressure fluidic connections are made between the finished microreactor and a stainless steel compression chuck and using silicone o-rings.

Homogeneous catalyst solutions will be delivered to the microreactor in a liquid solution using a high-pressure syringe pump. Gases such as carbon dioxide or carbon monoxide and hydrogen will be delivered by a second high-pressure syringe pump. They meet at a T-junction within the reactor, forming a two-phase segmented flow regime. Segmented flow is advantageous because it reduces diffusion between adjacent liquid slugs and increases mass transfer between the gas and liquid phases. The completed system has been flow-tested and is able to control temperature to ±0.1°C and pressure to ±0.01 bar at flow rates as small as 5μl/min. Extended flow studies were conducted and stable steady-state flows were observed at a variety of conditions within the design envelope (Figure 2). Validation studies using a known gas-to-liquid chemistry are ongoing [1].

FIGURE 1: Silicon micoreactor with 400-µm-wide channels. The top half of the reactor is cooled and thermally isolated from the heated bottom half.

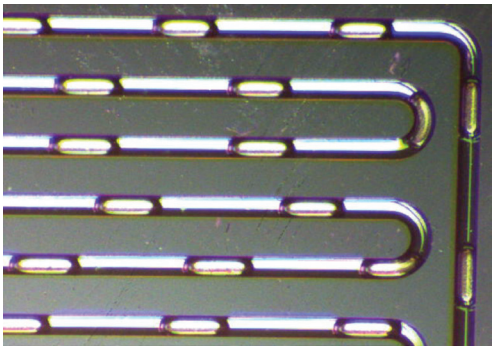


FIGURE 2: Steady segmented flow in the completed system at 40 bar and 105°C. The shorter slugs contain nitrogen gas and the longer slugs contain water.

REFERENCES

[1] F. Gassner, and W. Leitner, "CO2-Activation .3. Hydrogenation of Carbon-Dioxide to Formic-Acid Using Water-Soluble Rhodium Catalysts," *Journal of the Chemical Society-Chemical Communications*, no. 19, pp. 1465-1466, Oct. 1993.

Nano-engineered Organic Solar-energy-harvesting System

H. W. Lee, S. Bathurst, S.-G. Kim
Sponsorship: KFUPM-MIT Research Program

We envision a new organic photovoltaic cell design: a photo-active layer is positioned in between vertically aligned carbon nanotubes. In an organic solar cell, there are several conversion steps from solar energy to electrical energy, including light absorption, electron-hole pair creation and separation, exciton diffusion, and so on. The power conversion efficiency of an organic photovoltaic cell is much lower than that of silicon-based solar cells [1] since most excitons do not reach at the exciton dissociation site and therefore photon-generated charges are not collected to electrodes efficiently [2].

This research focuses on locating the electron acceptor within an exciton diffusion length from the electron donor by having them distributed at nanometer scale and have a vertically grown CNT array reach them with a 3-dimensional network configuration. To implement the design of well-dispersed electron donor and acceptor materials, we use vertically grown carbon nanotube arrays having 100~150-nm spacing (Figure 1) [3]. Figure 2 shows the conceptual design of our proposed PV device. After growing vertically aligned carbon nanotubes, the SiO_2 dam is structured surrounding the CNT array. Then, the CNT array will be filled with an active polymer layer (a mixture of P_3HT and PCBM) using the thermal inkjet printing method. We expect that our proposed CNT-based organic cell will increase the power-conversion efficiency drastically by collecting the photo-generated charges before they recombine.

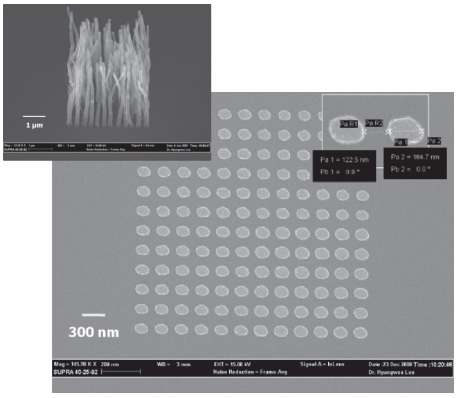


FIGURE 1: An array of catalyst nano dots having 100~150 nm spacing and vertically aligned carbon nanotubes grown by plasma enhanced chemical vapor deposition (PECVD).

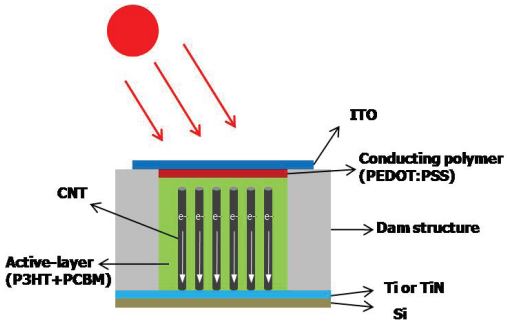


FIGURE 2: The conceptual design of the proposed photovoltaic cell having vertically aligned carbon nanotubes.

REFERENCES

[1] J. Y. Kim, K. Lee, N. E. Coates, D. Moses, T.-Q. Nguyen, M. Dante, A. J. Heeger, "Efficient tandem polymer solar cells fabricated by all-solution processing," *Science*, vol. 317, no. 13, pp. 222-225, 2007.

[2] J. J. M. Halls, K. Pichler, R. H. Friend, S. C. Moratti, A. B. Holmes, "Exciton diffusion and dissociation in a PPV/C60 heterojunction photovoltaic cell," *Appl. Phys. Lett.*, vol. 68, pp. 3120-3122, 1996.

[3] S. Kim, H. W. Lee, S-G Kim, "Transplanting Assembly of CNT-tipped AFM Probes," *Appl. Phys. Lett.*, accepted

Design of Coreless Magnetics for VHF Power Conversion

A. D. Sagneri, D. J. Perreault
Sponsorship: National Semiconductor Corporation, CICS

The desire for power converters with reduced size, weight, and cost has led to an effort to reduce energy storage requirements by switching in the VHF regime (30-300 MHz). At these frequencies, batch-fabricated converters with co-packaged passive components seem nearly within reach. It has already been demonstrated through layout optimization techniques that LDMOSFETs in a standard power process can operate effectively in VHF power converters [1-3]. This work looks at coreless magnetic components with form factors suitable to co-package with a monolithic IC implementing the switching and control functions of a VHF power converter.

Figure 1 shows an isolated VHF converter topology that requires a transformer and several inductors. The inductors LF and LREC can be absorbed into the transformer structure to reduce the component count, which eases the mechanics of co-packaging. Absorbing the inductors fixes the inductance matrix description of the transformer. A large number of transformer geometries can realize a given inductance matrix. The goal is to find one that has the best efficiency vs. volume characteristics.

While it is relatively easy to analyze a structure for its inductance matrix, inverting the problem is difficult. Here we first constrain the design space to a planar transformer. It is then possible to use models for the mutual inductance between concentric rings [4] to find a locus of geometries that have approximately the desired inductance characteristics. Each structure is then analyzed using FastHenry [5], to extract the self- and mutual-resistance terms. The full set of transformer parameters is then used to calculate power loss for the desired converter application, yielding a loss-diameter curve from which the desired structure can be picked.

Using this technique, structures are realized (Figure 2) from 4.5 – 10 mm in diameter and 0.8 mm thick. They yield efficiencies from 85% - 93% while transmitting 9.5 W.

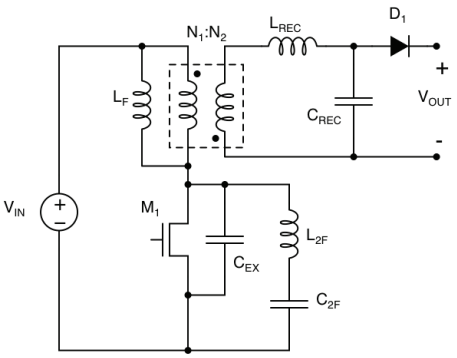


FIGURE 1: The isolated F2 DC-DC converter topology is suitable for use at VHF. The ideal transformer is implemented by a real structure that absorbs L_F as the magnetizing inductance and L_{REC} as leakage inductance to reduce the component count.

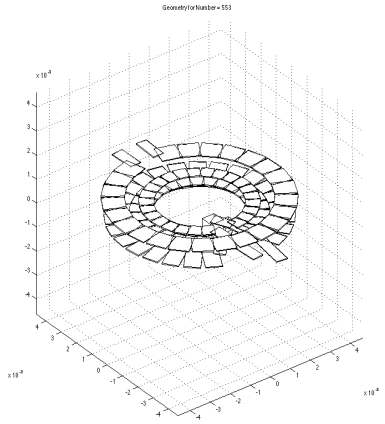


FIGURE 2: A segmented representation of a planar transformer. The transformers are fabricated on a 4-layer 0.031" PCB. Each turn is on a separate layer, so the total number of turns (primary and secondary) is 4.

REFERENCES

[1] J.M. Rivas, R.S. Wahby, J.S. Shafran, and D.J. Perreault, "New architectures for radio-frequency DC-DC power conversion," in Proc. 35th Annual IEEE Power Electronics Specialist Conference, Aachen, Germany, June 2004, pp. 4074-4084.

[2] A.D. Sagneri, "The design of a VHF DC-DC boost converter," Master's thesis, Massachusetts Institute of Technology, Cambridge, 2007

[3] J.M. Rivas, Y. Han, O. Lietermann, A. Sagneri and D.J. Perreault, "A high-frequency resonant inverter topology with low voltage stress," Power Electronics Specialist Conference Proceedings, June 2007

[4] W.G. Hurley and M. C. Duffy, "Calculation of self and mutual impedances in planar magnetic structures," IEEE Transactions on Magnetics, 1995, Vol. 31. No. 4, 2416-2422

[5] L.M. Silveira, M. Kamon, and J.K. White, "Efficient reduced-order modeling of frequency-dependent coupling inductances associated with 3-D interconnect structures," IEEE Transactions on Components, Packaging, and Manufacturing Technology, May 1996, Part B, Vol. 19, No. 2

Solar Thermoelectrics

R. Amatya, R. J. Ram
Sponsorship: MITEI

Solar thermoelectric generators (STG) (Figure 1) employing light concentrators and high-ZT thermoelectric materials are an attractive alternative to solar photovoltaics for micro-power applications. Earlier work on STG [1-3] has shown low system efficiency (<1%) primarily due to small-module ZT and low solar concentration. To date, the highest measured efficiency for solar thermoelectrics is 3.35%, using a unicouple of ZT = 0.4 and solar concentration of 50 suns (1 sun = 1000W/m^2) [1]. A low-cost parabolic concentrator can give up to 10 suns of solar radiation. A cost model was developed using a simulation tool called HOMER. Our economic model for a micro-power STG (η_{sys}~ 4.5%) shows a 30% cost reduction compared to commercial photovoltaics.

A complete thermodynamic analysis based on energy balance and heat transfer allows us to predict system efficiency at any given solar radiation for the STG. The total efficiency depends on both the solar concentrator and the thermoelectric module performance. The concentrator efficiency decreases due to convective and radiative losses from the hot side. Convective losses can be reduced by introducing suppression mechanisms such as multiple glass panels and dead air in between the glass and the absorber. For radiative loss suppression, a special coating called "selective surface" can be utilized; it has larger absorption coefficient at the visible wavelength range and low emissivity at higher wavelengths, where the black body radiation occurs. STG performance is modeled using mature thermoelectric materials such as micro-alloy Bi_2Te_3 and SiGe, as well as novel materials with high material ZT such as ErAs: InGaAlAs and $(AgSbTe)_x(PbSnTe)_{1-x}$ - LAST. At low temperature (< 500K), with Bi_2Te_3 (ZT_{module} = 0.77), η_{sys} of 3.76% can be achieved using air convection at the cold side. At larger temperature range, using selective surface coating and water convection, η_{sys} of 5.5% can be achieved (Figure 2).

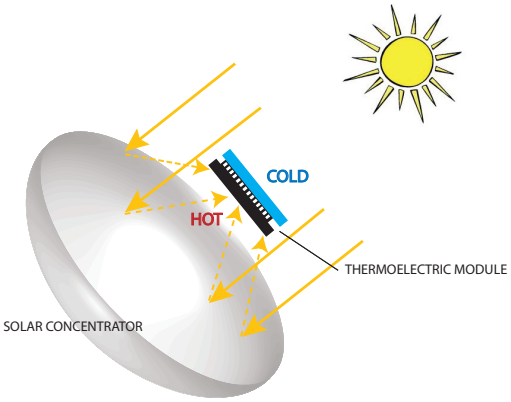


FIGURE 1: Solar thermoelectric generator (STG).

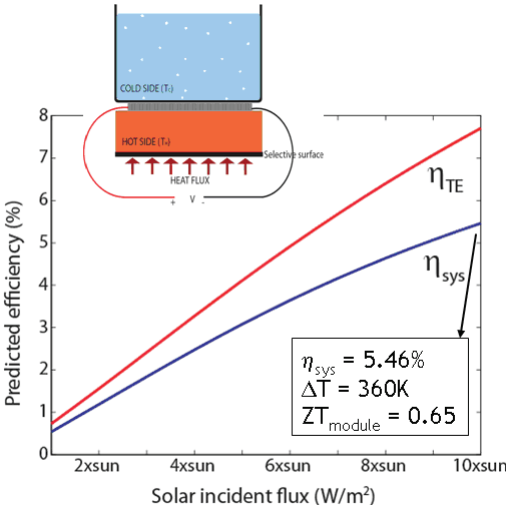


FIGURE 2: Theoretical prediction for module (h_{TE}) and system (h_{sys}) efficiency for a STG using n-type ErAs: InGaAlAs and p-type LAST material.

REFERENCES

[1] M. Telkes, "Solar Thermoelectric Generators," *Journal of Applied Physics*, vol. 25, no. 6, pp. 765-777, June 1954

[2] N. Vatcharasanthien, J. Hirunlabh, J. Khedari, M. Daguenet, "Design and analysis of solar thermoelectric power generation system," *International Journal of Sustainable Energy*, vol. 24, no. 3, pp. 115-127, Sept.2005

[3] S. A. Omer and D. G. Infield, "Design optimization of thermoelectric devices for solar power generation," *Solar Energy Materials and Solar Cells*, vol. 53, pp. 67-82, Jan. 1998.

Microfabricated Thin-film Electrodes for Solid Oxide Fuel Cells

W. C. Jung, K. Haga, D. Chen, H. L. Tuller
Sponsorship: NSF, DMR-0243993; Saint Gobain

Micro- solid oxide fuel cells (SOFCs) are currently under intense investigation for portable power applications, such as notebook computers and mobile phones [1]. In this work, thin film $SrTi_{1-x}Fe_xO_3$ (STF) cathodes were fabricated on top of single-crystal yttria-doped zirconia (YSZ) solid electrolyte substrate by both pulsed laser deposition (PLD) and thermal inkjet printing (TIJ) (see Figure 1), and their properties were systematically investigated in relation to the cathodic performance of the STF. Various additives were added to the inks to control viscosity and reduce clogging. Deposition conditions were carefully selected to obtain uniform and crack-free films (see Figure 2).

Analysis of the impedance spectra, collected on symmetrical cells of the type STF/YSZ/STF over the temperature range of 570 – 650°C and the pO_2 range of $2x10^{-5}$ – 1 atm, was consistent with the mixed ionic-electronic behavior of the STF characterized by fast surface-oxygen exchange kinetics. Present studies focus on correlating the bulk transport properties of STF with changes in the corresponding changes in oxygen exchange kinetics. Ink jet deposited films were found to exhibit similar performance to PLD-deposited films as long as care was taken that no reaction products between STF and YSZ were formed during sintering.

REFERENCES

[1] C.D. Baertsch, K.F. Jensen, J.L. Hertz, H.L. Tuller, S.T. Vengallatore, S.M. Spearing, M.A. Schmidt, *Journal of Materials Research* **19** (9), 2604 (2004)

[2] J. L. Hertz and H. L. Tuller, *Micro-fuel Cells* in A. Mitsos and P.I. Barton (eds.), Microfabricated Power Generation Devices: Design and Technology, Wiley-VCH, Weinheim, Germany, 2009, pp.51-80.

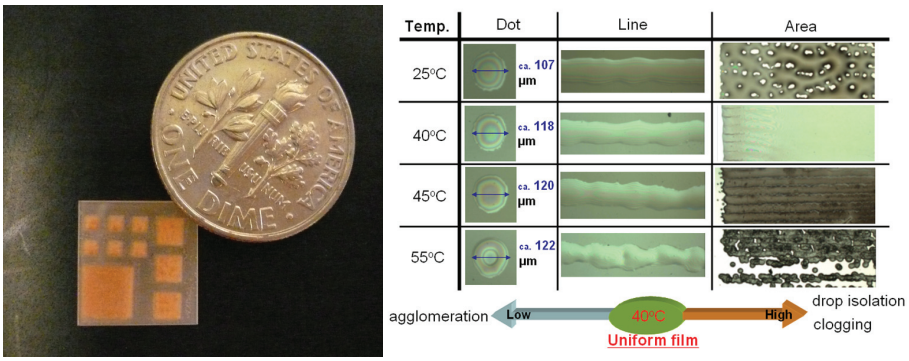


FIGURE 1: A photograph of STF (left) films prepared by thermal inkjet printing and subsequent sintering and (right) the effect of substrate temperature on morphology of ink-jetted STF films.

Thin-film Epitaxial Catalysts for Low-temperature Solid Oxide Fuel Cells

G. J. la O', S. J. Ahn, E. C. Crumlin, Y. Shao-Horn
Sponsorship: NSF

A key issue for the commercialization of solid oxide fuel cells (SOFCs) has been the catalytic limitations of the perovskite (ABO_3) cathode (i.e., such as $LaMnO_3$ or $LaCoO_3$) where oxygen reduction reactions (ORRs) occur. The conventional strategy to improve cathode ORR activity has been to synthesize ABO_3 materials with higher oxygen vacancy concentration. This goal has been traditionally accomplished by doping the perovskite A and B sites with aliovalent alkaline-earth (i.e., Sr, Ba, Ca) and transition metal (i.e., Ni, Fe) elements, respectively. Recently, strain-engineered electrode [1] and electrolyte [2] materials for SOFCs have demonstrated remarkable effects on catalytic activity and oxygen ion transport. These effects had been attributed to compressive or expansive strains in the crystal as a result of lattice-mismatched epitaxial growth. Here we report strain-induced catalytic enhancement for ORR on epitaxial (001) $La_{0.8}Sr_{0.2}CoO_3$ (LSC) grown on Y_2O_3-stabilized ZrO_2 with Gd_2O_3-doped CeO_2 buffer layer. In-plane expansive strains of 1.4 % and 0.29 % were observed for 45-nm and 130-nm epitaxial LSC films, respectively, as shown in Figure 1a. These expansive strains resulted in higher oxygen nonstoichiometry for epitaxial LSC films in comparison to bulk LSC, as shown in Figure 1b. Consequently, ~10x higher chemical surface oxygen exchange kinetics (k_{chem}) than bulk LSC [3] were observed for these epitaxial LSC films, as shown in Figure 1c. This study demonstrates a new approach to significantly enhance the catalytic activity of conventional perovskite materials by strain-engineering.

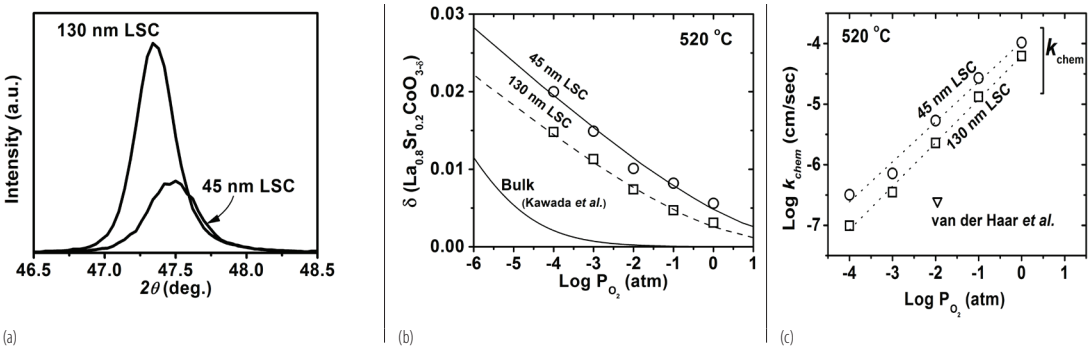


FIGURE 1: (a) Out-of-plane XRD results from LSC (002) reflection with 130-nm LSC peak shifted to a 2q lower angle indicating relaxation of the strain in the LSC film. (b) Enhanced oxygen nonstoichiometry (d) for 45-nm and 130-nm LSC films in comparison to bulk LSC [3]. (c) Enhanced k_{chem} for epitaxial films with thickness of 45 nm and 130 nm, in comparison to bulk values previously reported [4].

REFERENCES

[1] A. Yamada, Y. Suzuki, K. Saka, M. Uehara, D. Mori, R. Kanno, T. Kiguchi, F. Mauvy and J.C. Grenier, "Ruddlesden-Popper-Type Epitaxial Film as Oxygen Electrode for Solid-Oxide Fuel Cells," *Advanced Materials*, vol. 20, p. 4124, Nov. 2008.

[2] J. Garcia-Barriocanal, A. Rivera-Calzada, M. Varela, Z. Sefrioui, E. Iborra, C. Leon, S.J. Pennycook and J. Santamaria, "Colossal ionic conductivity at interfaces of epitaxial ZrO2 : Y2O3/SrTiO3 heterostructures," *Science*, vol. 321, p. 676, Aug. 2008.

[3] T. Kawada, J. Suzuki, M. Sase, A. Kaimai, K. Yashiro, Y. Nigara, J. Mizusaki, K. Kawamura and H. Yugami, "Determination of Oxygen Vacancy Concentration in a Thin Film of La0.6Sr0.4CoO3 - delta by an Electrochemical Method," *J Electrochem Soc*, vol. 149, p. E252, July 2002.

[4] L.M. van der Haar, M.W. den Otter, M. Morskate, H.J.M. Bouwmeester and H. Verweij, "Chemical Diffusion and Oxygen Surface Transfer of La1 - xSrxCoO 3 - delta Studied with Electrical Conductivity Relaxation," *J Electrochem Soc*, vol. 149, p. J41, 2002.

Microfabricated Thin-film Electrolytes and Electrodes for Solid Oxide Fuel Cells

S. J. Litzelman, W. C. Jung, H. L. Tuller
Sponsorship: NSF

Micro-solid oxide fuel cells (SOFCs) are currently under intense investigation for portable power applications, such as notebook computers and mobile phones [1]. While thin film nanostructured solid electrolytes result in lower cell losses due to reduced ohmic resistance, grain boundaries may serve as fast diffusion pathways for cations, resulting in reduced long-term stability. The effects of grain boundary chemistry and interdiffusion on ionic transport have yet to be systematically investigated.

To explore the relationship between performance and stability, CeO_2 thin films were grown by pulsed laser deposition (PLD) [1] and Ni and Gd were subsequently in-diffused along the grain boundaries in the temperature range of 700-800°C. Novel electron-blocking microelectrodes, prepared via a photolithographic lift-off process, enabled determination of the partial electronic and ionic contributions to the total conductivity. Changes in space charge carrier profiles were modeled to account for changes in carrier transport parallel and perpendicular to the columnar grain boundaries in the CeO_2 film.

REFERENCES

[1] C.D. Baertsch, K.F. Jensen, J.L. Hertz, H.L. Tuller, S.T. Vengallatore, S.M. Spearing, M.A. Schmidt, *Journal of Materials Research* 19 (9), 2604 (2004)

[2] J. L. Hertz and H. L. Tuller, *Micro-fuel Cells* in A. Mitsos and P.I. Barton (eds.), Microfabricated Power Generation Devices: Design and Technology, Wiley-VCH, Weinheim, Germany, 2009, pp.51-80.

[3] S.J. Litzelman, R.A. De Souza, B. Butz, H.L. Tuller, M. Martin, D. Gerthsen, *Journal of Electroceramics*, DOI: 10.1007/s10832-008-9445-y (2008)

Advanced Photoelectrodes for Photo-assisted Water Electrolysis

J. Engel, H. L. Tuller in collaboration with D. Nocera
Sponsorship: Chesonis Family Foundation

With continuously growing energy demands, new alternative energy solutions become essential. In order to achieve sustainability, efficient conversion and storage of solar energy are imperative [1], [2]. Photoelectrolysis utilizes solar energy to evolve hydrogen and oxygen from water, thereby enabling energy storage via chemical means. This work investigates photoelectrodes, which offer high conversion efficiency, long-term stability, and low cost. The focus is initially on semiconducting metal oxides in which the energy band, defect, and micro-structure are tuned to optimize optical absorption, charge transport and reduced overpotentials.

REFERENCES

[1] N.S. Lewis, D.G. Nocera, Proceedings of the National Academy of Sciences 103, 43 (2006)
[2] R. van de Krol, Y. Liang, J. Schoonman, Journal of Materials Chemistry 18, 2311 (2008)

Materials

Molecules as Segmented Storage Elements in Floating Gate Memories

S. Paydavosi, V. Bulović

Sponsorship: SRC/FCRP MSD

Conventional flash memories may reach fundamental scaling limits [1] because of the minimum tunnel oxide thickness and poor charge retention due to defects in the tunneling oxide, necessitating new approaches to meet the scaling requirements while simultaneously meeting the reliability and performance requirements of future products. In this study we demonstrate alternative nano-segmented floating gate memories using organic molecules as programmable charge-storage and charge-retention elements in capacitive structures. These organic thin films consist of inherently well-ordered planner molecules that are on the order of 1nm in size, representing a uniform set of identical nanostructured charge-storage centers. We investigated and compared the memory behavior of a variety of molecular thin films for identifying the molecular thin-film characteristics best suited for design of floating gate memory. The initial results show device durability over 10^5 program-erase cycles, with a hysteresis window of up to 3.3 V for program/erase conditions of +8V/-8V, corresponding to the charge storage density of 5 x 10^{12} cm^{-2}. These results signify the potential of using molecular organic thin films as a floating gate of flash memory devices.

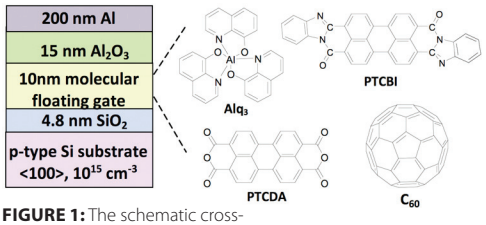


FIGURE 1: The schematic cross-section of the device structure with chemical structures of tested molecular organic thin films.

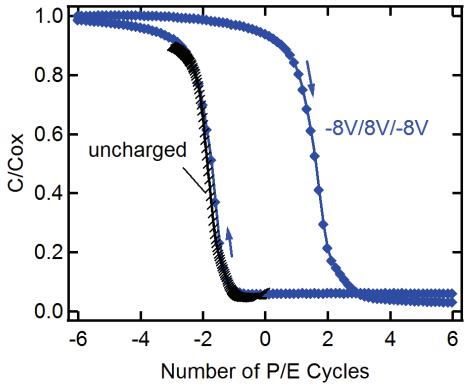


FIGURE 2: The C-*V* plot of a device with a10-nm thick PTCBI layer showing a 3.3±0.1 V hysteresis window.

REFERENCES

[1] Pavan, P., Bez, R., Olivo, P. & Zanoni, E. Flash Memory Cells-An Overview. *Proceedings of the IEEE* **85**, 8 (1997).

In-situ Deposition of High-k Dielectrics on a III-V Compound Semiconductor

C. W. Cheng, Y. Li, J. Hennessy, D. A. Antoniadis, E. A. Fitzgerald
Sponsorship: SRC/FCRP MSD

We developed an *in-situ* manufacturable method to passivate the III-V compound semiconductor (especially the GaAs) in an MOCVD system. The trimethyaluminum (TMA) and isopropanol (IPA) were chosen as the precursors of the Atomic Layer Deposition (ALD) of Al_2O_3. The III-V channel and buffer layer were grown by the CVD mode and then the passivation Al_2O_3 was deposited by the ALD mode by applying appropriate procedures and growth parameters in an MOCVD system. This design made our CVD machine the first *in-situ* passivation CVD machine in the world, and it achieved low interfacial defect density at the oxide/III-V semiconductor. Beside the *in-situ* method, the *ex-situ* method was also investigated to compare the results with the *in-situ* method. The self-cleaning effect was also explored in the *ex-situ* process by applying TMA/IPA as ALD precursors. Both depletion- and enhanced-mode MOSFET were fabricated to evaluate the real performance of the device with *in-situ* passivation oxide.

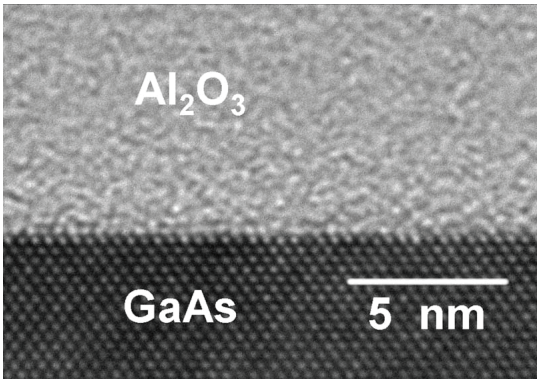


FIGURE 1: An HRTEM image of the interface between GaAs substrate and Al_2O_3 film grown at 370 °C. The TMA and IPA pulse times were both 5 s.

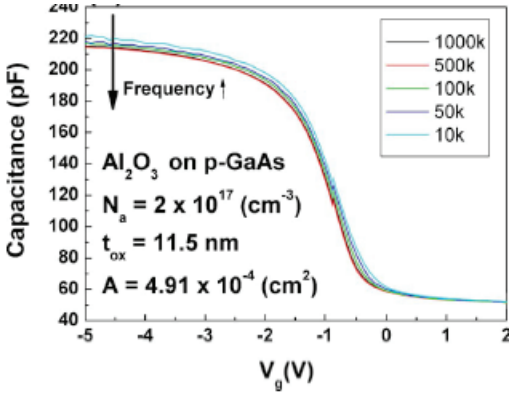


FIGURE 2: The C-V characteristics of in-situ Al_2O_3 / p-GaAs MOS capacitor measured at different frequencies from 10 kHz to 1 MHz.

REFERENCES

[1] C.W. Cheng and E.A. Fitzgerald,"*In situ* metal-organic chemical vapor deposition atomic-layer deposition of aluminum oxide on GaAs using trimethyaluminum and isopropanol precursors," *Applied Physics Letters*, vol. 93, no.3 , pp. 031902:1-3, July 2008.

[2] C.W. Cheng,J. Hennessy, D. Antoniadis, E.A. Fitzgerald ,"The Discrepancy of C-V Characteristics of *In* and *Ex Situ* Atomic-layer-deposition Al_2O_3 on n- and p- GaAs with Arsine Treatment," submitted to *IEEE Electron Device Letters.*

A CMOS-compatible Substrate and Contact Technology for Monolithic Integration of III-V Devices with Silicon

N. Yang, M. Bulsara, E. A. Fitzgerald

Sponsorship: DARPA COSMOS program

This work explores a method of planar integration of III-V HEMTs with silicon CMOS technology, which will allow for true monolithic integration of III-V RF components with digital logic. The substrate platform and contact technology of the III-V devices are studied. Our group previously developed the substrate platform on which these devices will be built, which is shown in Figure 1 [1], [2]. It has been termed a silicon-on-lattice-engineered-silicon (SOLES) substrate. The buried germanium in this substrate provides a template for the growth of III-V materials, whereas the top silicon-on-insulator allows for the processing of traditional CMOS devices. This substrate platform offers flexible integration of III-V and Si devices [3], [4] as well as the capability to be processed in a Si fabrication facility. We are currently exploring the thermal stability of the SOLES substrate, both in terms of the mechanical stability and the diffusion or interdiffusion of the various layers. Methods to increase the thermal budget of this substrate are sought. These methods include the incorporation of additional buried layers in the substrate. Both the ease of integration of these new materials as well as the ease of subsequent device processing on the SOLES substrate are considered in the materials choices.

For true monolithic integration, both the substrate platform and device processing must be compatible with Si CMOS. Thus, we seek a device process that will eliminate or minimize exposure of the III-V materials. In addition, using only materials that are traditional to the silicon fabrication will be advantageous in allowing for simultaneous processing of both the Si and III-V devices. The III-V contact technology traditionally makes use of gold, a deep-level trap in silicon. Because the use of gold is detrimental to silicon devices and because of the simultaneous goal of process integration, we seek to create silicide contacts to GaAs through a silicon cap. Nickel silicide is currently being explored for this application due to its low thermal budget, as compared to TiSi2 and CoSi2.

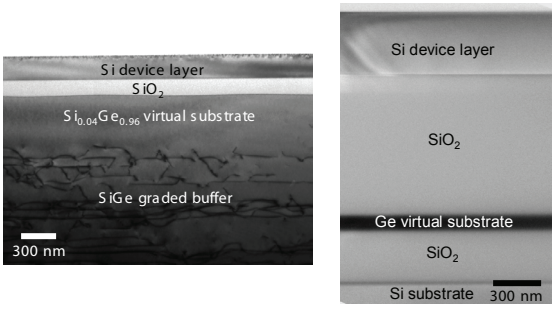


FIGURE 1: TEM micrographs of two variations of the SOLES structure. The buried Ge layer is incorporated into the substrate either through a) a SiGe graded buffer [1], or b) by the SmartCutTM process [2].

REFERENCES

[1] C. L. Dohrman, K. Chilukuri; D. M. Isaacson; M. L. Lee, and E. A. Fitzgerald, "Fabrication of silicon on lattice-engineered substrate (SOLES) as a platform for monolithic integration of CMOS and optoelectronic devices," Materials Science and Engineering B: Solid-State Materials for Advanced Technology, vol. 135, no.3, pp.235-237, Dec. 2006.

[2] F. Letertre, "Formation of III-V Semiconductor Engineered Substrates Using Smart CutTM Layer Transfer Technology," in Mater. Res. Soc. Symp. Proc. 2008, pp. 1068-C01-01

[3] K. Chilukuri, M. J. Mori, C. L. Dohrman, and E. A. Fitzgerald, "Monolithic CMOS-compatible AlGaInP visible LED arrays on silicon on lattice-engineered substrates (SOLES)," Semiconductor Science and Technology, vol. 22, pp. 29-34, 2007.

[4] W. K. Liu, D. Lubyshev, J. M. Fastenau, Y. Wu, M. T. Bulsara, E. A. Fitzgerald, M. Urteaga, W. Ha, J. Bergman, B. Brar, W. E. Hoke, J. R. LaRoche, K. J. Herrick, T. E. Kazior, D. Clark, D. Smith, R. F. Thompson, C. Drazek, N. Daval, "Monolithic integration of InP-based transistors on Si substrates using MBE," J. Crystal Growth, vol.311, no.7, pp.1979–1983, Mar.2009

Selective Epitaxial Growth of Ultrathin SiGe-on-Si for CMOS Applications

M. Kim, J. L. Hoyt
Sponsorship: DARPA

The selective epitaxial growth of ultrathin SiGe-on-Si for structures suitable for CMOS devices has been studied. Very thin $Si_{0.3}Ge_{0.7}$ (thickness less than 12nm) was grown in exposed Si regions on oxide-patterned Si wafers. The SiGe growth and misfit dislocation density were studied and analyzed as a function of film thickness and window orientation. Intensive TEM techniques were used for this study.

Strained SiGe and Ge channel PMOS have large hole mobility enhancement over traditional Si channels, and it has been shown that the hole mobility can be enhanced up to 10X relative to unstrained Si [1], [2]. Hole mobility in strained SiGe channel MOSFET is increased with increasing Ge composition. However, growing Ge or SiGe with high Ge composition on bulk Si increases the lattice mismatch in the heteroepitaxy. Increasing the Ge composition above 70% does not bring increased mobility enhancement because the channel thickness is limited due to critical thickness constraints [3]. Increasing the critical thickness for strained SiGe grown in small areas will enable thicker SiGe channels and a pathway to avoid the mobility degradation associated with ultra-thin films. In addition, this area of study is of interest for epitaxial growth in small-area SiGe source/drains as a means of increasing compressive strain in Si PMOSFETs.

Past studies showed that growing low-Ge-content (<30%) SiGe in small areas (~10 x 10 um) increases the critical thickness [4]. In this study, we have grown $Si_{0.3}Ge_{0.7}$ on exposed Si regions on oxide-patterned Si wafers, with pattern size spanning sub-microns to a few tens of microns. With this limited area growth, the critical thickness of $Si_{0.3}Ge_{0.7}$ was ~8nm, which is a 3X increase from the equilibrium thickness of 2.5nm (Figure 1). The misfit dislocation for SEG growth is strongly influenced by the processing conditions such as prebake temperature, as well as the shape of the growth area. Figure 2 shows 10-nm-thick $Si_{0.3}Ge_{0.7}$ film, one grown in <110> square oxide opening, the other in 45°rotated feature. Dislocation density is much higher in Figure 2(b), and further study is in progress to understand the effect of window shape on the misfit dislocation density.

REFERENCES

[1] C. W. Leits, M. T. Curie, M. L. Lee, Z-Y. Cheng, D. A. Antoniadis, and E. A. Fitzgerald,„Hole Mobility Enhancements in Strained Si/Si1-yGey p-Type Metal-Oxide-Semiconductor Field-Effect Transistors Growth on Relaxed Si1-xGex (x<y) Virtual Substances," *Applied Physics Letters*, vol. 79, pp. 4276-4278, December 2001.

[2] M. L. Lee and E. A. Fitzgerald, "Optimized strained Si/ strained Ge dual-channel heterostructures for high mobility P- and N-MOSFETs" *IEEE International Electron Devices Meeting 2003*, vol. 19, pp. 18.1.1-4, 2003

[3] C. Ni Chleirigh, "Strained SiGe-channel p-MOSFETs: Impact of Heterostructure design and Process Technology," PhD Thesis, Massachusetts Institute of Technology, Cambridge, 2007.

[4] D. B. Noble, "Misfit Dislocation Formation in Si1-xGex Strained Layers Grown by Limited Reaction Processing," PhD Thesis, Stanford University, Palo Alto, 1991.

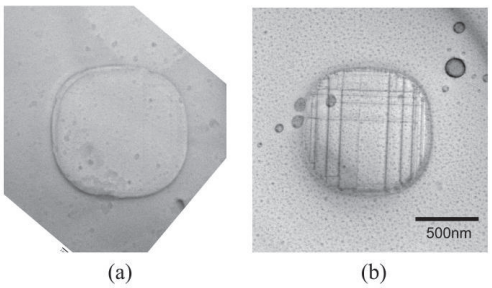


FIGURE 1: Plan-view TEM images of $Si_{0.3}Ge_{0.7}$ films illustrating the critical thickness in small areas. The field region is SiO_2. (a) No misfit dislocation is detected for a 6-nm-thick film. (b) For an11-nm film, dislocations are clearly visible. Scale bar applies to both (a) and (b).

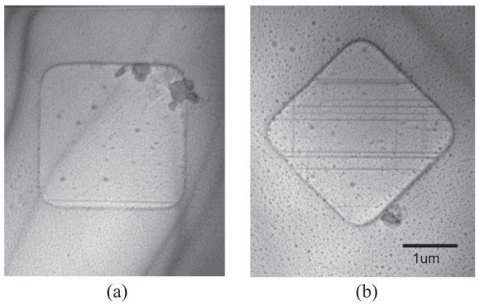


FIGURE 2: Plan-view TEM mages of $Si_{0.3}Ge_{0.7}$ that was grown (a) in <110> square oxide opening, and (b) in 45° rotated feature, which shows higher dislocation density. Both SiGe films are ~10nm thick.

Graphene by Ambient-pressure CVD

A. Reina, S. Thiele, X. Jia, D. Nezich, S. Bhaviripudi, M. S. Dresselhaus, J. Schaefer, J. Kong

Sponsorship: NSF CAREER (DMR-0845358), Intel Higher Education Program, SRC/FCRP MSD, Lincoln Lab Advanced Concept Committee.

We present an approach to grow graphene films consisting of 1 to 10 graphene layers in ambient pressure on thin metal films [1]. The graphene so produced is transferable to non-specific substrates. The growth of graphene occurs by segregation of carbon from the bulk of the metal film. Such segregation takes place in a CVD process in which the metal thin film is cooled down as it is being doped by carbon from a hydrocarbon source. We find that such graphene precipitation can be controlled in ambient pressure conditions in order to obtain coverage of up to 87% of no more than 2 graphene layers.

The size of such films is limited only by the size of the catalytic metal film. Here, we demonstrate sizes of around 1in^2. Transferring of single- and multi-layer graphene to other substrates enables their characterization in isolation from its growth surface. The ambipolar transfer characteristics of the graphene synthesized is demonstrated and electron and holes mobilities of 200-2200 cm^2/Vs were measured. The graphene films also show optical transmittance of 90% in the wavelength range of 400-1000 nm and average sheet resistances of 1 kΩ/sq.

REFERENCES

[1] A. Reina, X. Jia, J. Ho, D. Nezich, H. Son, V. Bulović, M.S. Dresselhaus, and J. Kong, "Large-Area few-layer graphene films on arbitrary substrates by Chemical Vapor Deposition" *Nano Letters*, vol. 9, no. 1, pp. 30–35, 2009

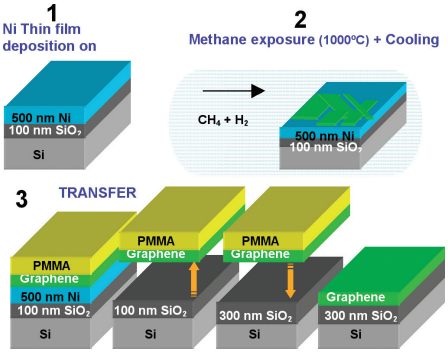


FIGURE 1: Graphene growth and transfer process. 1. Thin films of Ni are deposited on SiO_2/Si by ebeam evaporation and sputtering. 2. The films are annealed and exposed to methane at 1000˚C. Carbon decomposed on the surface of Ni diffuses into the bulk of the Ni film. During cooling, graphene precipitation is generated by carbon segregation from the bulk of the film. 3. Transferring of the graphene film synthesized is enabled by wet etching of the Ni film. A PMMA layer is used as support.

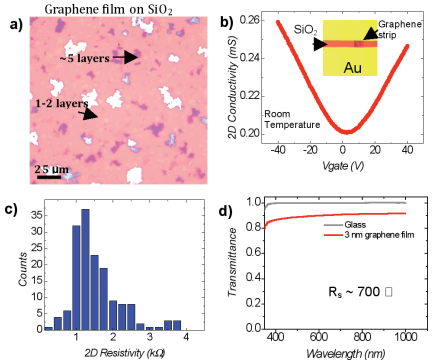


FIGURE 2: a) Optical image of a graphene film transferred to a SiO_2/Si substrate. Most of the area (shown in pink) is covered by no more than 2 graphene layers. Recognition of the number of layers is done by measuring the optical contrast created by the film, which depends on the number of layers. b) Electron transport of a graphene strip on SiO_2/Si and modulated by a back gate. c) 2D resistivities measured by several device geometries such as that shown in the inset of b). d) Optical transmittance of a graphene film fabricated by this method showing a transmittance close to 90% over the wavelength range of 400-1000 nm.

Fabrication of Large-area Graphene-based Electronic Devices

A. Hsu, A. Potter, J. Wu, J. Kong, T. Palacios
Sponsorship: ISN, SRC/FCRP IFC

Since the discovery of graphene in 2004 [1], there has been a tremendous amount of interest in this material for its unique electronic properties. Graphene is a stable two-dimensional material composed of a monolayer of carbon atoms with extremely high electron mobility up to 200,000 cm^2/Vs [2]. Therefore, in nanostructured devices, electrons may undergo ballistic rather than ohmic transport. Additionally, graphene is a zero-band-gap semiconductor with the conduction and valence bands meeting at the Dirac point. However, there has been much interest in using 1-D graphene nanoribbons (GNR) as a method for inducing a band gap at the Dirac point [3]. These exciting properties coupled with the benefits of already mature planar processing technology have fueled the excitement about graphene-based electronics.

Initially, most measurements have been done on isolated graphene flakes through mechanical exfoliation or "the scotch tape method." However, recent developments using chemical vapor deposition (CVD) have demonstrated growth of large areas of single-layer graphene and transfer to arbitrary substrates. [4]. Other work on producing large-area devices has focused mainly on growth of graphene on fixed SiC substrates [5]. Although these growth methods have shown promising results, currently, the best device performances reported have been measured on suspended exfoliated graphene.

Our work focuses on improving the material quality and device processing technology of CVD graphene devices. Work in progress includes utilizing high-k dielectric substrates and self-aligned transistor structures to maximize the frequency performance of graphene transistors and exploring nanoribbon graphene devices fabricated through conventional dry etching and patterned-growth modalities. This project also aims to explore future electronic and optoelectronic applications of graphene devices beyond transistors. We have, for example, recently demonstrated the use of graphene's ambipolar transport for high efficiency frequency doubling [6].

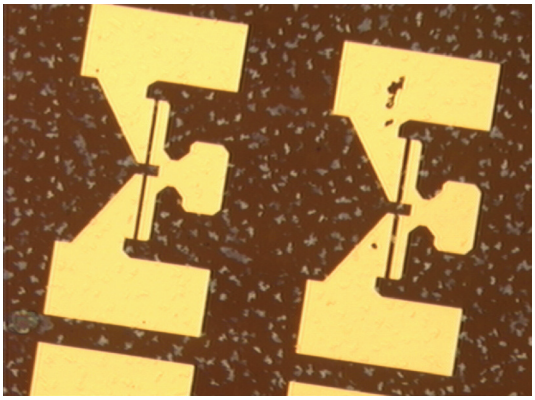


FIGURE 1: Patterned Ohmic Contacts of graphene transferred onto hafnium oxide substrate.

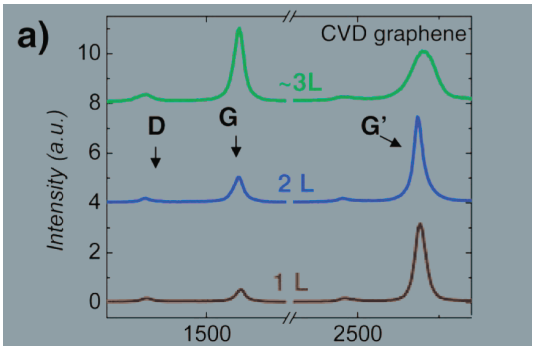


FIGURE 2: Raman spectra for CVD graphene on SiO_2 substrates. The strength of the D band represents defect levels. The ratio of the G' to G provides a rough metric to qualify the number of monolayers of grapheme [6].

REFERENCES

[1] Novoselov, K. S., Geim, A. K., Morozov, S. V., et al. "Electric Field Effect in Atomically Thin Carbon Films," *Science*, vol. 306, pp. 666-669, October 2004.

[2] Du, Xu., Skachko, I., Barker, A., Andrei, E.Y. "Approaching ballistic transport in suspended graphene," *Nature Nanotechnology*, vol. 3, pp. 491-495, July 2008.

[3] Han, M.Y., Ozyilmaz, B., Zhang, Y., Kim, P. "Energy Band-Gap Engineering of Graphene Nanoribbons," *Phys. Rev. Lett.* vol. 98, pp. 206805, May 2007.

[4] Reina, A., Jia X., Ho, J., Nezich, D., Son, H., Bulović, V., Dresselhaus, M., Kong, J. "Large Area, Few-Layer Graphene Films on Arbitrary Substrates by Chemical Vapor Deposition," *Nano Letters*, vol. 9, pp. 30-35, 2009.

[5] Kedzierski, J., Hsu, P., Healey, P., et al. "Epitaxial Graphene Transistors on SiC Substrates," *IEEE Transactions on Electron Devices*, vol. 55, pp. 2078-2085, August 2008.

[6] Wang, H., Nezich, D., Kong, J., Palacios, T., "Graphene Frequency Multipliers," presented at March APS, Pittsburgh, USA, 2009.

Magnetic Oxides for Optical Isolators and Magnetoelectronic Devices

C. A. Ross, G. J. Dionne, A. Taussig, L. Bi, V. Sivakumar, H. S. Kim
Sponsorship: Lincoln Laboratory, ISN, NSF

We have established a thin-film laboratory that includes a pulsed-laser deposition (PLD) system and an ultra-high vacuum sputter/analysis system. In PLD, a high-energy excimer laser is used to ablate a target, releasing a plume of material that deposits on a substrate to form a thin film. The PLD is particularly useful for making complex materials such as oxides because it can preserve the stoichiometry of the target material.

We have been using PLD to deposit a variety of oxide films for magneto-optical devices such as isolators. These materials include iron oxide, which can adopt one of four different ferrimagnetic or antiferromagnetic structures depending on deposition conditions, and bismuth iron garnet (BIG, $Bi_3Fe_5O_{12}$), which is useful for magneto-optical isolators in conventional photonic devices. The ideal material for an isolator combines high Faraday rotation with high optical transparency. Garnets have excellent properties but do not grow well on silicon substrates, making it difficult to integrate these materials. In contrast, iron oxide (maghemite) grows very well on MgO or Si, with high Faraday rotation, but its optical absorption is high. One way to solve this problem is to develop new magneto-optical active materials, which can grow epitaxially on Si by using buffer layers. Through doping with transitional metal ions, these materials can exhibit strong Faraday rotation as well as low optical loss. Recently, we have examined Fe and Co-doped $SrTiO_3$ thin film (Figure 1) [1], which shows strong magneto-optical properties and lower optical absorption compared with iron oxide. The best figure of merits of 1.1 deg/dB and 0.57 deg/dB, which are defined as Faraday rotation divided by optical absorption loss at 1550-nm wavelength, have been achieved in $Sr(Ti_{0.6}Fe_{0.4})O_3$ and $Sr(Ti_{0.7}Co_{0.3})O_3$, respectively. These films could be useful for waveguide isolators and other magnetoelectronic devices in which optical absorption losses are critical. Additionally, As_2S_3/$Sr(Ti_{0.6}Fe_{0.4})O_3$ strip-loaded waveguides were fabricated on epitaxial $Sr(Ti_{0.6}Fe_{0.4})O_3$ on LSAT (001) substrates (Figure 2) [2]. Optical transmission measurements at 1550-nm wavelength confirmed the relatively high transparency of the magneto-optical film. A second project involves the use of electrochemical methods to control the magnetization of iron oxide spinel structure films (magnetite or maghemite) grown on conducting substrates, making a chemically-switchable material. The insertion of Li ions by electrochemical discharge changes the oxidation state of the Fe(III) to Fe(II) and can reduce the magnetization of the film by about 30%, in a reversible process. Recent experiments on nanoparticles of iron oxide show much greater changes in magnetization, up to ~80%, indicating that the process is kinetically limited. Lithiation of CrO_2 also successfully changed the magnetization with an initial change of $10\mu_B$ per Li^+ ion insertion.

REFERENCES

[1] Hyun-Suk Kim, Lei Bi, G. F. Dionne, and C. A. Ross, "Magnetic and Magneto-optical Properties of Fe Doped $SrTiO_3$ Films," *Appl. Phys. Lett.* 93, 092506 (2008)

[2] Lei Bi, Hyun-Suk Kim, Juejun Hu, Lionel C. Kimerling and C. A. Ross, "As_2S_3/$Sr(Ti_{0.7}Co_{0.3})O_3$ and As_2S_3/$Sr(Ti_{0.6}Fe_{0.4})O_3$ strip-loaded waveguides for integrated magneto-optical isolator applications", *Proc. SPIE* 7218, 721803 (2009).

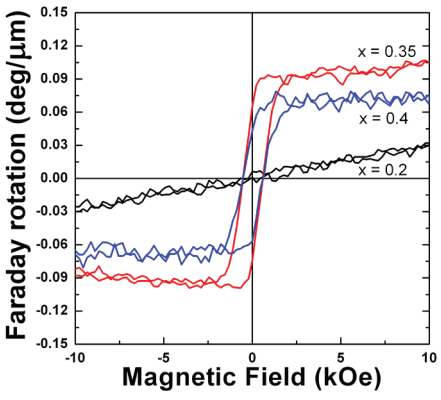


FIGURE 1: Faraday rotation at 1550-nm wavelength vs. applied field for $Sr(Ti_{1-x}Fe_x)O_3$ films grown on $LaAlO_3$ (001) substrates.

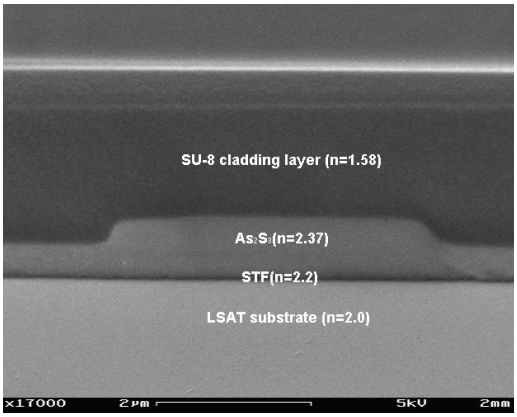


FIGURE 2: Cross-sectional SEM image of an As_2S_3/$Sr(Ti_{0.6}Fe_{0.4})O_3$ strip-loaded waveguide with an SU-8 top-cladding layer fabricated on an LSAT(001) substrate.

Scanning Beam Interference Lithography

M. Ahn, C.-H. Chang, R. Heilmann, Y. Zhao, M.L. Schattenburg
Sponsorship: NASA

Traditional methods of fabricating gratings, such as diamond tip ruling, electron- and laser-beam scanning, or holography, are generally very slow and expensive and result in gratings with poor control of phase and period. More complex periodic patterns, such as gratings with chirped or curved lines, or 2D and 3D photonic patterns, are even more difficult to pattern. This research program seeks to develop advanced interference lithography tools and techniques to enable the rapid patterning of general periodic patterns with much lower cost and higher fidelity than current technology.

Interference lithography (IL) is a maskless lithography technique based on the interference of coherent beams. Interfering beams from an ultra-violet laser generates interference fringes, which are captured in a photo-sensitive polymer resist. Much of the technology used in modern IL practice is borrowed from technology used to fabricate computer chips. Traditional IL methods result in gratings with large phase and period errors. We are developing new technology based on interference of phase-locked scanning beams, called scanning beam interference lithography (SBIL). The SBIL technique has been realized in a tool called the MIT Nanoruler, which recently won an R&D 100 award (Figure 1). Large gratings can be patterned in a matter of minutes with a grating-phase precision of only a few nanometers and a period error in the ppb range.

Current research efforts seek to generalize the SBIL concept to pattern more complex periodic patterns, such as variable period (chirped) gratings, 2D metrology grids, and photonic patterns [1]. Important applications of large, high-fidelity gratings are for high-resolution x-ray spectroscopes on NASA x-ray astronomy missions, high energy laser pulse compression optics, and length metrology standards. We have recently developed a new grating patterning technique called aligned multiple overlay SBIL, which uses multiple (up to four) precisely overlaid IL images to divide the fundamental grating pattern down to very short periods, in this case 50-nm pitch, over large areas (Figure 2). This type of pattern has many applications including nanomagnetics, semiconductor, and nanobio manufacturing.

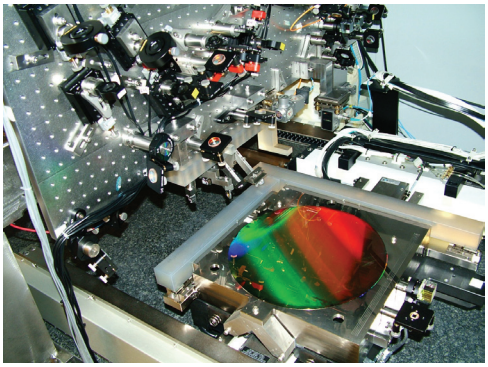


FIGURE 1: Photograph of the Nanoruler lithography and metrology system built by MIT students. This unique tool is the most precise grating patterning and metrology system in the world.

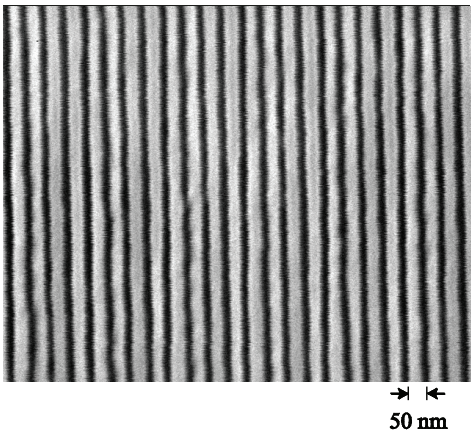


FIGURE 2: A 50-nm pitch (25-nm line/space) grating pattern fabricated by 4X overlaid interference lithography.

REFERENCES

[1] "Doppler writing and linewidth control for scanning beam interference lithography," J. Montoya, C.-H. Chang, R.K. Heilmann and M.L. Schattenburg, *J. Vac. Sci. Technol. B* **23**, 2640-2645 (2005).

[2] "Phase control in multiexposure spatial frequency multiplication," Y. Zhao, C.-H. Chang, R.K. Heilmann and M.L. Schattenburg, *J. Vac. Sci. Technol. B* **25**, 2439-2443 (2007).

[3] "Design of a double-pass shear mode acousto-optical modulator," C.-H. Chang, R.K. Heilmann, M.L. Schattenburg and P. Glenn, *Rev. Sci. Instr.* **79**, pp. 033104-1-5 (2008).

[4] "Fabrication of 50 nm-period gratings with multilevel interference lithography," C.-H. Chang, Y. Zhao, R.K. Heilmann and M.L. Schattenburg, *Opt. Lett*. **33,** 1572-1574 (2008).

[5] "Spatial-frequency multiplication with multilayer interference lithography," C.-H. Chang, Y. Zhao, R.K. Heilmann and M.L. Schattenburg, *J. Vac. Sci. Technol. B* **26**, 2135-2138 (2008).

Spatial-phase-locked Electron-beam Lithography

E. E. Moon, L. L. Cheong, H. I. Smith, J. T. Hastings (U. Kentucky)
Sponsorship: NSF

Our research in spatial-phase-locked electron-beam lithography (SPLEBL) is conducted in collaboration with the University of Kentucky. It is aimed at reducing pattern-placement errors in scanning electron-beam-lithography systems to the sub-1 nm level. Such high precision is essential for certain applications in photonics and nanoscale science and engineering. SPLEBL is currently the only approach capable of achieving such pattern-placement accuracy. As shown in Figure 1, SPLEBL uses a periodic signal, derived from the interaction of the scanning e-beam with a fiducial grid placed directly on the substrate, to continuously track the position of the beam while patterns are being written. Any deviation of the beam from its intended location on the substrate is sensed, and corrections are fed back to the beam-control electronics to cancel beam-position errors. In this manner, the locations of patterns are directly registered to the fiducial grid on the substrate. The research effort at MIT is now focused on developing the materials and processes for producing the fiducial grid, with the objectives of: maximizing the signal-to-noise of the secondary-electron signal derived from the grid; minimizing electron scattering from the grid, which would be deleterious to precision lithography; maximizing the area and absolute accuracy of the grid; and minimizing the cost and inconvenience of producing the grid on substrates of interest.

The current approach derives the modulation of the secondary-electron signal purely from the topography of the grid. The fabrication is exceedingly simple: the electron beam resist is covered with a grid in a G-line resist, and a few-nanometer coating of metal. Since most e-beam resists are not sensitive in the visible and near-UV, and since most e-beam resists are dissolved in different solvents than are G-line resists, we are able to use the two resists independently. We expose the G-line resist to interference lithography (using a Mach-Zender interferometer or coherent-diffraction lithography) and develop it to form the fiducial pattern. We then uniformly coat the grid with a metal such as Al, providing an enhancement of secondary-electron yield at the vertical sidewalls. When an electron beam scans across such a pattern there are spikes in the secondary electron emission from the sides of the vertical walls, due to enhanced electron escape probability along the sidewalls, as illustrated in the data in Figure 2. The metal and photoresist are stripped before the e-beam resist is developed. Further research will include selection of the grid thickness, metal thickness, and metal type to optimize the signal-to-noise ratio. In addition, if there is incompatibility of solvents between the G-line resist and the e-beam resist we can add a thin film of water-soluble poly-vinyl alcohol between the electron-beam resist and the G-line resist. Finally, the shape of the grid sidewalls can be tailored to optimize the secondary-electron signal in the fundamental grid frequency, and minimize the higher spatial frequency lobes observed in Figure 2.

REFERENCES

[1] J. T. Hastings, F. Zhang, and H. I. Smith, "Nanometer-level stitching in raster-scanning e-beam lithography using spatial-phase locking," *J. Vac. Sci. Technol. B*, vol. 21, no. 6, pp. 2650-2656, Nov/Dec 2003.

[2] F. Zhang, H. I. Smith and J. F. Dai, "Fabrication of high-secondary-electron-yield grids for spatial-phase-locked electron-beam lithography," *J. Vac. Sci. Technol. B*, vol. 23, no. 6, pp. 3061-3064, Nov/Dec 2005.

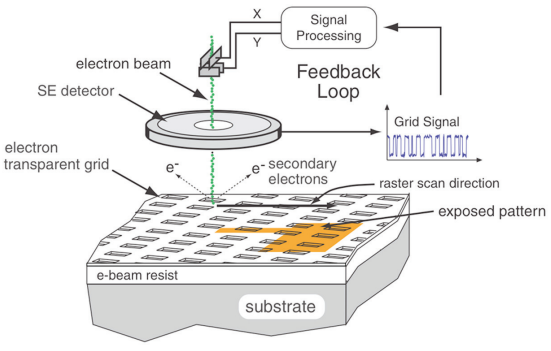


FIGURE 1: Schematic of the global-fiducial-grid mode of spatial-phase-locked electron-beam lithography. The periodic signal detected from the fiducial grid, which includes both X and Y components, is used to measure placement error, and a correction signal is fed back to the beam-deflection system.

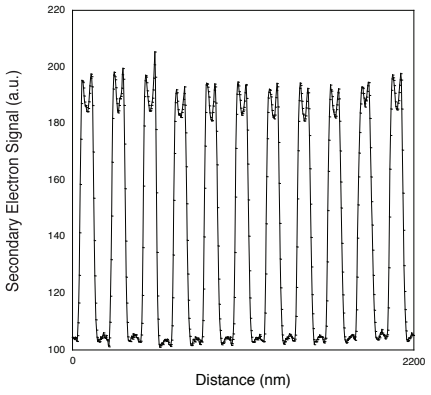


FIGURE 2: Plot of the secondary-electron yield in a fiducial pattern composed of PFI-88 photoresist covered with 3 nm of Au/Pd, averaged along one direction.

Fabrication of Free-standing Silicon-Nitride Zoneplates for Neutral-helium Microscopy using Segmented-grid-spatial-phase-locked Electron-beam Lithography

T. Reisinger, C. Fucetola, T. B. O'Reilly, L. L. Cheong, H. I. Smith, B. Holst
Sponsorship: Bergen Research Foundation

Neutral-helium microscopy is a relatively new technique that employs a focussed supersonic-expansion helium beam (~50meV) to image a sample in scanning mode. It potentially offers significant advantages. Firstly, the atoms are neutral, which means that insulating surfaces can be imaged without prior coating. Furthermore, the energy of the beam (a few tens of meV for a wavelength of about 1 Å) is very low, a factor of 1000 less than electrons for a similar wavelength. This means that fragile samples can be investigated without any damage. Helium atoms can be focussed in a number of ways, but Fresnel zoneplates have achieved the smallest beam focus so far (1μm). The first transmission-mode images created using this technique was published early 2008 [1].

In order to further improve the technique, we have developed a new fabrication process for free-standing Fresnel zoneplates to be used as focusing elements in a scaled-down and stabilised setup designed to improve resolution to about 300 nm (full width half maximum) and create the first reflection mode images. The quality of the images obtained using this technique will strongly depend on the diffraction efficiency of the fabricated zoneplates, which is determined by how closely the zoneplate resembles the ideal. Scanning electron-beam lithography (we used the RAITH 150 system available at RLE's SEBL facility) provides the necessary resolution, but pattern fidelity is limited by intra- and inter-writefield distortion. We have developed a fabrication process for the free-standing zoneplates and are currently working on minimizing both mentioned distortion errors using interference lithography gratings as a reference (see Figures 1 and 2) [2].

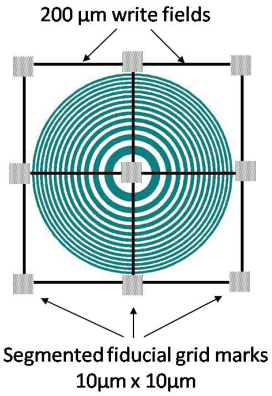


FIGURE 1: Schematic of spatial-phase locking approach for a zoneplate pattern using a segmented fiducial grid. The marks at the corner of the 200-μm writefields are dot-grids with a period of 200 nm, which were created by segmenting a Mach-Zehnder interference-lithography grid. They are used to align the writefield to the substrate as well as relative to each other, by scanning the write-field at the corners which are not relevant to the zoneplate pattern. The result will be a zoneplate with higher diffraction efficiencies.

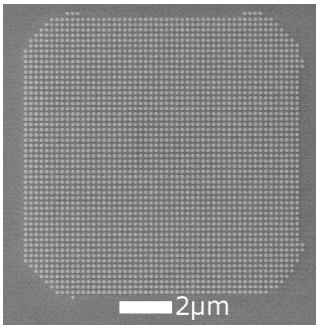


FIGURE 2: SEM micrograph of the segmented-grid alignment-mark. The titanium-gold dots are arranged in a 200-nm grid, where the two grid-axes subtend an angle of 90° to an accuracy of better than 1 arc minute. The segmentation was achieved using standard contact-ultraviolet-lithography. The spatial phase of these marks is measured for each write field by two orthogonal line scans and the writefield alignment is updated based on that spatial phase at three writefield corners.

REFERENCES

[1] M. Koch, S. Rehbein, G. Schmahl, T. Reisinger, G. Bracco, W. E. Ernst, and B. Holst, J. Mic. (cover story) 229, 1 (2008). See also Nature Research Highlights: Nature 451, p.226-227, 2008.

[2] J. T. Hastings. Nanometer-Precision Electron-Beam Lithography with Applications *in Integrated Optics*. PhD thesis, Massachusetts Institute of Technology, June 2003.

Design and Fabrication of Sampled Bragg Gratings in SOI

J. Sun, C. W. Holzwarth, H. I. Smith
Sponsorship: DARPA

Waveguide Bragg gratings are used in optical communication systems for many applications. However, in order to achieve more advanced grating properties, such as phase shift and chirp, Scanning-Electron-Beam-Lithography (SEBL) with special precision-control techniques (e.g. Spatial-Phase-Locked EBL) represents one approach. We propose a novel sampled-Bragg grating (SBG) structure to realize various grating responses using optical lithography only. In this scheme, interference lithography is used to fabricate the background grating with excellent coherence, and then the background grating is amplitude-modulated to achieve various grating responses. In SBG, various grating responses are realized by reallocating the sampling positions and by varying the duty cycle of each sampling. For example, the phase shift grating is achieved by phase shifting the sampling instead of the grating itself. Figure 1(a) shows the simulated transmission spectrum of a phase shift grating using SBG, where the desired filter response appears in the -1st channel. Similarly, the chirp grating is achieved by chirping the sampling period, as shown in Figure 1(b).

The sampling period is usually of the order of ~10mm, which is much larger than the grating period and enables to use optical-contact lithography. A processing flow for SBG fabrication was developed. A thin layer of SiO_2 was first evaporated on top of an SOI wafer. The background grating was formed on this layer through interference lithography. This SiO2 grating layer will serve as a hard mask to etch grating into silicon later. Then the sampling pattern was transferred onto the grating layer by optical-contact lithography and etching away excess background grating. After this, a second contact lithography was performed to pattern the waveguides and HBr etching was used to transfer the waveguide pattern into silicon to form a ridge waveguide. Finally, the grating pattern was etched into the top of the silicon ridge waveguide to a certain depth to form the SBG. Figure 2(a) shows the micrograph of a fabricated SBG, and Figure 2(b) shows the cross-sectional view of the SBG under Scanning-Electron-Microscope.

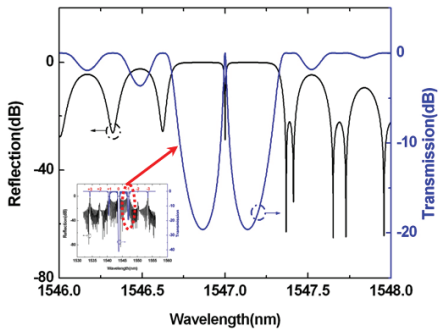


FIGURE 1(A): Simulated response of a phase-shift grating using SBG.

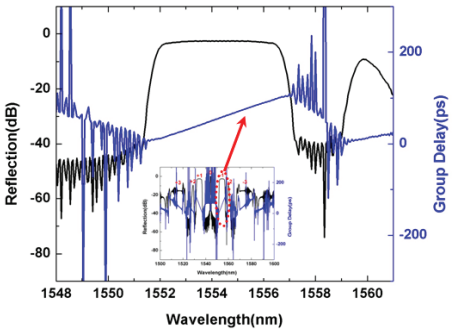


FIGURE 1(B) Simulated response of a chirp grating using SBG

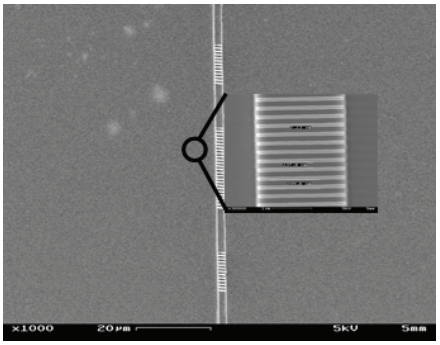


FIGURE 2(A): SEM of a fabricated SBG

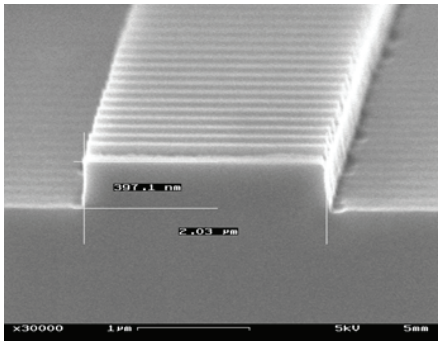


FIGURE 2(B): Cross-sectional view of the SBG

Anodic Aluminum Oxide Scaffolds for IC Interconnect and Energy-storage Applications

J. Oh, Y. C. Shin, A. Al-Obeidi, C. V. Thompson
Sponsorship: NSF

Metallic nanowires and nanotubes are promising candidates for advanced electrode arrays for sensor arrays and energy storage applications such as micro-batteries [1], [2]. To integrate synthesized nanowires into the devices, it is desirable to fabricate them with controlled size and location on the device-applicable substrates.. As a strategy, we are developing templated self-assembly methods that combine top-down (lithography) and bottom-up (self-assembly) approaches for fabricating and assembling various metallic nanowires and nanotubes for sensor and energy-storage applications [3].

Ordered porous alumina (OPA) is a nano-structured material that self-orders with domains and has been widely used as a template for growth of metallic nanowires and nanotubes [3]. However, the nanowires grown in the OPA are electrically blocked from the substrate due to a thin insulating barrier oxide at the base of the pores. While it is desirable to remove the thin barrier oxide, this removal is normally done using chemical etching, a barrier-thinning technique, or a reverse-bias technique [4]. These methods lead to pore widening and are difficult to implement for OPA on substrates, with difficulties increasing for small-diameter pores and pores with small spacings.

A new method for perforation of the OPA barrier layer has been developed, based on anodization of Al/W multilayer films on substrates [5]. When Al/W multilayer films are anodized and pores approach the Al/W interface, tungsten oxide forms and penetrates the alumina barrier oxide. After selective etching of the tungsten oxide, the base of the pores opened, without etching of the OPA (Figure 1). With this technique, we have demonstrated that it is possible to perforate OPA barrier layers for porous structures with small-diameter pores at small spacings and fabricated free-standing metallic nanowires, such as Ni, Au, and Pt, and carbon nanotubes on metallic layers on Si substrates (Figure 2) by selectively removing the OPA template. Using these NWs and NTs with or without the AAO as a platform, we are testing electronic characteristics for future IC interconnects and developing a micro-battery.

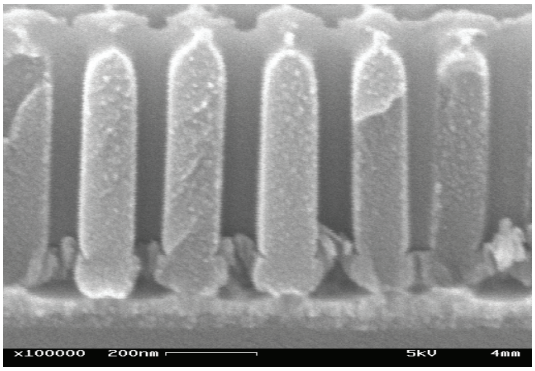


FIGURE 1: Cross-sectional SEM image of ordered porous alumina (OPA) after removal of thin barrier oxide.

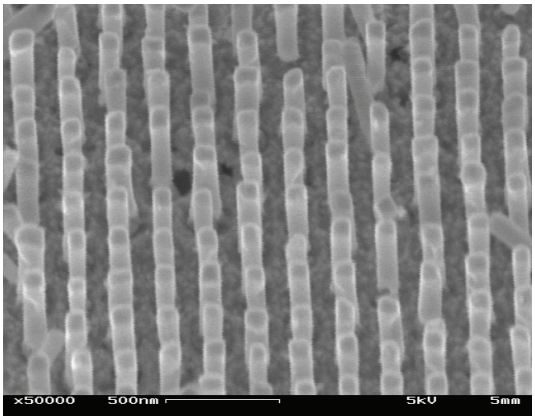


FIGURE 2: An SEM image of free-standing Ni nanowires on a conducting layer on Si substrates.

REFERENCES

[1] A. Naeemi and J. D. Meindl, "Compact physical models for multiwall carbon-nanotube interconnects," *IEEE Electron Device Letters,* vol. 27, pp. 338-340, May 2006.

[2] C. K. Chan, H. L. Peng, G. Liu, K. McIlwrath, X. F. Zhang, R. A. Huggins, and Y. Cui, "High-performance lithium battery anodes using silicon nanowires," *Nature Nanotechnology,* vol. 3, pp. 31-35, Jan 2008.

[3] R. Krishnan and C. V. Thompson, "Monodomain high-aspect-ratio 2D and 3D ordered porous alumina structures with independently controlled pore spacing and diameter," *Advanced Materials,* vol. 19, pp. 988-+, Apr 6 2007.

[4] O. Rabin, P. R. Herz, Y. M. Lin, A. I. Akinwande, S. B. Cronin, and M. S. Dresselhaus, "Formation of thick porous anodic alumina films and nanowire arrays on silicon wafers and glass," *Advanced Functional Materials,* vol. 13, pp. 631-638, Aug 2003.

[5] J. Oh and C. V. Thompson, "Selective barrier perforation in porous alumina anodized on substrates," *Advanced Materials,* vol. 20, pp. 1368-+, Apr. 2008.

Medical Electronics

High-throughput Arrayed Comets for DNA Damage and Repair

D. K. Wood, D. M. Weingeist, B. P. Engelward, S. N. Bhatia
Sponsorship: National institute of Environmental and Health Sciences

DNA damage has long been known to contribute to cancer, aging, neurological disorders, and heritable diseases. Although effective methods for assessing DNA damage levels have been available for decades, and it is well established that information about DNA damage levels is highly useful both in the clinic and in population studies, measurements of DNA damage are far from routine. The core experimental method for this work is the well-established comet assay, in which cells are embedded in agarose, exposed to buffers that dissolve the cell membrane and denature DNA, and subjected to electrophoresis. The governing principle is that damaged DNA migrates more readily than undamaged DNA, which tends to stay tightly wound within the nucleoid.

A major goal was to increase throughput by using patterning techniques to enable analysis of cells within a defined array. We optimized a patterning method that captures cells in microwells [1], [2] that are molded directly into agarose gel (Figure 1). This method enables capture of single or multiple cells, controlled by well size, and produces analyzable comets from any amount number of cells (Figure 1). The tunable well size and the biocompatibility of agarose also enable studies on any cell type. This platform has proved effective for studying multiple irradiation and chemical exposures on a single slide. Figure 2 demonstrates X-ray dose response studies, where 10 doses were measured on a single slide, and 3 different cell types were studied. We have further improved throughput with automated image analysis software and are using fluorescent labeling to multiplex conditions, cell types, and biomarkers. We will continue to increase the versatility and through-put with automated chemical spotting. We hope ultimately to provide an assay that is simple and easy enough to be useful in a broad range of clinical, epidemiological, and experimental gene-environment interaction studies.

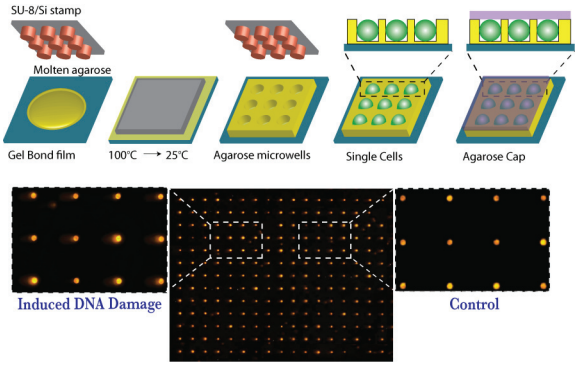


FIGURE 1: Fabrication of the comet-chip. Microwells are molded directly into agarose gel using a lithographically patterned Si/SU-8 stamp. Cells are loaded into the wells by gravitational settling, and an agarose capping layer encapsulates the cells. Lower panels show patterned comets from an experiment where cells are treated with PBS or H2O2.

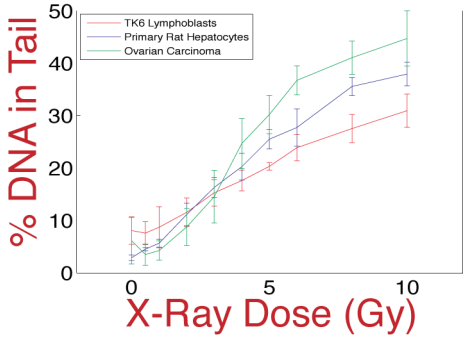


FIGURE 2: Dose response of cells treated with X-ray radiation. Colored lines represent different cell types. Ten X-ray doses were applied to each comet-chip.

REFERENCES

[1] J. R. Rettig and A. Folch, "Large-scale single cell trapping and imaging using microwell arrays," *Analytical Chemistry*, vol. 77, no. 17, pp. 5628-5634, Sept. 2005.

[2] A. Rosenthal, A. MacDonald, J. Voldman, "Cell patterning chip for control of the stem cell microenvironment," *Biomaterials*, vol. 28, no. 21, pp. 3208-3216, July 2007.

Development of Modeling Tools for the Human Cardiovascular Circulatory System

T. A. El-Moselhy, L. Daniel
Sponsorship: NSF

Studying certain medical conditions, such as hypertension, requires the simulation of the whole cardiovascular system, including arteries, veins, and various organs treated as vascular beds. Such a requirement renders full 2- or 3-D coupled fluid-structural simulations impractical due to their high demand in computational resources. The computational efficiency of lower dimensional models comes at a cost of sacrificing correctness. For instance, 1-D artery models cannot accurately model bends and bifurcations in the major arteries that significantly alter fluid flow, and 0-D vascular bed models cannot provide spatial information. One way to overcome the computational complexities associated with high dimensional models without sacrificing the accuracy is to develop techniques that generate automatically reduced order models from fluid-structural simulators for complex arterial segments, such as bends and bifurcations, to faithfully reproduce the flow and pressure at each end of such segments.

As a first step toward generating reduced order models for arterial segments, we developed a 2-D fluid-structure interaction solver to accurately simulate blood flow in arteries with bends and bifurcations. Such blood flow is mathematically modeled using the incompressible Navier-Stokes equations. The arterial wall is modeled using a linear elasticity model [1]. Our solver is based on the immersed boundary method (IBM) [2]. The numerical accuracy of our solver stems from using a staggered grid for the spatial discretization of the incompressible Navier-Stokes equations [3]. The computational efficiency of our method stems from using Chorin's projection method for the time stepping, coupled with the fast Fourier transform (FFT) to compute the pressure [2]. We have validated our results versus reference results obtained from MERCK Research Laboratories for a straight vessel of length 10cm and diameter 2cm. Our results for pressure, flow, and radius variations are within 3% of those obtained from MERCK.

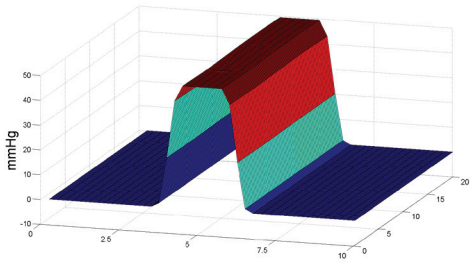


FIGURE 1: Pressure build-up inside artery at time 0.165 sec. Almost uniform pressure observed inside straight artery and almost zero pressure observed outside the artery.

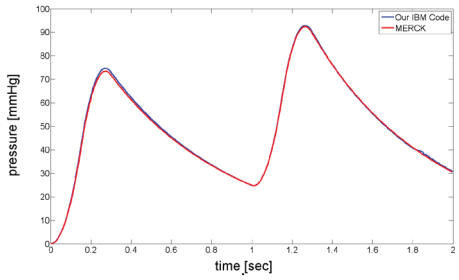


FIGURE 2: Pressure at the middle of a straight 10cm artery as a function of time. Simulations performed using our immersed boundary method code and compared to reference results obtained from MERCK.

REFERENCES

[1] A. Quarteroni, M. Tuveri, and A. Veneziani "Computational vascular fluid dynamics: problems, models and methods" Computing and Visualization in Science, 2000

[2] C. Peskin and D. McQueen "A Three- Dimensional Computational Method for Blood Flow in the Heart I. Immersed Elastic Fibers in a Viscous Incompressible Fluid" Journal of Computational Physics, 1989.

[3] B. Seibold "http://math.mit.edu/classes/18.336/"

Electrokinetic Accumulation of Enzymatic Product Enhances Detection Sensitivity in Microfluidic ELISA

L. F. Cheow, S. H. Ko, K. H. Kang, J. Han
Sponsorship: Agency for Science, Technology and Research, Singapore

We present a method to enhance detection sensitivity of microfluidic bead-based ELISA by accumulating fluorescent product molecules using nanofluidic electrokinetic preconcentration. Bead-based ELISA integrated on a microchip has been shown to provide a lower detection limit and require a shorter assay time [1], but signal intensity does not increase with time as the reaction product is continuously flushed away. We circumvent this limit by utilizing a nanofluidic electrokinetic preconcentrator to accumulate fluorescent product molecules downstream of the reaction zone and show that signal intensity increases with time, therefore greatly improving the detection sensitivity.

The experimental procedure is explained below. The sandwich immunoassay consisting of antibody-coated beads, carbohydrate antigen CA19-9 in serum, and HRP-coupled secondary antibody is conducted in a microcentrifuge tube. After extensive washing, the functionalized beads are physically trapped in front of pillar structures within the microchannel. Downstream of the self-assembled bead array is a nanochannel fabricated using the method in [3]. When voltages are applied at the reservoirs, electroosmosis induces flow of the substrate solution across the beads. Fluorescent product is continuously generated as the enzymes in the bead array catalyze the reaction between the substrate molecules. At the vicinity of the nanochannel, electrokinetic trapping lead to accumulation of the charged fluorescent product molecules and clear increase in signal intensity.

The results are shown in Figure 1. When the antigen concentration is 0 U/mL, the intensity ratio between the product and fluorescein tracer is 1:3. This ratio becomes 1:2 and 2:1 when the antigen concentration is increased to 0.05 U/mL and 0.5 U/mL respectively. Without preconcentrating product molecules, the detection limit of bead-based micro ELISA is 5 U/mL. Therefore, this method enables us to detect at least 100X fewer enzyme molecules and increase the dynamic range by 2 orders of magnitude.

REFERENCES

[1] K. Sato, M. Yamanaka, T. Hagino, M. Tokeshi, H. Kimura, and T. Kitamori,, "Microchip-based enzyme linked immunosorbent assay (microELISA) system with thermal lens detection," *Lab on a Chip*, vol. 4, pp. 570-575, 2004 .

[2] J. H. Lee, Y. Song, S. R. Tannenbaum, and J. Han, "Increase of reaction rate and sensitivity of low-abundance enzyme assay using micro/nanofluidic preconcentrator chip," *Analytical Chemistry*, vol. 80, no. 9, pp. 3198-2104, Mar.2008.

[3] S. J. Kim and J. Han, "Self-sealed vertical polymeric nanoporous junctions for high throughput nanofluidic applications," *Analytical Chemistry*, vol. 80, no. 9, pp. 3507-3511, Apr. 2008.

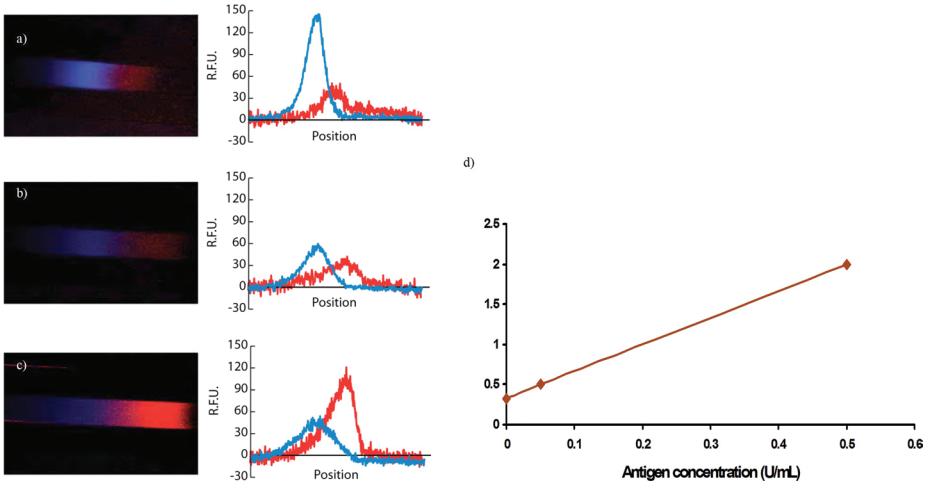


FIGURE 1: Experimental results: Fluorescence intensity of product molecules (red) and tracer (blue) for antigen concentration a) 0 U/mL b) 0.05U/mL c) 0.5 U/mL and d) linear relationship between intensity ratio and antigen concentration.

Microfluidic-based Preparative Protein Separation by Free-flow Isoelectric Focusing (FF-IEF)

J. Wen, J. Albrecht, E. W. Wilker, M. B. Yaffe, K. F. Jensen
Sponsorship: Army Research Office - ISN, Koch Center for Cancer Research, Department of Biology

Isoelectric Focusing (IEF) is the first step for 2-D gel electrophoresis and plays an important role in sample purification for proteomics research. Microfluidic-based IEF has been developed recently in the analytical scale but is less feasible for protein samples with milliliters in volume and milligrams in mass. In this work we have overcome these limitations of traditional IEF with a novel microfluidic free flow IEF (FF-IEF) device in a preparative scale for continuous protein separation in the liquid phase. The 5- by 7-cm device with 24 outlets was fabricated by soft lithography through a PDMS/glass feature (Figure 1). Novel design of the triangular-shape separation channel facilitates the establishment of the pH gradient with not only a corresponding increase in separation efficiency but also a decrease in focusing time. Multiple outlets of 24 fractions facilitated the sample collection and solution handling. We showed the reproducible establishment of the pH gradient from 10 to 4 in a linear fashion.

The electric field and potential efficiency across the separation channel were optimized with consideration of Joule-heating removal. After the shaping of the PDMS prior to the device binding, a functionalized polyacrylamide gel region at the bottom of the device was selectively controlled to adjust the ratio of the applied potential across the separation channel. Energy consumption across the functionalized polyacrylamide gel was investigated and selectively controlled to adjust the potential efficiency between 15-80% across the triangular separation channel. The length of the polyacrylamide gel was found to have a critical effect on the electric fields and could block as much as 99% of applied voltage. The device can achieve constant electric fields as high as 370 ± 20 V/cm through the entire triangular channel given the separation voltage of 1800 V, enabling a powerful micro-device for different separation environments.

Protein samples with a dynamic concentration range between μg/mL and mg/mL could be loaded into the micro device at a flow rate of 1 mL/hr and residence time of ~12 min. We have demonstrated the improved separation using the FF-IEF system over the traditional 2D gel electrophoresis on a protein complex of 9 proteins and 13 isoforms. Post-device sample concentrations result in a 10-20-fold increase, which allows for isolation and detection of low-abundance proteins. This preparative micro-device would also benefit proteomics research by retaining high molecular weight proteins, providing a higher yield of protein that has a broader range in pI, and saving 98% of the experimental time compared to a conventional IEF IGP gel strip (30 min instead of 23-36 hrs.

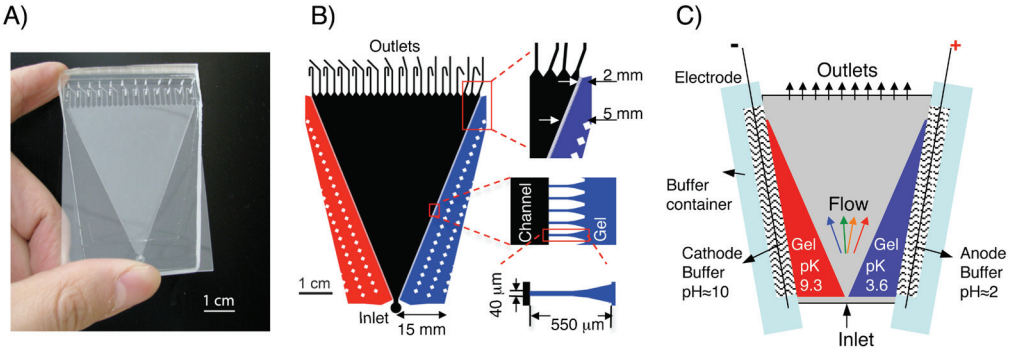


FIGURE 1: A) A FF-IEF device. B) The FF-IEF device design. C) Schematic drawing of microfluidic FF-IEF system. A functionalized pH gradient cathode (pK=9.3) and anode (pK=3.6) polyacrylamide gels were polymerized into the gel regions that were connected to the separation channel. Polyacrylamide gel sections both have 5mm in width on the top from the first post to the side and 15 mm on the bottom from the inlet to the side. A poster structure (squares) was included in the gel regions for support. The device is 5 cm by 7.5 cm with the center triangular separation channel of 4.6 cm in top width and 5.6 cm in height. All channels and channels have a depth of 160 mm.

Microfluidic Studies of Cancer Invasion

I. K. Zervantonakis, S. Chung, W. J. Polacheck, R. D. Kamm
Sponsorship: Draper Laboratory

Cell invasion is a central component of cancer metastasis, enabling tumor cells to escape from the primary organ and form metastases in distant sites, which are the cause for 90% of cancer deaths. The importance of the tumor microenvironment, including biochemical and biophysical factors, is well recognized in the metastatic cascade as an important regulator of the invasive phenotype. Microfluidic devices offer a unique tool for designing and performing *in vitro* assays that allow for control of these microenvironment cues while enabling high-quality imaging of cellular behavior. Our microfluidic device design for the cancer invasion assays is based upon previous work over the past years in our lab [1]-[3]. The design consists of independently addressable microfluidic channels interconnected through 3D matrices, wherein tumor cells can be seeded, while establishing interstitial flow and/or chemoattractant gradients through the matrix (Figure 1).

During the previous year we have used breast cancer (MDA231) and human glioblastoma (U87MG) cell lines in collagen type I matrices to perform chemotaxis and interstitial flow assays. We found that in the presence of an epidermal growth factor (EGF) gradient, both cancer cell lines extended long protrusions and migrated preferentially in the direction of the gradient. However, although both cell types demonstrated 3D cell motility, multiple individual U87MG cells invaded the gel, while the MDA231 showed a more collective cell-migration strategy (Figure 2). In the interstitial flow experiments, we embedded MDA231 cells inside the 3D matrices and assayed for their alignment to the flow streamlines. The results demonstrated that a slow interstitial flow of 3μm/s, comparable to flow velocities in tumors *in vivo*, resulted in alignment of the tumor cells that extended long protrusions along the streamlines, contrary to the control, where the cells were randomly orientated in the gel. Both results demonstrate that chemoattactant gradients and interstitial flow are critical regulators of tumor invasiveness and have important implications for the dissemination of tumor cells from the primary site. Ongoing work includes quantification of tumor cell invasion using time-lapse confocal microscopy for tracking single cells and measuring their migration characteristics. Furthermore, we are performing assays for probing tumor-endothelial cell interactions in the context of cancer angiogenesis and intravasation.

REFERENCES

[1] Chung S, Sudo R, Mack PJ, Wan CR, Vickerman V, Kamm RD. 2009. Cell migration into scaffolds under co-culture conditions in a microfluidic platform. *Lab Chip* 9: 269-75

[2] Sudo R, Chung S, Zervantonakis IK, Vickerman V, Toshimitsu Y, et al. 2009. Transport-mediated angiogenesis in 3D epithelial coculture. *FASEB J* 23(7):2155-64.

[3] Vickerman V, Blundo J, Chung S, Kamm R. 2008. Design, fabrication and implementation of a novel multi-parameter control microfluidic platform for three-dimensional cell culture and real-time imaging. *Lab on a Chip* 8: 1468-77

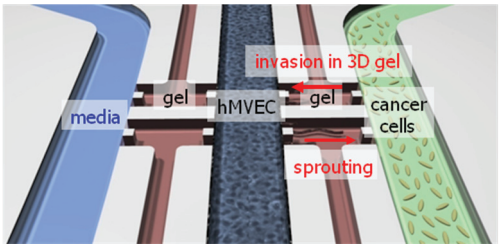


FIGURE 1: Microfluidic device design for studying cancer invasion and tumor-endothelial cell interactions. Cells are seeded in independently addressable channels, interconnected through 3D matrices across which chemoattractant gradients and interstitial flow can be established.

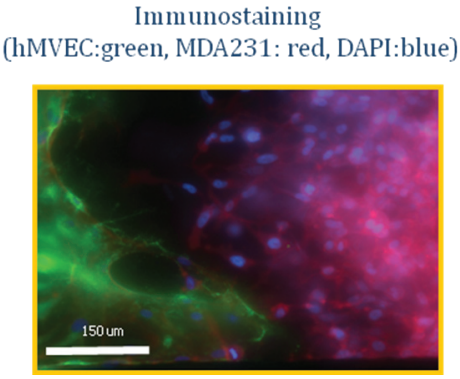


FIGURE 2: Immunostaining of tumor (red) and endothelial (green) cell nuclei (blue) inside the device. Cells are in direct contact, with a few cancer cells migrating individually at the front and an expanding tumor mass at the back

Integrated Microfluidics for Screening Stem Cell Microenvironments

W. G. Lee, W. Y. Sim, B. Chung, A. Khademhosseini
Sponsorship: NIH

Embryonic stem cell (ESC) differentiation is a potentially powerful approach for generating a renewable source of cells for tissue engineering and regenerative medicine [1]. It is known that the microenvironment greatly influences ESC differentiation and self-renewal. Most biological studies have aimed at identifying individual molecules and signals. However, it is becoming increasingly accepted that the wide array of signals in the ESC microenvironment can interact in a synergistic and antagonistic manner based on their temporal and spatial expression, dosage, and specific combinations. This interplay of microenvironmental factors regulates the fate of ESC in terms of decisions to proliferate, self-renew, differentiate, and migrate. Despite this complexity, the study of stem cell cues in a systematic manner is technologically challenging, expensive, slow, and labor intensive. Here we propose to develop an enabling technology based on a high-throughput integrated microfluidics that can overcome many of these challenges. To test the proposed system, we will characterize the integrated device in elucidating specific aspects of mesodermal differentiation in a systematic manner. By providing a way of testing combinatorial microenvironments for directing stem cell differentiation, this approach promises to be of great benefit for cardiac cell and tissue engineering.

To demonstrate the feasibility of the device, we first visualized the functional elements of the device such as fluidic channels, control channels, and microwells (Figure 1). This device was fabricated by multi-layer soft lithography. The fluidic channel made by positive photoresist (AZ 4620) is 30-μm-thick with a round shape, and the pneumatically actuated control channel fabricated by negative photoresist (SU-8 2150) is 40 μm thick. To obtain a round profile of a fluidic channel, the positive photoresist (AZ 4620) was reflowed at 200 °C for 2 min after development. Specifically, the middle layer contained a 20-μm thin RTV615 membrane for the fluidic channel. The crossing of control channels over fluidic channels formed an on-chip barrier valve.

To characterize the cell culture environment for the device, we seeded mouse ESCs into the fluidic channel of the device, docked into specific microwells, and then cultured EBs for 5 days (Figure 2). In our experiments, we cultured goosecoid (Gsc)-ESCs, which can show green fluorescent protein (GFP) for mesendodermal stages of the EBs. Note that no GFP indicates undifferentiated cells or ectoderm stage of the EBs. In summary, Gsc-ESCs were well-docked into the microwells, resulting in good EB formation. After a 5-day culture, GFP images were obtained from the EBs within the microwells.

REFERENCES

[1] A. Khademhosseini, R. Langer, J. Borenstein and J. P. Vacanti, "Microscale technologies for tissue engineering and biology," *Proceedings of the National Academy of Sciences, vol.* 103, pp. 2480-2487, Feb. 2006.

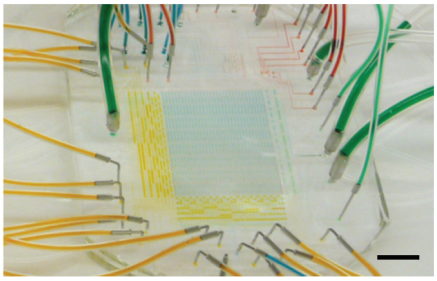


FIGURE 1: Visualization and compartmentalizaton of functional elements of the microfluidic screening device. Note fluidic pathways (green), multiplexed valves (yellow), vertical compartments and mixers (red), and horizontal compartments (blue). Scale bar is 10 mm.

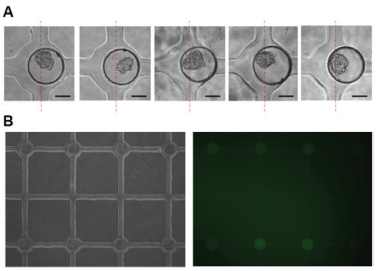


FIGURE 2: Characterization of EB formation of Gsc-ESCs and 5-day culture of the EBs within the microwells of the microfluidic screening device. Note that the GFP (green color) indicates mesendodermal differentiation of the EBs. (A) Observation of EB formation (1 day after cell loading). (B) Phase contrast and fluorescent images of 5-day cultured EBs. Magnification of the objective lens is 10 X. Scale bar is 100 µm.

A Micro Cell chip for Studying Effects of Mechanical Stimulation on the Fate of Mouse Embryonic Stem Cells

W. Y. Sim, W. G. Lee, A. Khademhosseini
Sponsorship: NIH

Regenerative medicine and tissue engineering are potentially important technologies in creating transplantable tissues for health and medical care. In particular, bone and cartilage regeneration by using embryonic stem cells (ESCs) is an area of great interest for improving the quality of life.

Recently, physical stimuli such as compression, shear stress, strain, stretch, and hydraulic force have been shown to play important roles in the chondrogenesis and osteogenesis of stem cells [1]. Mechanical stimuli enhance the differentiation of stem cells and improve the mechanical properties of tissue. It is important to understand how cells respond to variations in mechanical forces. Since mechanotransduction mechanisms are still not well understood, there is a great demand for developing new technology that enables precise control of the cellular microenvironment.

Here we present a micro cell chip integrated with various sizes of microwells for the study of effects of mechanical stimulation on the fate of mouse embryonic stem cells (mESCs). This cell chip is designed not only to culture mESCs loaded into variously sized microwells (diameters: 150-, 200-, 300-, 400-, 500-µm), but also to apply dynamic compressive stimulation for chondrogenesis and osteogenesis of mESCs. This device is based on the pneumatic actuator with a flexible diaphragm. It consists of one air chamber, twelve cell chambers, and a microvalve system; it is fabricated by multi-layer soft lithography (Figure 1). Specifically, it consists of seven layers of RTV615 material and laser-machined poly(methyl methacrylate) (PMMA) substrates. The device is initially filled with a solution containing mESCs and embryoid body (EB) culture medium by a syringe pump. After confirmation of the cell aggregation in each microwell (Figure 2), mESCs are exposed to cyclic compressive stimulus (frequency 1 Hz, pressure 5 kPa) for 10 minutes every 12 hours for 7 days. During the mechanical stimulation, the inlet and outlet of each cell chamber is closed by an integrated microvalve system to prevent an undesired shear stress on the cell chamber.

To evaluate the differentiation of mESCs under mechanical stimuli, we are currently conducting cell viability tests and immunocytochemistry on chondrogenesis and osteogenesis. This micro cell chip may provide a convenient and effective tool for directing the differentiation of ESCs into bone or cartilage.

REFERENCES

[1] W. Y. Sim, S. W. Park, S. H. Park, B. H. Min, S. R. Park, and S. S. Yang, „A pneumatic micro cell chip for the differentiation of human mesenchymal stem cells under mechanical stimulation," *Lab Chip*, vol. 12, pp. 1775-1782, 2007.

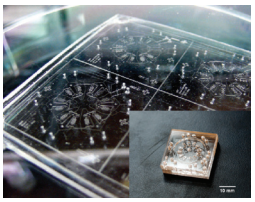


FIGURE 1: Photograph of a micro cell chip integrated with various sizes of microwells and microvalve system for the study of mechanical stimulation effect on the mESC fate. Three RTV 615 layers (microwells + microfluidic chambers and channels + microvalve). (Inset) Photograph of the fabricated device after oxygen plasma bonding with RTV 615 and PMMA layers. Scale bar is 10 mm.

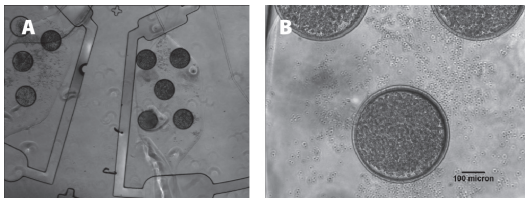


FIGURE 2: Phase contrast images of the EB formation after cell loading in 300 mm-diameter microwells. (A) Microvalve is located on the inlet and outlet of cell chambers. (B) Closed-up image of a microwells. Scale bar is 100 mm.

Measurement of Mass, Density, and Volume of Yeast through the Cell Cycle

A. K. Bryan, A. Goranov, A. Amon, S. R. Manalis
Sponsorship: NIH

Differences in cell density (mass per unit volume) have traditionally been used for cell synchronization and purification, but advances in density measurements may be used to investigate how cell size, both mass and volume, are regulated during cell growth and division [1]. As shown in Figures 1 and 2, we have validated two methods for measuring cell density and observing density changes in real time. In the first method, cell density is measured by combining single-cell mass and volume data from the suspended microchannel resonator (SMR) and Coulter counter to calculate cell density. The second method measures density changes in living cells by comparing cell density to fluid density as each cell transits the resonator. We used these techniques in Saccharomyces cerevisiae to identify an energy-dependent G1/S density change that requires START, TOR complex 1 function, and actin dynamics. In conjunction with these density measurements, FACS and bud emergence data suggest that bud formation may be required for this density shift. These density measurement techniques are applicable to most non-adherent cells and subcellular particles, and they offer cell-friendly and time-resolvable methods that extend beyond cell- cycle studies.

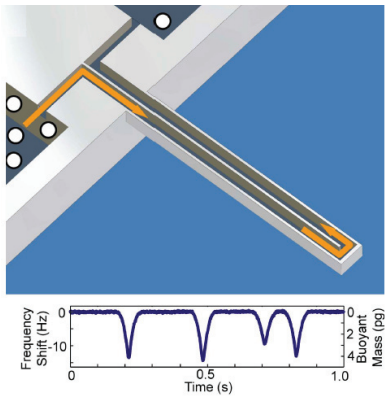


FIGURE 1: Illustration of instrument and cell measurement. Cells flowing through the cantilever displace a volume of fluid equal to their own volume and change the cantilever's resonant frequency proportional to this change in cantilever mass. The flow rates are controlled by pressure. The frequency shift as cells' flow through the microchannel is dependent on the position of the cell along the cantilever and the buoyant mass of the cell. The absolute maximum frequency shift for a cell (four of which are shown) occurs at the cantilever tip and this is proportional to the cell's buoyant mass. The system returns to a stable baseline upon each cell's exit from the microchannel.

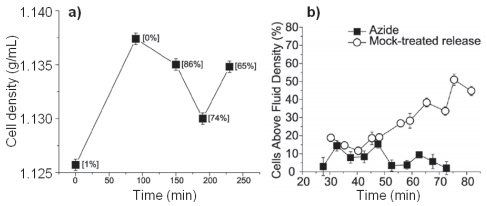


FIGURE 2: a) Density of formaldehyde-fixed cell populations synchronized by centrifugal elutriation. Bud counts are reported as percent budded in brackets next to each measurement. Cells begin to enter S-phase between 60 and 120 min. Error bars are the standard deviation for the technique as measured with NIST particle standards. b) Real-time single-cell relative density measurement. Cell state, distinguished by cell density, is determined by the direction of frequency shift. For a fluid density near that of the cells, G1 cells have a negative buoyant mass (positive frequency shift), and cells entering S-phase at a later timepoint have a positive buoyant mass (negative frequency shift). The proportion of cells in each state is directly correlated to the percent of cells below or above fluid density, and the change of cell state was recorded as it occurred for samples released from a G1 arrest.

REFERENCE

[1] A. K. Bryan, A. Goranov, A. Amon, S. R. Manalis, "Measurement of mass, density, and volume of yeast through the cell cycle," *PNAS,* in review.

Microscale Continuous Cell Culture

K. S. Lee, R. J. Ram
Sponsorship: NSF

For systems biology, the models are more often limited by the absence of experimental data than by available computational resources. Unfortunately, there is still great difficulty in making the leap from genetic and biochemical analysis to accurate verification with conventional culture growth experiments due to variations in culture conditions. Measurements of metabolic activity through substrate and product interactions or cellular activity through fluorescent interactions are generally highly dependent on environmental conditions and cellular metabolic states. For such experiments to be feasible, continuous cultures [1], [2] utilizing control strategies must be developed to measure relevant chemical concentrations, introduce chemical inputs, and remove waste. An integrated microreactor system with built-in input fluid metering for environmental control will enable controlled and programmed experiments capable of generating reproducible data.

The design of a microchemostat for providing environmental control is given in Figure 1. The chip is fabricated out of polycarbonate, utilizing PDMS membranes for actuation and pumping [1]. Mixing and oxygen delivery are performed through actuation of the membranes situated between the fluidic and actuation layers of the growth chamber sections. Initial growth results are shown in Figure 2. Culture experiments are performed with *E. coli* FB 21591 in 1 g/L glucose and 100 mM MES defined medium supplemented with 100 ug/ml kanamycin. Cell density is measured with an optical sensor set up to measure forward scattering through the growth chamber at 640 nm in a path length of 2 mm. The system is first run in batch culture to demonstrate cell viability within the reactor and then diluted and run in continuous mode with a dilution rate of 0.158 hr^{-1}. After continuous culture, the system is run in batch again to demonstrate cell viability and a reduced growth rate induced by continuous operation.

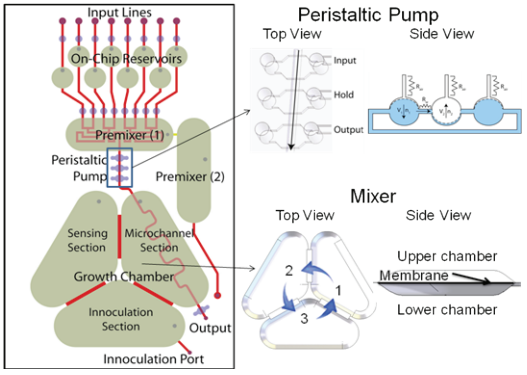


FIGURE 1: Schematic and picture of the microchemostat device. Eight inputs lines provide control over the chemical composition of the medium within the growth reservoir. Fluids are introduced through a peristaltic pump that injects liquid into the growth chamber. Fluids are first premixed in the premixer to reduce chemical gradients between the growth chamber and input fluids.

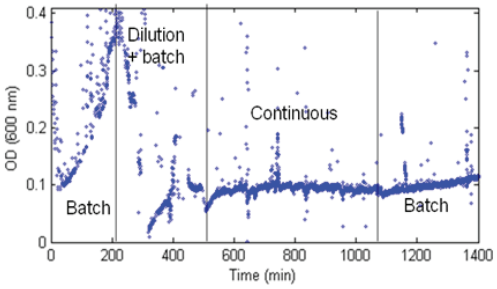


FIGURE 2: Plot of the cell density over time for a growth on a defined glucose medium. The chip is run in two modes; first batch growth, followed by continuous mode at a dilution rate of 0.158 hr^{-1}, and finally at batch growth again to demonstrate cell viability after continuous operation.

REFERENCES

[1] "La technique de culture continue, theorie et applications," J. Monod, Annales de l'Institut Pasteur (Paris), 79, 390-410 (1950).

[2] "Description of the chemostat," A. Novick, L. Szilard, Science, 112, 715-716 (1950).

[3] "Scaling properties of a low-actuation pressure microfluidic valve," V. Studer, G. Hang, A. Pandolfi, M. Ortiz, W. F. Anderson, S. R. Quake, J. Applied Physics, 95, 393-398 (2004).

MEMS & BioMEMS

Chip-Scale Quadrupole Mass Filters for a Micro Gas Analyzer

K. Cheung, L. F. Velasquez-Garcia, A. I. Akinwande
Sponsorship: DARPA

In recent years, there has been a desire to scale down linear quadrupoles. The key advantages of this miniaturization are the portability it enables and the reduction of pump-power needed due to the relaxation on operational pressure. Various attempts at making MEMS-based linear quadrupoles have met with varying degrees of success [1]-[3]. Producing these devices involved some combination of precision machining or microfabrication followed by electrode assembly. For miniature quadrupole mass filters to be mass-produced cheaply and efficiently, the electrode assembly should be removed from the process.

A chip-scaled quadrupole mass filter comprising a planar design and square electrodes was conceived, fabricated, and tested. Rectangular electrodes were utilized since this is the most amenable geometric shape for planar microfabrication. This deviation from the conventional round rod geometry required optimization and analysis, which was conducted with Maxwell 2D and MATLAB [4]. The fabrication process consists of thermal oxidation, the use of DRIE to define the features, and the fusion bonding of five patterned silicon wafers. This relatively simple process flow furthers the case for mass-production of these devices. A completed device measures 33 x 15 x 4 mm^3 and contains integrated ion optics as shown in Figure 1.

This non-conventional design introduces non-linear resonances that degrade the peak shape in the mass spectrum. Reported work with linear quadrupoles shows improved peak shape by operation in the second stability region [3]. Characterization of the device was conducted using FC-43, a standard calibration compound, and air as the analytes. The MuSE-QMF demonstrated a mass range of 250 amu using the first stability region and a minimum peak width of 0.7 amu in the second stability region. The main peaks for air (nitrogen, oxygen, argon, carbon dioxide) can be clearly distinguished in Figure 2.

In future work, we plan on modifying the processing and the mask layout to improve device performance. The design and fabrication concepts of this device can be expanded into arrayed configurations for parallel analysis and aligned quadrupoles operated in tandem for enhanced resolution.

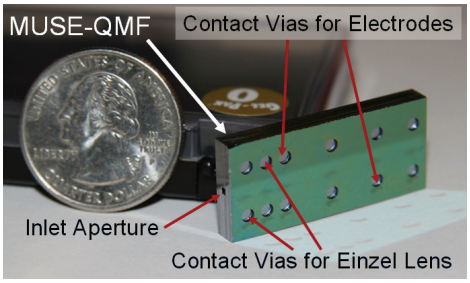


FIGURE 1: Fabricated micro-square electrode quadrupole mass filter (MuSE-QMF) next to a U.S. quarter.

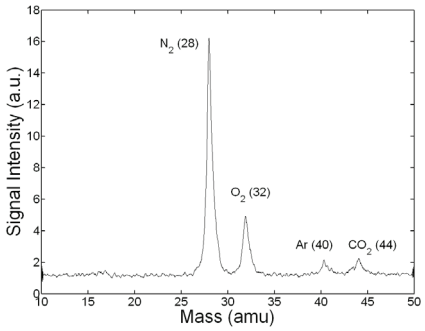


FIGURE 2: Mass spectrum for air using the MuSE-QMF driven in the second stability region at 2 MHz.

REFERENCES

[1] M. Geear, R.R.A. Syms, S. Wright, and A.S. Holmes, "Monolithic MEMS Quadrupole mass spectrometers by deep silicon etching," *Journal of Microelectromechanical Systems*, vol. 14, no. 5, pp. 1156-1166, Oct. 2005.

[2] J.J Tunstall, S. Taylor, R.R.A. Syms, T.Tate, and M.M. Ahmad, "Silicon micromachined mass filter for a low-power, low-cost quadrupole mass spectrometer," in *Proc. IEEE Eleventh Annual International Workshop on Micro Electro Mechanical Systems*, 1998, pp. 438-442.

[3] L.F. Velazquez-Garcia, K. Cheung, and A.I. Akinwande, "A versatile MEMS quadrupole platform for portable mass spectrometry using the first and second stability regions," *Journal of Microelectromechanical Systems*, vol. 17, no. 6, pp. 1430-1438, Dec. 2008.

[4] K. Cheung, L. F. Velásquez-García, A. I. Akinwande, "Fully Batch-Fabricated Linear Quadrupole Mass Filters", *Technical Digest of the 2008 IEEE Solid-State Sensors, Actuators, and Microsystems Workshop*, Hilton Head Island SC, USA, pp. 316-319

Tactile Sensors and Actuators for Smart Surface Applications

M. E. Swanwick, S. M-L Pfaendler, A. J. Flewitt, A. I. Akinwande
Sponsorship: Gates-Cambridge Trust, Nokia Research Center Cambridge UK

Novel tactile sensor and actuator devices using zinc oxide nanowires have been developed to enhance the interaction between people and their environment for smart surface applications. Both the sensor and actuator device use the piezoelectric effect of zinc oxide (ZnO) nanowires. The devices are based on a cross-bar network comprising a top and bottom array of electrodes around a composite of vertically grown nanowires and an insulating polymer. This cross-bar network allows for individually addressable locations for both sensing and actuation. The results for the tactile pressure sensor show a clear spike in current when an insulating tip is placed on and removed from the surface (Figure 1). This result is compared to controls including a touch on the adjacent cross electrodes and testing another device without wires. Both tests show at least an order of magnitude difference in current between the control and the pressure sensor.

The actuator device utilizes a thin membrane of thermally grown silicon dioxide that is oscillated at resonance to induce tactile sensation. The oxide membrane is fabricated by using a deep back-side etch of a silicon wafer and utilizing the thermally grown oxide as an etch stop. The rest of the device is very similar to the pressure sensor with an electrode cross bar network and a zinc oxide nanowire polymer composite. The nanowires are grown in a furnace by chemical vapour deposition or by a low temperature hydrothermal method, producing wires of length of 1–12μm [1], [2]. The system is actuated by applying an alternating current through the top and bottom electrodes. The piezoelectric nanowires expand and contract according to the AC signal [3]. The results show a first resonance peak at 139kHz, followed by a slightly lower peak at 191kHz. The amplitude of oscillation is still not known precisely, but it is estimated to be approximately 15nm at 33V.

Currently, haptic feedback for portable electronic devices such as mobile phones is limited to vibration over a large area or the whole phone [4], [5]. This project addresses these issues by making the tactile actuators and sensors smaller than the pixel size that the finger can sense. This small pixel size leads to virtual buttons and textured surfaces that are software-controlled and infinitely variable. The long term goal of the project is to have a transparent and flexible device so that it can be incorporated into a variety of different displays and surfaces.

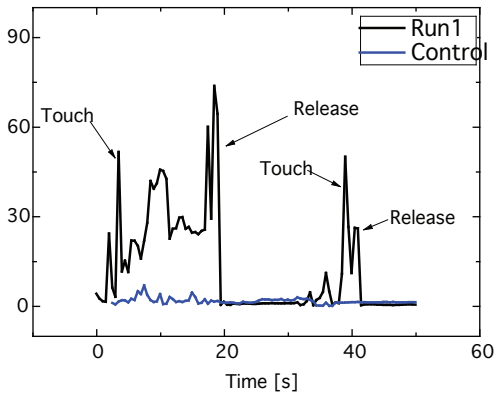


FIGURE 1: Tactile pressure sensor results compared with a control run. An insulated probe tip was manually pressed onto the device, as signified by the Touch and Release labels. For the control run, the tip was placed on an adjacent cross-bar and the tip was again manually placed and rubbed on the surface.

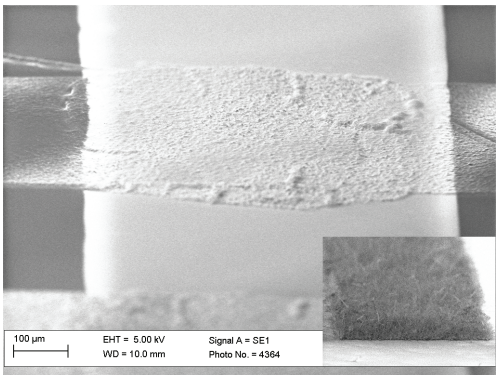


FIGURE 2: An SEM micrograph of the cross-bar activation device taken at a 70-degree angle. The device is a SiO_2 membrane with Nb electrodes and thermally grown vertical ZnO nanowires in a polymer composite. Insert in lower right: Thermally grown ZnO nanowires on Nb (the electrode is 100 µm wide for scale)

REFERENCES

[1] S.H. Dalal, "Zinc Oxide Nanowires and their Applications," Ph.D. thesis, University of Cambridge, Cambridge, UK, 2008.

[2] A. R. Rachamim; S. H. Dalal; M. E. Swanwick; A. J. Flewitt; W. I. Milne, " Quantitative Investigation of the Factors Affecting the Hydrothermal Growth of Zinc Oxide Nanowires," presented at *2009 MRS Spring Meeting*, San Franscisco, CA, April 2009.

[3] Z. L. Wang, "Novel Nanostructures of ZnO for Nanoscale Photonics, Optoelectronics, Piezoelectricity, and Sensing," *Appl. Phys. A*, vol. 88, pp 7 – 15, 2007.

[4] I. Pouprev, S. Maruyama, and J. Rekimoto, "Ambient Touch: Designing Tactile Interfaces for Handheld Devices," *Computer-Human Interactions (CHI2002)*, vol. 4, pp. 51 – 60, 2002.

[5] A. Nashel and S. Eazzaque, "Tactile Virtual Buttons for Mobile Devices," *Computer-Human Interactions (CHI2003): New Horizons, Short Talk: Haptic Interfaces*, pp. 854 – 855, April 2003.

MEMS-based Plasma Probes for Spacecraft Re-entry Monitoring

L. F. Velásquez-García, A. I. Akinwande
Sponsorship: NASA

NASA's strategic plan calls for a focus on advanced sensing that would assure continued safe operations. We propose a set of three cost-effective and reliable MEMS-based sensors to diagnose in real time the conditions of the plasma surrounding the spacecraft during reentry. The proposed sensors are (i) arrays of Langmuir probes, (ii) arrays of retarded potential analyzers, and (iii) arrays of GPS antennas. Each sensor is targeted to gather specific information of the plasma, and it is operated in such a way that allows fast data collection. There are reports of MEMS-based devices for plasma diagnostics such as Langmuir probes [1]. Although these sensors work, their shield is made of polyimide. Therefore, these sensors are not compatible with the high-temperature or high-density plasmas that the spacecraft encounters at re-entry. Silicon Carbide (SiC) is a semiconductor material that is very resistant to hostile environments [2]. There are current research efforts to develop SiC-based MEMS intended for harsh environments, including pressure, acceleration, temperature, and strain transducers, as well as transistors [3]-[5]. The SiC is a promising material to implement low-cost and reliable plasma diagnostics. We are exploring SiC both as a coating and as fabrication substrate. The work has focused on the Langmuir probe development. Langmuir probe densities as large as 10^6/cm^2 have been demonstrated (Figure 1). Also, fabrication experiments using a plasma-enhanced chemical vapor deposited (PECVD) SiC coatings have been conducted (Figure 2). Future research includes the development of an RPA based on an ionizer we recently developed [6] and experimental validation of the sensors.

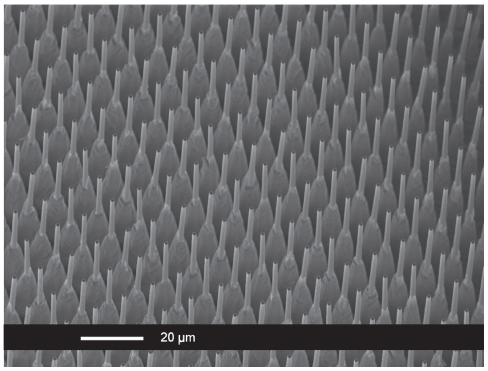


FIGURE 1: A set of high aspect-ratio Si columns (1 µm ×1 µm × 100 µm) coated with a protective SiO_2 film. The tips of the columns can be used as Langmuir probes to sample the plasma every 10 µm.

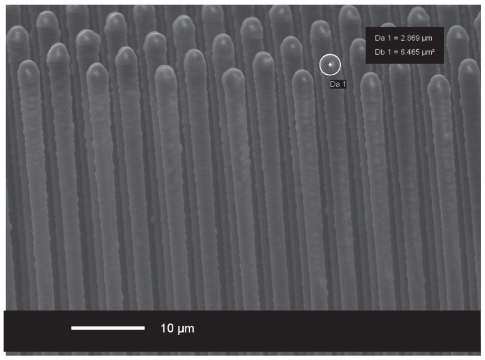


FIGURE 2: A set of high-aspect-ratio Si columns coated with a PECVD SiC film.

REFERENCES

[1] J. A. Stillman, F. C. Chiang, P. A. Pribyl, M. Nakamoto, W. Gekelman, and J. W. Judy, "Microfabricated Probes for Laboratory Plasmas", in *Proceedings Solid-State Sensors, Actuators, and Microsystems Workshop*, Hilton Head Island SC, pp 308 – 311, 2006.

[2] M. Wijesundara, G. Valente, W. Ashurst, R. Howe, A. Pisano, C. Carraro, and R. Maboudian, "Single-Source Chemical Vapor Deposition of 3C-SiC Films in a LPCVD Reactor I. Growth, Structure, and Chemical Characterization", *Journal of the Electrochemical Society*, Vol. 151, n. 3, pp. C210-C214, 2004.

[3] R. S. Okojie, G. M. Beheim, G. J.Saad, and E. Savrun, "Characteristics of Hermetic 6H-SiC Pressure Sensor at 600 C, in *Proceedings of the AIAA Space 2001 Conference and Exposition*, Albuquerque, NM, August 28-30, 2001 (AIAA Paper No. 2001-4652).

[4] R. S. Okojie, D. Lukco, Y. L. Chen, and D. J. Spry, "Reliability Assessment of Ti/TaSi2/Pt Ohmic Contacts on SiC After 1000 h at 600 C," *Journal of Applied Physics*, Vol. 91, no. 10, pp. 6553-9559, 2002.

[5] A. Pisano (PI), HERMIT Program at U. C. Berkeley, DARPA MTO PI Meeting, Long Beach CA, July 2007.

[6] L. F. Velásquez-García, B. Gassend, and A. I. Akinwande, "CNT-Based Gas Ionizers with Integrated MEMS Gate for Portable Mass Spectrometry Applications", to be presented at *the 15th International Conference on Solid-State Sensors, Actuators and Microsystems*, Denver, CO, USA, June 21 – 25, 2009.

Investigating Stem Cell Dynamics Utilizing Microfluidic-based Time-lapse Imaging

G. H. Underhill, D. R. Albrecht, J. Resnikoff, S. N. Bhatia, J. V. Shah

An understanding of the mechanisms underlying stem cell fate and function has recently been augmented by the application of microfabricated systems, designed to systematically probe important environmental stimuli and intrinsic genetic programs [1]. In particular, current approaches leveraging these systems aim to enhance both the spatial and temporal resolution of stem cell analysis, providing a more complete picture of dynamic stem cell processes. Microfluidics represents a promising technology for the parallel analysis of cellular responses to numerous perturbations simultaneously within a single device [2], although it can be difficult to implement in traditional biology laboratory settings. To examine the dynamics of embryonic stem (ES) cell self-renewal and differentiation, we have employed a simple microfluidics platform, without valves or specialized equipment, coupled with near-simultaneous time-lapse imaging. This integrated system incorporates a miniaturized 96-well, ~6 x 4 mm^2 imaging area with a variable input/output channel design and enables the interrogation of ES cell kinetics within multiple environments. We have tested the platform with both feeder-independent mouse ES cell lines as well as co-cultures of mouse ES cells with supportive mouse embryonic fibroblast (MEF) feeder layers and demonstrated self-renewal over 3-4 days of analysis. The examination of ES cells containing fluorescent protein fusions was utilized to monitor chromosome dynamics during self-renewal and to evaluate proliferation kinetics; furthermore, perturbation with an anti-mitotic agent demonstrated the dynamic response to exogenous factors within the device. Overall, these studies illustrate the capacity to dynamically assess and manipulate stem cell processes through the integration of a simple, but modular, microfluidics-based imaging platform.

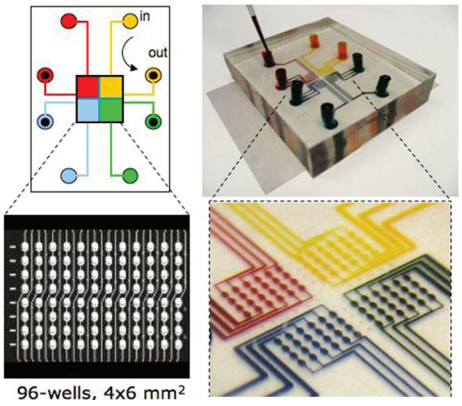


FIGURE 1: Microfluidic device for imaging mES dynamics. The design and scheme for four independent experiments is illustrated.

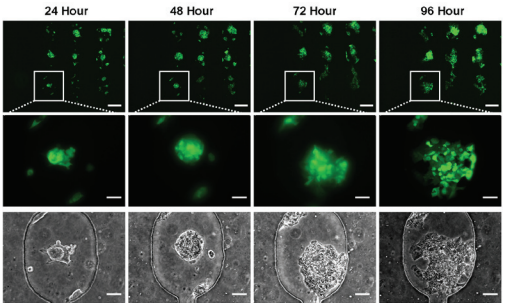


FIGURE 2: The Oct4-EGFP mES cells cultured on gelatin-coated glass coverslips and imaged at 24-hr time points. The top series illustrates a field imaged at 4X magnification, containing multiple microwells. The bottom series of paired fluorescent and phase contrast images represents the indicated single well imaged at 20X magnification. Scale bars: 200 mm (top), 50 mm (bottom paired).

REFERENCES

[1] G.H. Underhill and S. N. Bhatia, "High-throughput analysis of signals regulating stem cell fate and function," *Curr Opin Chem Biol*, vol. 11, no. 4, pp. 357-366, Aug. 2007.

[2] J. Melin and S. R. Quake, "Microfluidic large-scale integration: the evolution of design rules for biological automation," *Annu Rev Biophys Biomol Struct*, vol. 36, pp. 213-231, June 2007.

Direct Patterning of Metallic MEMS through Microcontact Printing

C. E. Packard, A. Murarka, V. Bulović
Sponsorship: DARPA, Hewlett-Packard

Standard photolithography-based methods for fabricating microelectromechanical systems (MEMS) present several drawbacks including expense, incompatibility with flexible substrates, and limitations to wafer-sized device arrays. We have developed a new fabrication method for rapid fabrication of large-area MEMS that breaks the paradigm of lithographic processing using a scalable, large area microcontact printing method to define three-dimensional electromechanical structures. Our PDMS Lift-Off Transfer (PLOT) involves the rapid removal of a pick-up stamp from a transfer pad to transfer a continuous metal film from the pad to the stamp. A stamp that forms the membrane suspension supports is fabricated by molding a thin layer of PDMS against a silicon master with a predefined relief. The metal membranes are deposited by thermal evaporation onto a transfer pad which has been prepared with an organic molecular release layer. To achieve transfer of the metal membrane over the supports of the device, the stamp is brought into conformal contact with the transfer pad and then released by rapidly peeling away. MEMS bridge structures, such as the ones shown in Figure 1, have been fabricated using PLOT, and their performance as variable capacitors has been characterized. In Figure 2, the capacitance of these devices increases with applied voltage, indicating mechanical deflection of the bridges due to the electrostatic force. PLOT forms MEMS structures without requiring elevated temperature processing, high pressure, or wet chemical or aggressive plasma release etches, providing compatibility with sensitive material sets for the fabrication of integrated micro- or opto-electronic/MEMS circuits. Flexible, paper-thin device arrays produced by this method may enable such applications as pressure sensing skins for aerodynamics, phased array detectors for acoustic imaging, and novel adaptive-texture display applications.

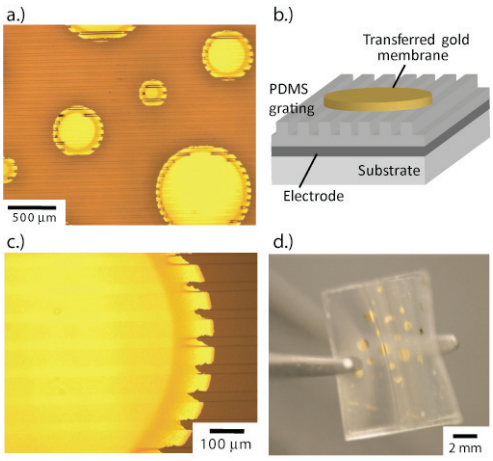


FIGURE 1: Devices formed by PLOT: optical micrographs (a. & c.), schematic (b.) and photograph of devices formed on a flexible substrate (d.)

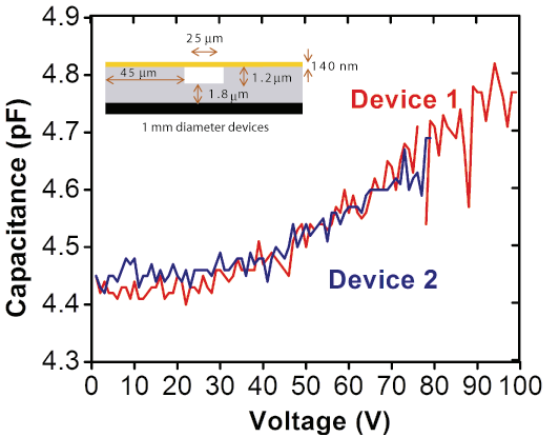


FIGURE 2: Capacitance increases with applied voltage in two devices, indicating mechanical deflection of the bridging metal film.

Design of Micro-scale Multi-axis Force Sensors for Precision Applications

M. A. Cullinan, R. M. Panas, M. L. Culpepper
Sponsorship: DoD

Multi-axis force-sensing at the micro-scale is necessary for a wide range of applications in biology, materials science, and nanomanufacturing. A three-degree-of-freedom force sensor (Figure 1) was designed that is capable of accurately and precisely measuring the adhesion forces (nanoNewtons) between biologically active surfaces. This force sensor is positioned and actuated using a Hexflex nanopositioner and Lorenz force actuators as seen in Figure 2.

In order to design high-accuracy, high-precision, multi-axis MEMS force sensors, a closed form model was developed to optimize the strain sensitivity of the MEMS force sensor. This model first sets constraints on the system due to package size, fabrication techniques, desired degrees of freedom, and force range. The layout of the flexure system is optimized to meet the kinematic and manufacturing constraints of the MEMS force sensor. The geometry of the flexures is set to maximize the strain at the sensor locations.

This model was incorporated into a thermal/electric model to fully characterize all of the inputs to the system. The resolution of the force sensor is a function of the noise from the strain sensors, the noise in the electronics, the thermomechanical noise, and the sensitivity of the strain sensors to a force input. Based on this model, the dominant noise sources are identified and the sensor system is optimized to reduce these noise sources. The thermal/electric model is also used to determine the major factors limiting the accuracy of the force sensor. In most cases, the drifts in both the electronics and sensors caused by fluctuations in room temperature were the major sources of accuracy errors. Therefore, an environmental enclosure with closed-loop control over temperature was designed and implemented. Overall, the final design of the force sensor is capable of producing sub-nanoNewton-resolution force measurements with nanoNewton-level accuracy.

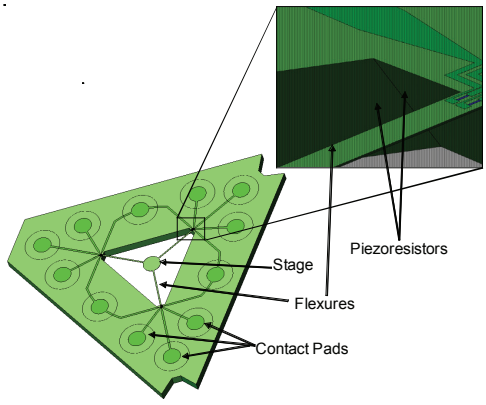


FIGURE 1: A 3-axis force sensor with polysilicon strain gauges on the flexure beams.

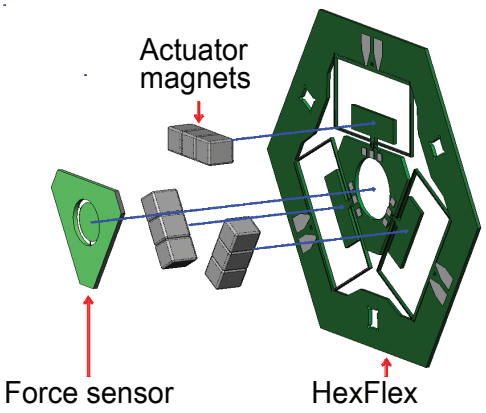


FIGURE 2: Schematic of how the force sensor actuator magnets fit on the Hexflex nanopositioner.

Design of a Six Degree of Freedom Nanopositioner for Use in Massively Parallel Probe-based Nanomanufacturing

C. M. DiBiasio, M. L. Culpepper

Sponsorship: NSF via OSU NSEC

In probe-based nanomanufacturing a micro-scale probe tip is used to create or measure nm-scale features. The serial nature of probe-based manufacturing dictates that practical throughput rates will require the use of two-dimensional tip arrays. These arrays must be controlled in six degrees-of-freedom to maintain parallelism with respect to the work surface. Meso-scale, 6-axis nanopositioners [1] will be needed because they (1) are lower cost ($100s US versus $10,000s), (2) possess higher bandwidth, and (3) are more thermally stable than macro-scale nanopositioners. Furthermore, their small size enables arraying many nanopositioners in a small footprint. Sensing is important as this enables closed loop position control and therefore control in a nanomanufacturing process. We have designed and microfabricated low-cost nanopositioners with nm-level accuracy and resolution that are equipped for closed-loop operation throughout a 50x50x50 μm3 work volume. Figure 1 shows the nanopositioner (less actuators [2] and electronics) that contains an integrated 6-axis piezoresistive sensing system [3]. The figure inset shows the piezoresistor arrangement, wherein a first sensor is placed along the beam's neutral axis and the second sensor is placed at the beam's edge. Both sensors are placed near the root of the cantilever where maximum device strain occurs. The neutral axis sensor experiences strain primarily from out-of-plane bending while the sensor on the edge of the beam experiences strain from in- and out-of-plane bending. Biasing these signals makes it possible to obtain in-plane and out-of-plane measurements from the sensors while keeping them located on the same face of the flexible beam. The structure of the nanopositioner was microfabricated from a 400 μm thick silicon wafer with 500 nm polysilicon piezoresistors fabricated onto the flexural beams. Each nanopositioner costs approximately $250 US and initial tests indicate the nanopositioner will have 2 nm out-of-plane resolution and 20 nm in-plane resolution.

REFERENCES

[1] M.L. Culpepper and G. Anderson, "Design of a Low-cost Nano-manipulator Which Utilizes a Monolithic, Spatial Compliant Mechanism," *Precision Engineering*, vol. 28, pp. 469-482, Aug. 2004.

[2] D. Golda and M.L. Culpepper, "Two-axis Electromagnetic Moving-Coil Micro-Actuator," in *Proc. of the 2006 ASME International Mechanical Congress and Exposition*, 2006.

[3] C.M. DiBiasio and M.L. Culpepper, "Design of a Meso-scale Six-axis Nanopositioner with Integrated Position Sensing," in *Proc. Fifth Annual International Symposium on Nanomanufacturing*, 2008.

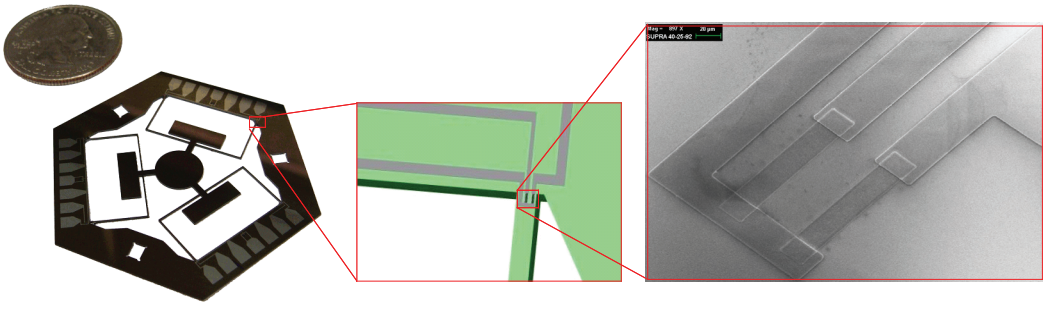


FIGURE 1: Microfabricated six-axis nanopositioner with integrated piezoresistive sensing. The inset shows the arrangement of the piezoresistors on the flexural beams.

Magnetically-assisted Assembly, Alignment, and Orientation of Micro-scale Components

J. Diaz, D. Cheng, C. G. Fonstad, Jr. in collaboration with F. Cadieu, Queens College of CUNY, M. Zahn, MIT
Sponsorship: Vitesse Chair

The use of magnetic forces to improve fluidic self-assembly of micro-components has been investigated using Maxwell 3D to model the forces between Ni thin films on semiconductor device micro-pills and Sm-Co thin films patterned on target substrates [1]. Orienting and restraining forces on pills far in excess of gravity are predicted, and it is found that the fall-off of these forces with pill-to-substrate separation can be engineered through the proper design of the Sm-Co patterns to retain only properly oriented pills [1], [2].

Micro-scale hybrid assembly is a potentially important way of doing heterogeneous integration, i.e., of integrating new materials on silicon integrated circuits to obtain functionality not readily available from silicon device structures alone, and fluidic self-assembly is an attractive way to automate micro-scale assembly. A serious limitation of fluidic self-assembly, however, is the lack of a good method for holding properly assembled components in place and accurately positioned until all of the components have been assembled and they have been permanently bonded in place. We have shown, based on our modeling, that suitably patterned magnetic films can be used to provide the forces necessary to retain, and to accurately orient and position, assembled micro-components.

Our motivation for pursuing micro-scale hybrid assembly is our general interest in doing optoelectronic integration, specifically of vertical cavity surface emitting lasers (VCSELS), edge-emitting lasers (EELs), and light emitting diodes (LEDs), with state-of-the-art, commercially processed Si-CMOS integrated circuits. Our ongoing research integrating these devices on silicon described elsewhere in this report provides the context for this work and illustrates the types of applications we envision for magnetically assisted self-assembly using the results of this study.

Assembly experiments to verify and demonstrate the theoretical predictions are currently in progress using two sizes of 6-μm-thick pills (50 μm by 50 μm and 50 μm by 100 μm) and a variety of magnetic thin film patterns. Recesses with different dimensions are also being studied [2].

REFERENCES

[1] D. Cheng, "Theoretical and Experimental Study of Magnetically Assisted Fluidic Self Assembly," MEng. Thesis, Department of Electrical Engineering and Computer Science, MIT, June 2008.

[2] D. Cheng, J. J. Rumpler, J. M. Perkins, M. Zahn, C.G. Fonstad, E. S. Cramer, R. W. Zuneska, and F. J. Cadieu, "Use of Patterned Magnetic Films to Retain and Orient Micro-Components during Fluidic Assembly," *Journal of Applied Physics*, Vol. 105, 07C123, 2009.

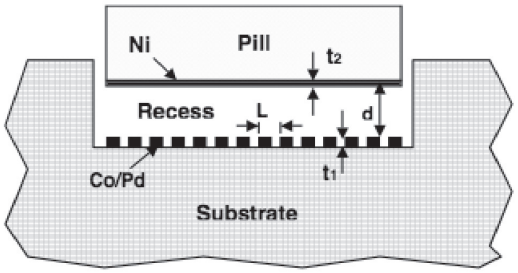


FIGURE 1: A cross-sectional cartoon illustrating the application of magnetically assisted assembly to recess integration. The variables indicated in the drawing correspond to the model used to calculate the magnetic force intensity.

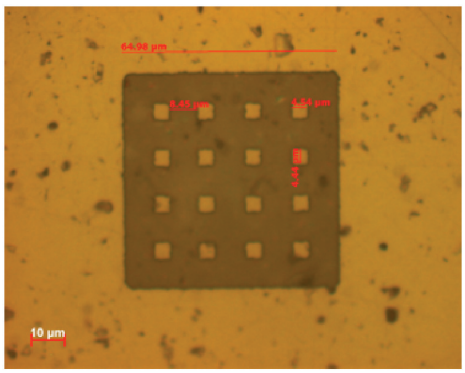


FIGURE 2: A microphotograph of a patterned samarium cobalt magnetic thin film. The abilities first to sputter-deposit and second to wet-etch thin films like this is critical to the successful implementation of magnetic self-assembly and are unique strengths of the MIT/Queens College effort.

Microfabricated Slits in Series: A Simple Platform to Probe Differences in Cell Deformability

H. Bow, P. Abgrall, J. Han

Sponsorship: Singapore-MIT Alliance, flagship research project "Design-Simulate-Fabricate Micro/Nano-fluidics for Cell and Biomolecule Manipulation"

Change in cell stiffness is a characteristic of blood cell diseases such as sickle cell anemia, malaria[1], and leukemia[2]. Often, increases in blood cell stiffness lead to loss of the cells' ability to squeeze through capillaries, resulting in organ failure, coma, and ultimately death. The spleen is the organ in the human body that is responsible for removing these less deformable cells. It functions by forcing cells in blood to squeeze between endothelial cells arranged like the staves of a wooden barrel.

The goal of this project is to create a microfluidic device that can quickly and accurately screen, diagnose, and treat disorders involving cell deformability. We report the creation of a microfabricated device consisting of a series of 1-2 μm-wide polymeric slits, modeled on those of the spleen, Figure 1. Using this device, we demonstrate unambiguous mobility differences between cells differing solely in stiffness.

Figure 2 shows mobility differences for red blood cells (RBCs) treated with different concentrations of GA in a 2-μm slit device. The GA acts as an amine-crosslinker, making the cell membrane and cytosol stiffer. The RBCs are slightly larger than this slit size and must deform to traverse the slit. Velocities of 0.001% GA-treated cells were within experimental error to untreated cells. The cells treated with 0.01% GA exhibited a velocity of 0 μm/s, as they were too rigid to pass through the slits. At a concentration of 0.003 %, the cells were semi-rigid and showed decreased mobility compared to the untreated cells. Cell size was observed to be the same throughout the range of GA concentrations.

These results demonstrate that increased membrane stiffness can cause statistically significant mobility differences through a series of slits. Additionally, the low-cost aspect of this device makes it ideal for on-site disease (e.g., malaria) screening in resource-poor settings.

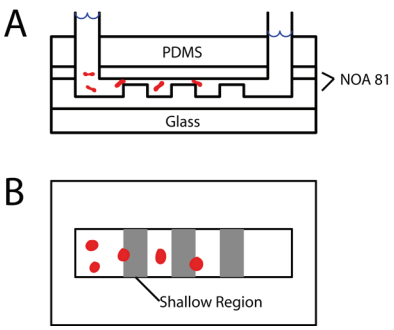


FIGURE 1: A. Side view. The smallest RBC dimension is greater than the height of the slits. Therefore, RBCs must deform to get through. B. Top view.

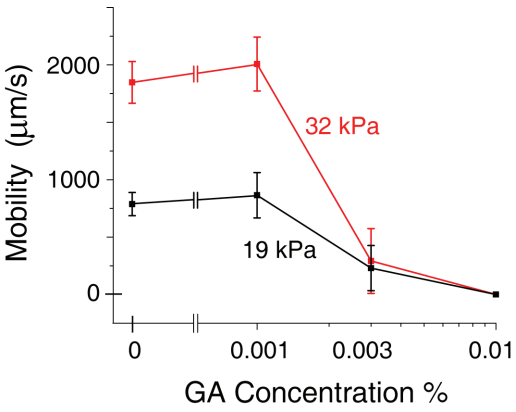


FIGURE 2: Mobility vs. GA concentration. Higher GA concentration increases cell stiffness, resulting in decreased mobility.

REFERENCES

[1] J. P. Shelby, J. White, K. Ganesan, P. K. Rathod and D. T. Chiu, "A microfluidic model for single-cell capillary obstruction by Plasmodium falciparum-infected erythrocytes," *Proc. Natl. Acad. Sci. U. S. A.*, vol. 100, pp. 14618-14622, December 9, 2003.

[2] M. J. Rosenbluth, W. A. Lam and D. A. Fletcher, "Force Microscopy of Nonadherent Cells: A Comparison of Leukemia Cell Deformability," *Biophysical Journal*, vol. 90, pp. 2994-3003, 2006.

Microfabricated Devices for Portable Power Generation

C. H. Marton, K. Deshpande, M. A. Schmidt, K. F. Jensen
Sponsorship: Lincoln Laboratory, ARO

The development of portable power-generation systems remains an important goal, with applications ranging from the automobile industry to the portable electronics industry. The focus of this work is to develop microreaction technology that converts the chemical energy stored in fuels–such as light hydrocarbons and their alcohols—directly into electricity or into a different energy vector such as hydrogen. Developing devices with high energy-conversion efficiency requires addressing difficulties in high temperature operation: specifically, thermal management, material integration, and improved packaging techniques.

A catalytic combustion-based device intended for the direct conversion of thermal energy to electricity has been developed. The combustor has been designed to achieve attractive energy and power densities while addressing system challenges such as mechanically robust fluidic connections and minimal parasitic power losses related to pressurization of air. The channels of the combustor are etched using wet potassium hydroxide, which is the most economical etch technique available. Straight channels (1mm by 1mm in cross-section) are arranged in parallel and separated by 100-μm–thick silicon walls, in order to achieve low pressure drop (< 300 Pa at 10 SLPM gas flow) with significant surface area (~1 cm^2 per channel) for catalyst deposition. Two identical reactors are stacked using metal thermocompression bonding to increase reactor volume without a significant increase in exposed surface area. External gas distribution manifolds are compression-sealed to the reactor, eliminating the need for glass brazing of tubes, increasing the mechanical robustness of the device, and avoiding large pressure losses associated with flow constrictions. Platinum-on-alumina catalyst has been washcoated on the channel surfaces for the catalytic combustion of butane with air.

A combined reforming/separation device has been developed and demonstrated. The hydrogen generation unit combines a 200-nm-thick palladium-silver film with a methanol reforming catalyst (supported palladium). The catalytic combustion unit employs a supported platinum catalyst. Both units are formed in a silicon wafer by bulk silicon micromachining techniques. The energy generated in the combustion unit is efficiently transferred to the hydrogen production unit by the thermal conduction of silicon support. The system has been demonstrated to purify hydrogen at elevated pressures (up to 2 atm). Joint combustion/purification of the system has also been demonstrated, in which combustion and reforming occur simultaneously with the purification of the resulting hydrogen.

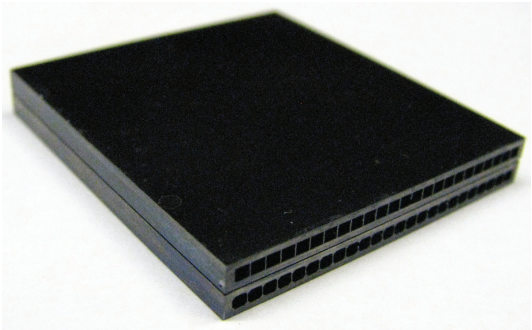


FIGURE 1: Catalytic combustion device prior to connection to the gas distribution manifold. Each of the 48 channels is 1 mm by 1 mm by 31 mm, and is separated by a 100-µm–thick wall.

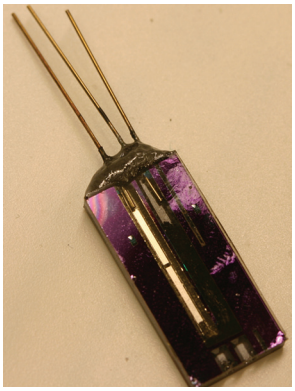


FIGURE 2: Combined reformer/separator device. The three fluidic connections are for reactant gases, combusted gases, and purified hydrogen.

Microfluidic Systems for Continuous Crystallization

M. Sultana, K. F. Jensen
Sponsorship: Lucent Technologies Fellowship, NSF

Microfluidic systems offer a unique toolset for discovering new crystal polymorphs and for studying the growth kinetics of crystal systems because of well-defined laminar flow profiles and online optical access for measurements. Traditionally, crystallization has been achieved in batch processes that suffer from non-uniform process conditions across the reactors and chaotic, poorly controlled mixing of the reactants, resulting in polydisperse crystal size distributions (CSD) and impure polymorphs. Consequently, batch crystallization suffers from reproducibility issues, increases difficulty in obtaining accurate kinetics data, and manufactures products with inhomogeneous properties. The small length scale in microfluidic devices allows for better control over the process parameters, such as the temperature and the contact mode of the reactants, creating uniform process conditions across the reactor channel. Thus, these devices have the potential to generate more accurate kinetics data and produce crystals with a controlled morphology and a more uniform size distribution. In addition, microfluidic systems decrease waste, provide safety advantages, and require only minute amounts of reactants, which is most important when dealing with expensive materials such as pharmaceutical drugs.

Figure 1 shows a microfluidic device used for crystallization; Figure 2 shows optical images of different polymorphs of glycine crystals grown inside reactor channels. A key issue for achieving continuous crystallization in microsystems is to eliminate heterogeneous crystallization–irregular and uncontrolled formation and growth of crystals at the channel surface–and aggregation of crystals, which ultimately clogs the reactor channel. We have developed a microcrystallizer using soft lithography techniques that introduce the reagents to the reactor channel in a controlled manner, preventing heterogeneous crystallization and aggregation. We have used optical microscopy *in situ* to obtain high-resolution images of crystals grown in continuous microreactors and use image analysis to derive growth kinetics of crystals of different morphologies and shapes. In addition, we have integrated an online spectroscopy tool for *in situ* polymorph detection. In summary, we have developed a microfluidic system for continuous crystallization of small organic molecules and integrated it with *in situ* detection tools for size and morphology characterization.

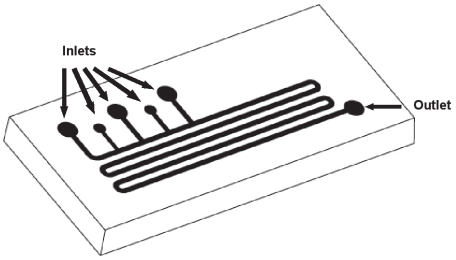


FIGURE 1: The microfluidic device used for crystallization.

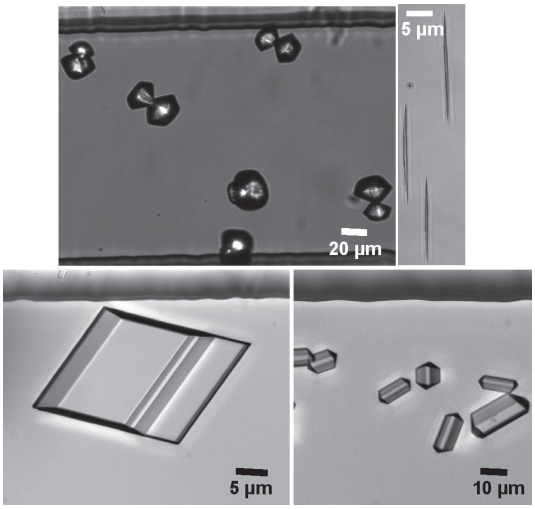


FIGURE 2: Different sizes and shapes of glycine crystals produced in the reactor channel.

Multistep Microfluidic Systems for Synthetic Chemistry

R. L. Hartman, N. Zaborenko, H. R. Sahoo, B. C. Yen, K. F. Jensen
Sponsorship: Novartis-MIT Center for Continuous Manufacturing

Microchemical systems have recently gained prominence for use in reaction screening and augmentation. However, most chemical syntheses combine several reaction and work-up steps, and independently studying each step limits understanding of how they are coupled in a process. To that end, microfluidic systems have been integrated to realize multistep reaction and liquid-liquid extraction steps [1], [2]. However, other separation techniques are needed in traditional batch synthetic transformations such as filtration, evaporation, and distillation. Consequently, developing a fundamental understanding of microfluidic distillation has been undertaken.

Distillation is a ubiquitous method of separating liquid mixtures based on differences in volatility. This unit operation is fundamental to a number of industrial processes, and performing such separations in microfluidic systems is difficult because interfacial forces dominate over gravitational forces. The concept of distillation has been engineered on a silicon-based microfluidic chip as shown by the device shown in Figure 1 [3]. Microfluidic distillation is realized by establishing vapor-liquid equilibrium during segmented flow. Enriched vapor in equilibrium with liquid is then separated using capillary forces, thus enabling a single-stage distillation operation. As shown in Figure 2, separation of binary liquid mixtures (e.g., methanol (MeOH) and toluene) is made possible by carrying out microfluidic distillation. These experimental results were consistent with phase equilibrium predictions.

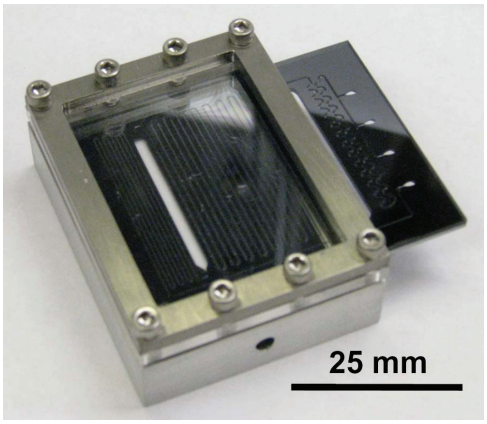


FIGURE 1: Fabricated distillation device with an on-chip condenser and integrated vapor-liquid membrane separator. The photograph shows a device packaged in an aluminum compression chuck for precise temperature control. [3]

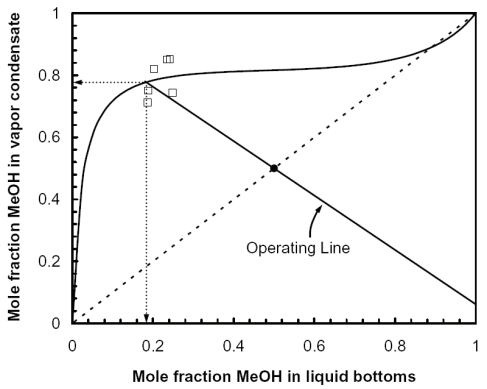


FIGURE 2: McCabe-Thiele diagram for distillation of 50:50 mol% MeOH-toluene at 70.0°C using the device shown in Figure 1. The curved line represents the phase-equilibrium of MeOH-toluene while the black squares denote multiple repeats of the single-stage enrichment. The solid straight line (i.e., operating line) represents equation (16) whereas the dashed line is y = x. [3]

REFERENCES

[1] H. R. Sahoo, J. G. Kralj, and K. F. Jensen, "Multistep continuous-flow microchemical synthesis involving multiple reactions and separations," *Angew. Chem.-Int. Edit.*, vol. 46, pp. 5704-5708, 2007.

[2] J.G. Kralj, H.R. Sahoo, and K.F. Jensen, "Integrated continuous microfluidic liquid-liquid extraction," *Lab on a Chip*, vol. 7, pp. 256-263, 2007.

[3] R.L. Hartman, H.R. Sahoo, B.C. Yen, and K.F. Jensen, "Distillation in microchemical systems using capillary forces and segmented flow," *Lab on a Chip*, 2009, DOI: 10.1039/b901790a.

Direct Printing of PZT Thin Films for MEMS

S. Bathurst, H .W. Lee, S. G. Kim
Sponsorship: DARPA Grant HR0011-06-1-0045, Hewlett-Packard

In 2008-2009, we continued our work on thermal ink-jet printing of PZT [1], further optimizing the deposition process and thermal post-processing. Early work showed that modified sol-gel inks often have reduced performance due to porosity, pin holes, and void formation. Multi-layer deposition was investigated as a means to seal voids. Multiple ferroelectric capacitors were fabricated, all with approximately 400nm of printed PZT. Multi-layer films showed consistently improved dielectric properties over single-layer films, with less leakage current and higher resistivity. The continued refinement of the thermal processing profile developed in 2007-2008 lead to a 3hr pyrolysis at 400C followed by a 650C anneal in an O_2 environment. These small adjustments improved organic removal, increased film densification, and provided improved piezoelectric response (Figure 2). The remanent polarization of each capacitor was measured as metric for piezoelectric performance. Finally, printing of devices with different thicknesses on a single wafer was demonstrated, something that cannot be accomplished with conventional coating techniques. Future work includes further development of a thermal treatment for multi-layer films. The samples in figure 2 were annealed between each layer, potentially affecting the alignment of the ferroelectric domains between layers. Work on devices in which the entire stack is annealed together is ongoing. Once this annealing is accomplished, thermal ink-jet printing of PZT of the highest dielectric and piezoelectric quality will have been realized.

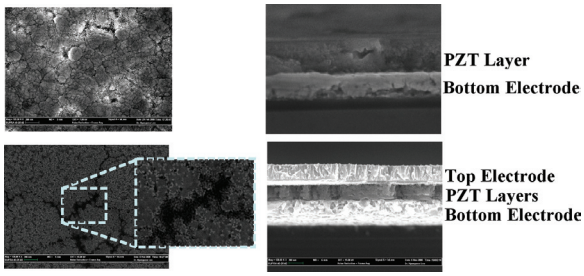


FIGURE 1: SEM images of two thermal ink-jetted PZT devices. Top: single 400nm layer; bottom: 4x100nm layers.

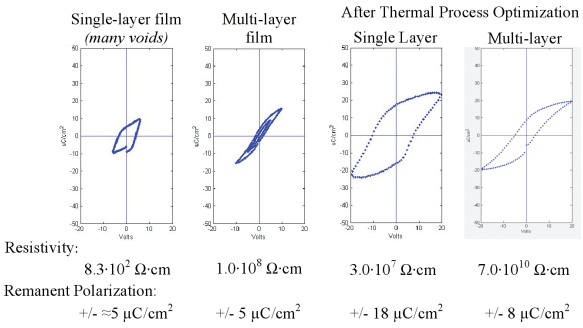


FIGURE 2: Performance data for four printed PZT devices showing the improvement as thermal processing improved and multi-layer deposition was begun.

REFERENCES

[1] S. Bathurst, H. W. Lee and S. G. Kim, "Direct Printing of Lead Zirconate Titanate Thin Films," in *21st IEEE International Conference on Micro Electro Mechanical Systems"*, 2008, pp 391-394.

Nonlinear Pie-shaped MEMS-scale Energy-harvester

A. Hajati, S. G. Kim

Sponsorship: DARPA Microsystem Technology Office, NSF

A novel nonlinear pie-shaped thin-film lead zirconate titanate Pb(Zr,Ti)O (PZT) MEMS energy-harvester has been developed. It harvests energy from parasitic ambient vibration via piezoelectric effect and converts it to electrical energy. The new nonlinear pie-shaped design tries to exploit the maximum theoretical power density of PZT for small levels of vibration and wide range of frequencies in a robust way. Contrary to the traditional designs based on cantilever high-Q oscillators which use bending strain, the new design heuristically utilizes the stretching strain in doubly-anchored beams in order to maximize the strain and power. It also provides a wide-bandwidth of operational frequency due to the system's nonlinearity and enables a robust power generation amid the unexpected change in the vibration spectrum. The device is microfabricated by a combination of surface and bulk micromachining processes in order to use the whole thickness of wafer to form a heavy proof mass. For the structural layers of the beams, 2-μm-thick, high-quality, low-stress silicon nitride is used; it is deposited using low-pressure chemical vapor deposition (LPCVD). Layers of thin-film PZT and ZrO_2 as the diffusion barrier are deposited by sol-gel spin-coating, wet-etched, and annealed to form the active area of the device. E-beam deposition and lift-off is used to place interdigitated (IDT) electrodes that extract the generated charge, exploiting the d piezoelectric mode of PZT. Deep reactive-ion-etching (DRIE) from top and back of the wafer patterns the nitride beams and silicon proof mass and finally a XeF_2 etching of silicon fully releases the device. Released devices are super-glued on Pin Grid Array (PGA) packages in such a way that the proof mass is located on top of the cavity to give it enough space for motion in response to the base vibration. The pads on the device are wire-bonded to the package's pads. Devices are heated to 100C and poled at 180kV/cm for 30 minutes using the setup shown in Figure 1. The piezoelectric properties of each device are electrically verified by Polarity/Voltage measurement (Figure 2). Currently, the poled devices are under electromechanical testing to verify their energy-harvesting characteristics.

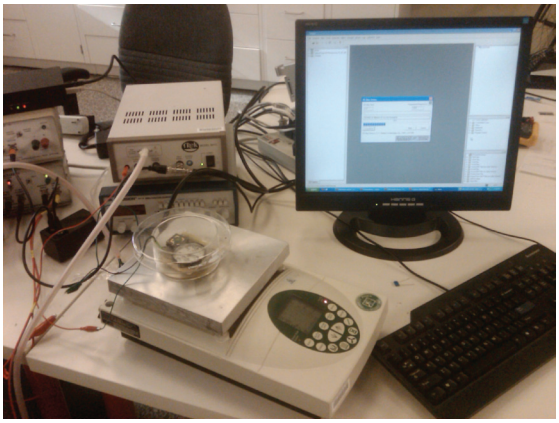


FIGURE 1: Device is being poled.

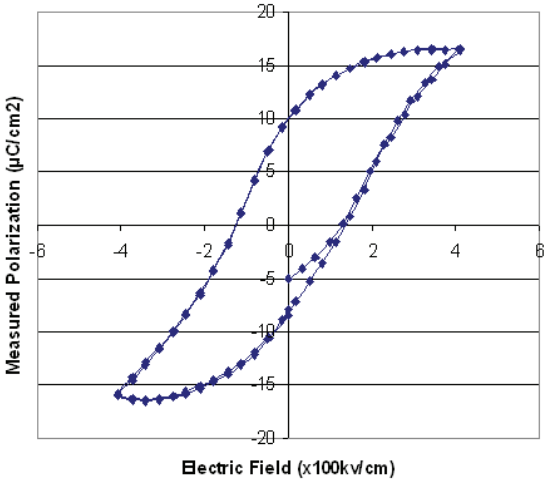


FIGURE 2: The P-V curve shows a healthy piezoelectric material.

REFERENCES

[1] Y.R. Jeon, Sood, J.H. Jeong, S.G. Kim, "MEMS power generator with transverse mode thin film PZT," *Sensors and Actuators A: Physical*, vol. 122, pp. 16-22, 2005.

[2] W.J. Choi, Y. Xia, J.A. Brewer, and S.G. Kim, "Energy harvesting MEMS device based on thin-film piezoelectric cantilevers," in *Proc. of INSS05*, San Diego, CA, June 27-28, 2005.

[3] A. Hajati and S.G. Kim, "Rectifierless Piezoelectric Micro Power Generator," *SPIE Smart Structures and Materials & Nondestructive Evaluation and Health Monitoring 2008*, San Diego, CA, 2008.

Templated Inkjet Printing for MEMS

H. J. Lee, S. Bathurst, H. Lee, S. G. Kim
Sponsorship: DARPA, Hewlett-Packard, Korea Institute of Science and Technology

Drop-on-demand (DoD) printing has shown great promise as a low-volume production method for MEMS. A new method for depositing lead zirconate titanate (PZT) piezoelectric thin films via thermal inkjet (TIJ) printing was recently reported by authors [1]. We demonstrated that well optimized printing conditions could provide thickness uniformity with less than 100-nm variation. However, the printed pattern showed more than +/- 10-μm edge (line) roughness, which is far bigger than the necessary minimum feature size for most MEMS devices. In general, the minimum possible line width created by most droplet-based deposition processes has been bigger than ~25 mm due to the possible spot resolution, and 3-5 mm roughness was demonstrated only in a research environment [2]. A pre-fabricated dam or trench can be a solution for defining fine edges by printing, which requires additional dam patterning with lithography or laser trimming and additional post-processing steps for dam structure removal [1], [3].

We show that an imprinted self-assembled mono-layer (SAM) template behaves as a wetting/non-wetting barrier for water-based inkjetted droplets and confines water-based inks within the hydrophilic region. The SAM imprinting is done by micro-contact printing with fluorinated thiol ink. The smallest droplet size tested in this work was 3pL, which could define 20-μm line roughness at best. The inkjet droplets were printed between the imprinted square patterns as shown in Figure 1. The pitch between each droplet and the dropping interval were controlled as shown in Figure 2. The left figures show the patterns without imprint guided inkjet printing and the right figures show the printing with template assistance. The pattern with imprint assisted printing shows a line roughness of less than +/- 1μm, which could not be achieved with the current inkjet printing methods.

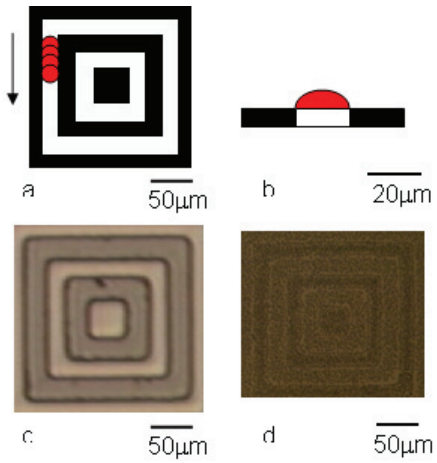


FIGURE 1: Top view (a) and cross-section view (b) of imprint guided printing; the red dot is dropped ink, white region is hydrophilic, and black is hydrophobic. A PDMS stamp (c) and invisible thiol pattern on platinum surface (d) shown by exhaled moisture

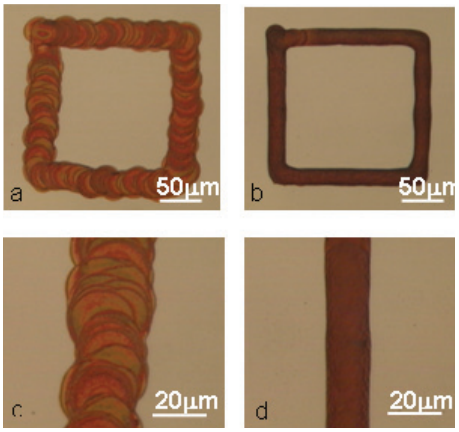


FIGURE 2: Inkjet-printed lines on untemplated surface (a) and templated surface (b). The untemplated case shows line roughness of +/- 10mm (c) and the templated case is +/- 1mm (printing condition: 3pL ink drop/ 2.5-mm pitch/ 2.0 second dropping interval).

REFERENCES

[1] S. Bathurst, H.W. Lee, S.-G. Kim, "Direct printing of lead zirconate titanate thin films for microelectromechanical systems," in *Micro Electro Mechanical Systems, MEMS 2008. IEEE 21st International Conference*, January 13-17, 2008, pp. 391-394.

[2] Y. Wang, J. Bokor, A. Lee, "Maskless lithography using drop-on-demand inkjet printing method," *Lithographic Technologies VIII*. Edited by Mackay, R. Scott. *Proceedings of the SPIE*, volume 5374, pp. 628-636 (2004).

[3] E. Lam, "Fabrication and material characterization of silver cantilevers via direct surface micromachining," Master's thesis, Massachusetts Institute of Technology, Cambridge, 2008.

A 1-mW, 25-Hz Vibration-energy-harvesting System

S. C. Chang, D. M. Otten, J. H. Lang
Sponsorship: DARPA

This project is part of the Hybrid Insect MEMS (HI-MEMS) program sponsored by the Defense Advanced Research Projects Agency (DARPA). The main objective of this program is to establish the interface between adult neural systems and external electronics. Here, insects are the first test bed, and they will be directed to fly to specific locations in real time via wireless remote control through the external electronics. In order to provide sustainable energy for the controlling on-moth electronics, a local energy-harvesting system is required. The energy-harvesting system has two major parts: the vibration-energy-harvester [1] and the DC-DC boost converter [2]. In the past 12 months, a 1-mW vibration-energy-harvester was designed, fabricated, and tested. Figure 1 shows the harvester. A DC-DC 10-mV to 1-V boost converter has also been designed and is ready for tape out. Figure 2 shows the topology of the boost converter.

The vibration-energy-harvester consists of a resonator with moving magnets and a coil. As the resonator vibrates, neodymium iron boron magnets sweep past coils through which power will be harvested. The coils are made with flexible printed-circuit technology to maximize the flux linkage and minimize the coil mass. The harvester was tested on a shaker table, which simulates the vibration of a moth. After testing, 1-mW of time average power was extracted at a mass cost of 1.067g. Work is now underway to significantly reduce the mass of the harvester.

The boost converter takes in the AC output voltage of the harvester, rectifies it to a DC voltage and boosts the voltage to 1V. The converter is a two-stage boost converter with off-chip inductors to increase the quality factor and overall efficiency. Due to the low input voltage of the harvester, synchronous rectification using low-power discontinuous comparators is employed. Spice simulation indicates that the converter can achieve 80% efficiency. The power processing switches have been laid out and are currently in the queue to be fabricated in 0.18-um CMOS process.

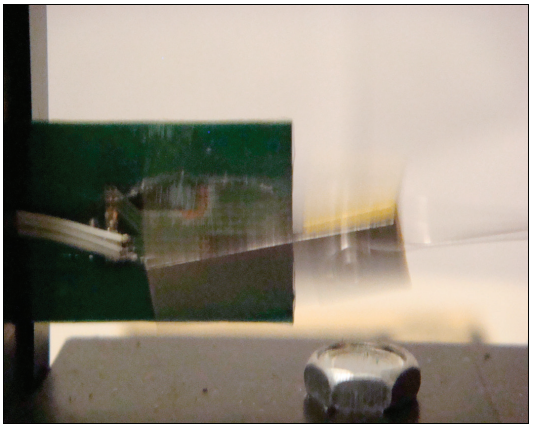


FIGURE 1: Energy-harvester system scavenging power from a shaker table that simulates the vibration of a flying moth. The harvester is capable of generating 1-mW of power from a 25-Hz, 1-mm vibration source.

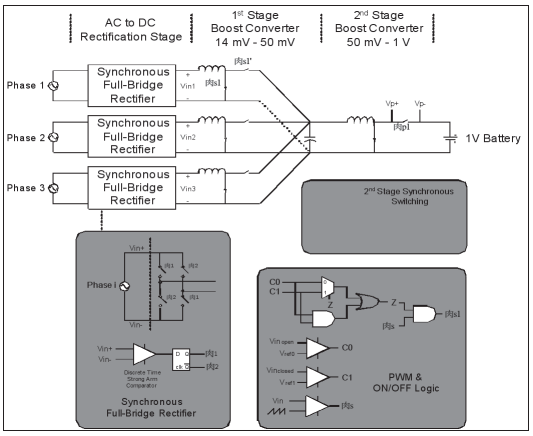


FIGURE 2: Boost Converter Circuit topology consisting of three sets of first-stage boost converters with synchronous rectification. Inductors will be off-chip.

REFERENCES

[1] R. Amirtharajah and A. P. Chandrakasan, "Self-powered signal processing using vibrationbased power generation," *IEEE Journal of Solid-State Circuits, 1997 Symposium on VLSI Circuits,* 13-15 June 1997, vol. 33, pp. 687-95, 1998.

[2] S. Meninger, J. O. Mur-Miranda, R. Amirtharajah, A. Chandrakasan, and J. H. Lang, "Vibration- to-electric energy conversion," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 9, pp. 64-76, 2001.

Development and Application of Distributed MEMS Pressure Sensor Array for AUV Object Avoidance

V. I. Fernandez, S. M. Hou, F. S. Hover, J. H. Lang, M. S. Triantafyllou
Sponsorship: NOAA: MIT Sea Grant College Program

A novel sensing technology for unmanned undersea vehicles (UUVs) is under development. The project is inspired by the lateral line sensory organ in fish, which enables some species to form three dimensional maps of their surroundings. The lateral line is a sensory system which measures the flow velocity and pressure distribution over the fish's surface, enabling behaviors such as collision avoidance [1] and object recognition [2]. These behaviors are related to a particular subset of the lateral line organ, which measures only the pressure gradient [3]. We report progress in fabricating a sensor array capable of measuring similar quantities as the lateral line organ.

The system consists of arrays of hundreds of pressure sensors spaced about 2 mm apart on etched silicon and Pyrex wafers. The sensors are arranged over a surface in various configurations. The target pressure resolution for a sensor is 1 Pa, which corresponds to the noiseless disturbance created by the presence of a 0.1-m-radius cylinder in a flow of 0.5 m/s at a distance of 1.5 m. A key feature of a sensor is the flexible diaphragm, which is a thin (20 μm) layer of silicon attached at the edges to a silicon cavity. The strain on the diaphragm due to pressure differences across the diaphragm is measured. At this stage, the individual MEMS pressure sensors are being constructed and tested.

The output voltage was measured and the relative change in resistance $\Delta R/R$ for the resistors as functions of pressure were calculated (Figure 2). For a diaphragm with a width of 2.82 mm, we obtained the experimental values of $(\Delta R/R)/P$ are -2.94×10^{-7} Pa, -2.78×10^{-7} Pa, 2.52×10^{-7} Pa and 2.65×10^{-7} Pa. The theoretical value is $\pm 1.07 \times 10^{-7}$ Pa. There are several explanations for the discrepancy between theory and experiment. Regardless, the sensitivity of the sensor is better than the original expectations.

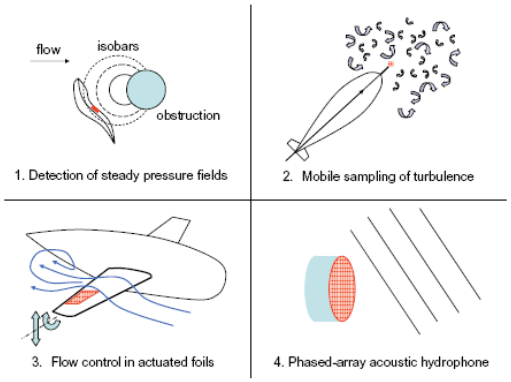


FIGURE 1: Pressure-sensor array applications.

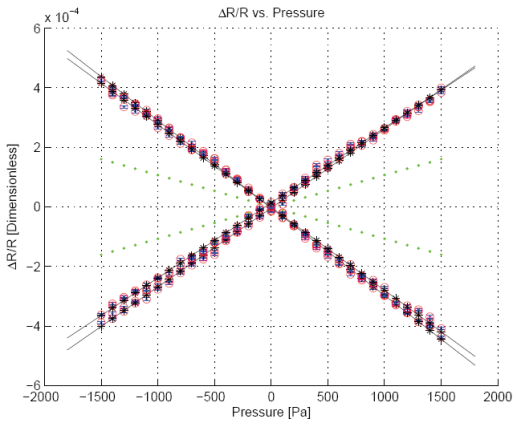


FIGURE 2: $\Delta R/R$ at various pressures for each of the four strain-gauge resistors on a particular diaphragm with width 2.82 mm. The circles represent data points, the asterisks and solid lines represent the best-fit lines, and the dotted lines represents the theoretical data.

REFERENCES

[1] S.P. Windsor, D. Tan, J.C. Montgomery. "Swimming kinematics and hydrodynamic imaging in the blind Mexican cave fish (Astayanax fasciatus)," *Journal of Experimental Biology*, vol. 211, pp. 2950-2959, 2008.

[2] C. von Campenhausen, I. Riess, and R. Weissert, "Detection of stationary objects by the blind cave fish *Anoptichthys jordani* (Characidae)," *Journal of Computational Physiology A*, vol. 143, pp. 369-374, 1981.

[3] J.C. Montgomery, S. Coombs, and C.F. Baker, "The mechanosensory lateral line system of the hypogean form of *Astyanax fasciatus*," *Environmental Biology of Fishes*, vol. 62, pp. 87-96, 2001.

Integrated Measurement of the Mass and Surface Charge of Discrete Microparticles Using a Suspended Microchannel Resonator

P. Dextras, T. P. Burg, S. R. Manalis
Sponsorship: NCI

Measurements of the mass and surface charge of microparticles are employed in the characterization of many types of colloidal dispersions. The suspended microchannel resonator (SMR) is capable of measuring individual particle masses with femtogram resolution. Here we employ the high sensitivity of the SMR resonance frequency to changes in particle position relative to the cantilever tip to determine the electrophoretic mobility of discrete particles in an applied electric field [1]. When a sinusoidal electric field is applied to the suspended microchannel, the transient resonance frequency shift corresponding to a particle transit can be analyzed by digital signal processing to extract both the buoyant mass and electrophoretic mobility of each particle (Figure 1). These parameters, together with the mean particle density, can be used to compute the size, absolute mass, and surface charge of discrete microspheres, leading to a true representation of the mean and polydispersity of these quantities for a population. We have applied this technique to an aqueous suspension of two types of polystyrene microspheres in order to differentiate them on the basis of their absolute mass and their surface charge (Figure 2). The integrated measurement of electrophoretic mobility using the SMR is found to be quantitative based on comparison with commercial instruments and exhibits favorable scaling properties that will ultimately enable measurements from mammalian cells.

REFERENCE

[1] P. Dextras, T. P. Burg, and S. R. Manalis, "Integrated Measurement of the Mass and Surface Charge of Discrete Microparticles Using a Suspended Microchannel Resonator," Anal. Chem., 2009, 81 (11), pp 4517–4523.

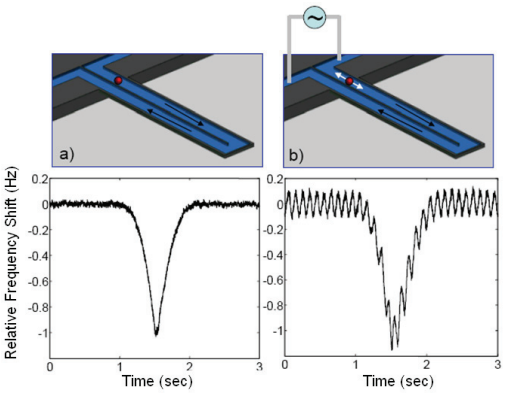


FIGURE 1: (a) A cut-away view of the fluid-filled suspended microchannel through which particles travel (top). This channel is a tunnel through the inside of the resonant cantilever structure. A transient resonance frequency time course is shown (bottom) for a 2.2μm polystyrene particle which drifts through the sensor under a small pressure gradient. The height of the peak is proportional to the particle's buoyant mass. (b) If an oscillating electric field is applied longitudinally to the channel, particles will oscillate at the same frequency due to a combination of electrophoresis and electroosmotic flow. Spectral analysis of the resulting resonance frequency time course can be performed to extract the particle's electrophoretic mobility.

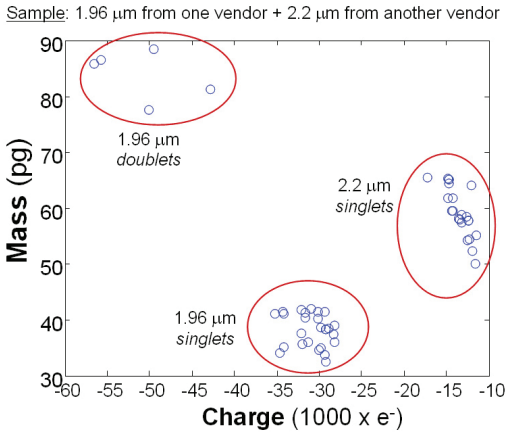


FIGURE 2: Plotting the absolute masses of individual particles against their measured zeta potential or charge reveals additional information about the population. Both scatter plots reveal two sub-populations of the more negative of the two particle types, which is not evident in the zeta potential data alone. We interpret these to be monomers and dimers of this particle type since one sub-population has a mean mass that is roughly double that of the other one at the same zeta potential. The observation that this type of particle tends to aggregate more than the other type in the mixture is supported qualitatively by the observation that these particles exhibited higher non-specific binding to the channel walls. The mass-charge scatter plot illustrates how these sub-populations are more readily differentiated on the basis of charge. It is therefore expected that integrated measurement of both the surface charge and mass distributions will provide advantages in the differentiation of complex particle mixtures.

Surface Micromachining via Digital Patterning

E. W. Lam, H. Li, V. Bulović, M.A. Schmidt
Sponsorship: DARPA, Hewlett-Packard

Conventional microelectromechanical systems (MEMS) fabrication relies heavily on the semiconductor manufacturing paradigm. While this model is well-suited for planar devices such as integrated circuits, it is drastically limited in the design and fabrication of three-dimensional devices such as MEMS. From a commercial viewpoint, this paradigm also poorly fits MEMS because the lower market demand makes it harder to offset the high production costs. Ridding MEMS fabrication of its reliance on such techniques may introduce several advantages, namely a wider base of substrate materials as well as decreased manufacturing costs.

Our project investigates severing MEMS fabrication from the traditional paradigm via digital patterning technologies. We have previously shown how MEMS can be used for the direct patterning of small molecular organics [1]. Using similar concepts, we have shown that surface micromachining can also be achieved.

In 2007-2008, we identified a viable material set for our surface micromachining process' sacrificial and structural layers: poly-methylmethacrylate (PMMA) and silver nanoparticles. To account for surface non-uniformity of the deposited PMMA, we employed solvent vapors to effectively lower the polymer's glass transition temperature and cause reflow at room temperatures [2]. To limit surface wetting and increase material loading of the silver nanoparticles, we deposited a PMMA reservoir to contain the silver nanoparticle solution (Figure 1). Free-standing cantilevers were fabricated (Figure 2), confirming that these techniques can be used for a surface micromachining process.

The next stage will be to fabricate additional MEMS structures and test the silver nanoparticle's mechanical properties. These properties will be used to design and fabricate a demonstration system based on our surface micromachining process. Subsequent stages will include creating a library of digital fabrication processes so that entire MEMS devices can be fabricated without the use of semiconductor manufacturing techniques.

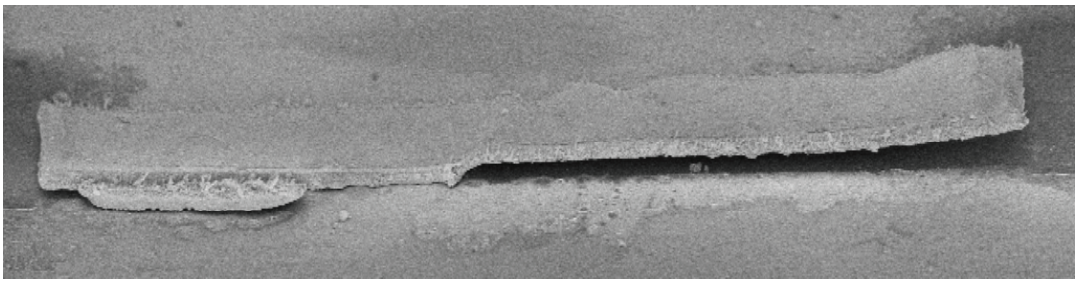


FIGURE 1: A silver surface micromachined cantilever fabricated using direct printing.

REFERENCES

[1] J. Chen, V. Leblanc, S.-H. Kang, M.A. Baldo, P.J. Benning, V. Bulović, and M.A. Schmidt, "Direct patterning of organics and metals using a micromachined printhead," in *Proc. MRS Spring 2005*, San Francisco, CA, Mar./Apr. 2005, pp. H1.8:1-7

[2] J. Feng, M. Winnik, R.R. Shivers, and B. Clubb, "Polymer blend latex films: morphology and transparency," *Macromolecules*, vol. 28, no. 23, pp. 7671-7682, Nov. 1995.

Integration of Printed Devices and MEMS

H. Li, M. A. Schmidt
Sponsorship: DARPA, Hewlett-Packard

As part of an overall effort on Non-Lithographic Technologies for MEMS and NEMS, we are developing processes for the integration of printed MEMS and devices. The goal of this project is to demonstrate the power of a printed technology for microsystems. We have already developed a surface micromachined cantilever technology that utilizes silver as a structural material and a novel organic spacer. Further, we have developed a family of both inorganic and organic devices that can ultimately be printed. As an initial demonstration, we are building a MEMS capacitive accelerometer that integrates the silver surface micromachined proof mass and spring with a capacitive sense circuit fabricated using organic FETs.

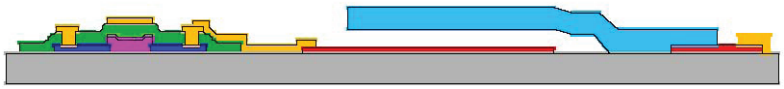


FIGURE 1: Schematic illustration of the integration of a printed MEMS cantilever with a printed electronic device.

The MIT-OSU-HP Focus Center on Non-lithographic Technologies for MEMS and NEMS

M. A. Schmidt (in coll. with S.-G. Kim, C. G. Sodini, V. Bulović, H. L. Tuller, MIT; D. Keszler, J. Wager, OSU; J. Stasiak, Hewlett-Packard)
Sponsorship: DARPA, Hewlett-Packard

This center is part of a set of centers on MEMS/NEMS fundamentals supported by DARPA. The MIT-OSU-HP Focus Center aims to develop new methods for fabrication of MEMS and NEMS that do not use conventional lithographic techniques. The Center leverages the leading expertise of MIT and OSU in MEMS and printed devices, with the printing expertise of HP. The Focus Center is organized into four primary areas: tools, materials and devices, circuits, and demonstration systems.

In the area of tools, we are leveraging the existing thermal inkjet (TIJ) technology of HP and augmenting it with specific additional features, which expand the palette of available materials for printing. We are developing materials and devices over a broad spectrum from active materials and photonic and electronic materials to mechanical materials. In the circuits area, we are studying the behavior of the devices that can be realized in this technology with the goal of developing novel circuit architectures. Lastly, we intend to build several "demonstration" systems that effectively communicate the power of the new technologies that will emerge from this center. In the past year, the center has succeeded in demonstrating a number of the key "building blocks" for a fully printed system. Specifically, we have created printed transistors, printed optical elements (light emitters and photodetectors), printed active materials (piezoelectrics), and a printed MEMS structure (micro-cantilever). Looking forward, we will begin efforts to integrate some of these building blocks.

MEMS Micro-vacuum Pump for Portable Gas Analyzers

V. Sharma, M.A. Schmidt
Sponsorship: DARPA

There are many advantages to miniaturizing systems for chemical and biological analysis. Recent interest in this area has led to the creation of several research programs, including a Micro Gas Analyzer (MGA) project at MIT. The goal of this project is to develop an inexpensive, portable, real-time, and low-power approach for detecting chemical and biological agents. Elements entering the MGA are first ionized, then filtered by a quadrupole array, and sensed using an electrometer. A key component enabling the entire process is a MEMS vacuum pump, responsible for routing the gas through the MGA and increasing the mean free path of the ionized particles so that they can be accurately detected.

A great deal of research has been done over the past 30 years in the area of micro pumping devices [1, 2]. We are currently developing a displacement micro-vacuum pump that uses a piezoelectrically driven pumping chamber and a pair of piezoelectrically driven active-valves; the design is conceptually similar to the MEMS pump reported by Li et al. [3]. We have constructed an accurate compressible mass flow model for the air flow [4] as well as a nonlinear plate deformation model for the stresses experienced by the pump parts [5]. Using these models, we have defined a process flow and fabricated five generations of the MEMS vacuum pump over the past years and are currently working on improving the overall design.

Figure 1 shows a schematic of the pump. For ease in testing we have initially fabricated only layers 1-3 and have constructed a testing platform which, under full computer control, drives the pistons and monitors the mass flows and pressures at the ports of the device. The lessons learned from the first four generations of the pump have led to numerous improvements. Every step from the modeling, to the etching and bonding, to the testing has been modified and improved along the way. The most recent fifth generation pump test data appears in Figure 2. Figure 2a shows the measurements of the vacuum being generated in an external volume ($5.6cm^3$) by the micropump operating at 2Hz. The pump was able to reduce the external volume pressure by 163 Torr. Figure 2b shows the micropump-generated flow rate as a function of pumping frequency (driven in a 6-stage cycle by a controlling microprocessor to move the gas from the input to the output). The performance of this pump compares very well with that of other similar scaled micropumps in the literature. Next, we plan to fabricate and test an improved overall design and develop a final set of models to fabricate any future micropumps to the desired specifications.

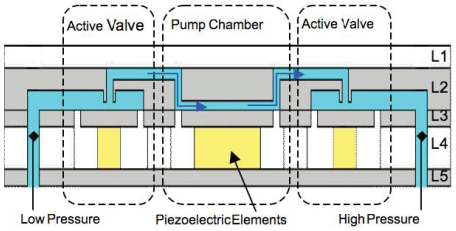


FIGURE 1: The MEMS vacuum pump schematic. Layers 1 and 4 are glass, layers 2 and 5 forming the chambers, channels, and support are silicon, and layer 3 forming the pistons and tethers is SOI silicon

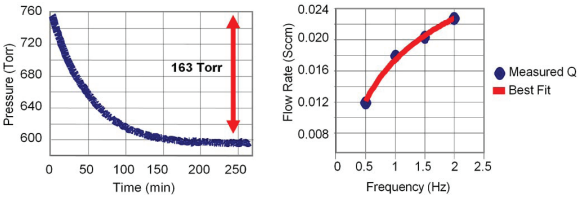


FIGURE 2: a) The vacuum generation performance of the micropump. b) The pump-generated flow rate as a function of the pumping frequency.

REFERENCES

[1] D.J. Laser and J.G. Santiago, "A review of micropumps," *Journal of Micromechanics and Microengineering*, vol. 14, no. 6, pp. 35-64, 2004.

[2] P. Woias, "Micropumps--past, progress and future prospects," *Sensors and Actuators B: Chemical*, vol. 105, no. 1, pp. 28-38, 2005.

[3] H.Q. Li, D.C. Roberts, J.L. Steyn, K.T. Turner, J.A. Carretero, O. Yaglioglu, Y.-H. Su, L. Saggere, N.W. Hagood, S.M. Spearing, M.A. Schmidt, R. Mlcak, and K. Breuer, "A high-frequency, high flow rate, piezoelectrically driven MEMS micro-pump," *IEEE Solid State Sensors and Actuators Workshop*, Hilton Head SC, June 2000.

[4] A.K. Henning, "Improved gas flow model for micro-valves," *Proceedings of Transducers 2003*, Boston, MA, pp. 1550-1553, June 2003.

[5] D.C. Roberts, O. Yaglioglu, J.Carretero, Y.-H Su, L. Saggere, and N.W. Hagood, "Modeling, design, and simulation of a piezoelectrically driven microvalve for high pressure, high frequency applications," in *Proc. SPIE–The International Society for Optical Engineering, Smart Structures and Materials 2001–Smart Structures and Integrated Systems*, Newport Beach, CA, Mar. 2001, pp. 366-380

Phase-change Materials for Actuation

Q. Guo, Y. Li, J. Kalb, C. V. Thompson
Sponsorship: Singapore-MIT Alliance

Phase-change materials (chalcogenide alloys) are used for optical data storage in commercial phase-change memories, such as rewritable compact discs (CD±RW) and rewritable digital video disks (DVD±RW, DVD-RAM). Recently, they have also shown high potential for the development of phase-change random access memories (PC-RAMs or PRAMs), which might replace flash memories in the future.

In this project, we suggest a different application of phase-change materials in optically triggered micro actuators [1]. The suggested device consists of a thin film of a phase-change material deposited on a micro-fabricated low-stress SiN cantilever. The SiN cantilevers are manufactured by chemical vapor deposition of low-stress SiN on Si wafers, patterning the SiN film using optical lithography and revealing the cantilevers using dry etching and wet etching. Amorphous thin films of phase-change materials are subsequently sputter-deposited on these cantilevers. A laser-induced crystallization in the film initiates a cantilever deflection since this transformation is accompanied by a large density change at the order of 6-9%. Then we will re-amorphize the crystalline part of the film by short laser pulses, and the cantilever tip should return to its initial position. Both the amorphous and crystalline states of phase-change materials are stable at room temperature, and the resulting device can serve as a bi-stable micro actuator.

We have also used a similar technique to investigate the stress change as a function of film thickness and capping layer [2]. This approach can be used in optimization of chalcogenides for use in PRAMS.

In addition to chalcogenides, the cantilevers used with combinatorial deposition have been used to investigate the crystallization-induced stress for a metallic amorphous alloy system (Cu-Zr). It was discovered that the magnitude of the stress change scaled with the ease of glass formation, yielding fundamental new insight into the materials requirements for amorphization [3].

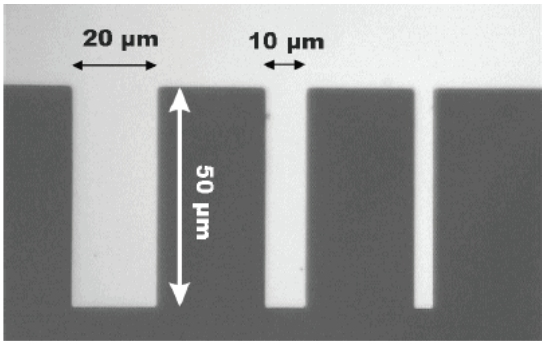


FIGURE 1: Optical micrograph of SiN cantilevers fabricated using optical lithography and dry/wet etching. An amorphous phase-change $Ge_2Sb_2Te_5$ film has been deposited on top.

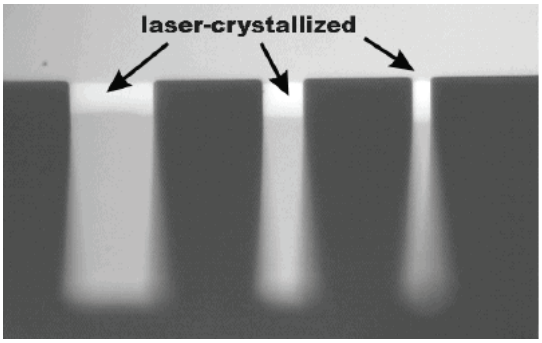


FIGURE 2: The $Ge_2Sb_2Te_5$ film has been crystallized with a scanning HeNe laser near the support of the cantilevers. As a consequence, the reflectivity increases and the cantilever tip moves up by about 7.5µm, which reveals the laser-induced strain and stress in the film.

REFERENCES

[1] J.A. Kalb, Q. Guo, X. Zhang, Y. Li, C. Sow, and C.V. Thompson, Phase-Change Materials in Optically Triggered Microactuators, J. of Microelectromechanical Systems 17, 1094 (2008).

[2] Qiang Guo, Minghua Li, Yi Li, Luping Shi, Tow Chong Chong, Johannes A. Kalb, and Carl V. Thompson, Crystallization-induced stress in thin phase change films of different thicknesses, Appl. Phys. Lett., 93, 221907 (2008).

[3] Y. Li, Q. Guo, J.A. Kalb, and C.V. Thompson, Matching Glass-Forming Ability with the Density of the Amorphous Phase, Science 322, 1816 (2008).

Origin and Control of Intrinsic Stresses in Metallic Thin Films for N/MEMS Applications

H. Yu, C. V. Thompson
Sponsorship: NSF

Because mechanical properties strongly influence the reliability and performance of films in N/MEMS applications, understanding and controlling of the intrinsic stresses in as-deposited films is of great importance. For high-atomic-mobility metals (e.g., Au, Ag, Al, Cu) deposited on amorphous substrates, much of the observed tensile stress can be attributed to grain structure evolution during which individual islands grow, impinge, and coalesce to form a continuous film. The stress state shifts from tensile during island coalescence to compressive as the film grows past continuity (see Figure 1).

The origin of post-coalescence compressive stress has been debated extensively over the past decade. Models associated with adatom-surface [1], [2] and adatom-grain boundary [3] interactions have been proposed to explain the compressive stress generation during deposition and its relaxation during interruptions of growth. Using an in-situ stress measurement system and ex-situ TEM characterization, we have experimentally shown that, for films with the same thickness, grain size has an impact on stress behavior during a growth interruption. The relationship between the inverse of grain size and the corresponding reversible stress rise was found to be linear, with zero stress for heteroepitaxial film (interpreted as films with "infinite" grain size) (see Figure 2) [4]. This experimental result strongly indicates that the microstructure of the as-deposited film, especially the grain boundary, is critical to the origin and control of intrinsic compressive stress in these films.

Current investigations are focused on analysis of the effects of processing conditions, e.g., substrate temperature and deposition rate, on the magnitude of the residual stresses in polycrystalline films We are also investigating the use of substrate topography to control island formation and stress evolution.

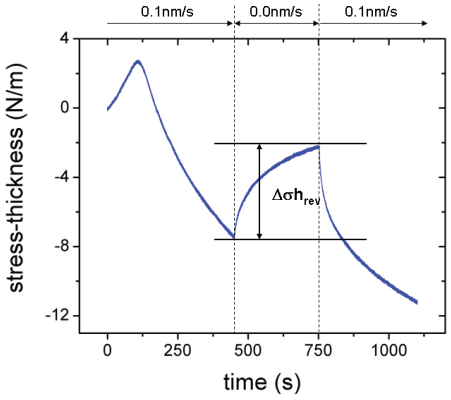


FIGURE 1: Stress-thickness curve for gold deposited at 0.1 nm/s on stress-free silicon nitride. The growth was interrupted after 450 s and resumed after 750 s.

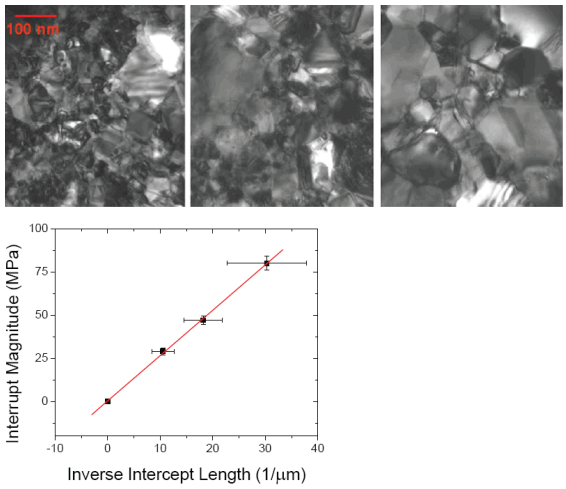


FIGURE 2: The TEM characterization and the relationship between tensile rise during interruption and the inverse grain size. As the grain size increases, the stress trends towards zero.

REFERENCES

[1] F. Spaepen,"Interfaces and stresses in thin films," Acta. Materialia, vol. 48, pp. 31-42, 2000.

[2] C. Friesen and C.V. Thompson, "Reversible Stress Relaxation during Precoalescence Interruptions of Volmer-Weber Thin Film Growth, Physical Review Letters, vol. 89, no.2, p.126103, Sept. 2002.

[3] E. Chason, B.W. Sheldon, L.B. Freund, J.A. Floro, and S.J. Heame, "Origin of compressive residual stress in polycrystalline thin films", Physical Review Letters, vol. 88,no. 15, p. 156103, Apr.2002..

[4] J.S. Leib, "Relationships Between Grain Structure and Stress in Thin Volmer-Weber Metallic Films," Doctoral Thesis, Massachusetts Institute of Technology, Cambridge, 2008.

Microfluidic Perfusion for Modulating Stem Cell Diffusible Signaling

K. Blagović, L. Przybyla, Y.-C. Toh, J. Voldman

Sponsorship: NIH NIBIB, NSF Graduate Research Fellowship, A*STAR International Fellowship

Stem cell phenotype and function are influenced by microenvironmental cues comprised of cell-cell, cell-extracellular matrix (ECM), cell-media interactions, and mechanical forces. Although conventional cell-culture techniques have been successful, they provide incomplete control of the cellular microenvironment. Our research focuses on developing microscale systems for controlling the cellular microenvironment of mouse embryonic stem cells (mESCs) to control their function.

To modulate cell-media interactions, we have developed a two-layer PDMS microfluidic device that incorporates a valve architecture, debubblers, and cell culture chambers, allowing for a rich set of culture conditions on the same chip [1-3]. We are using our microfluidic system to determine the minimal media sufficient for mESCs to maintain their self-renewal characteristics under constant flow. Upon growing mESCs in defined, serum-free media conditions under perfusion, we have observed a change in the preponderance and the heterogeneity of stem cell markers. Using a combination of assays, we have observed similar or upregulated levels of the stem cell marker Nanog, as well as a more stem cell-like morphology of cells under perfusion (Figure 1).

The use of ESCs for clinical therapeutic applications requires expansion of the pluripotent cells. This usually necessitates the use of a bioreactor where the cells are subjected to mechanical forces: fluid shear stresses [4]. We are quantitatively investigating the effect of fluid shear stress on ESC self-renewal by using a 1x6 logarithmic flow rate microfluidic device. By specifying the dimensions of the flow rate-setting resistor channels, we were able to apply shear stress varying by a factor of 4 across chambers, enabling us to simultaneously study shear stress effects on mESC self-renewal over a range of 1024× (Figure 2a). Initial results show that mESC proliferation is negatively correlated to shear stress over a range of 0.016 to 16 dynes/cm^2 (Figure 2a).

ESCs dynamically interact with their extracellular matrix (ECM) and culture substrate. In particular, different substrates adsorb ECM differently, which in turn affects cell attachment and function. Standard culture techniques typically utilize *tissue culture polystyrene* (TCPS), a treated polystyrene substrate that promotes ESCs attachment. We developed a process that integrates micro-patterned polystyrene onto glass substrates, combining the cell culture compatibility of polystyrene with the fabrication compatibility of glass (Figure 2b). This process integrates cell culture surfaces directly within a device and preserves the standard microfluidic assembly process of plasma bonding. We have demonstrated a simple technique for realizing multi-functional polystyrene patterns for the fabrication of complex, highly integrated microfluidic cell culture platforms.

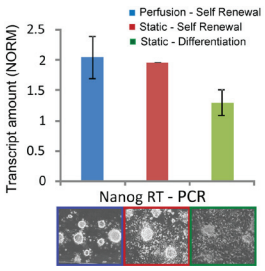
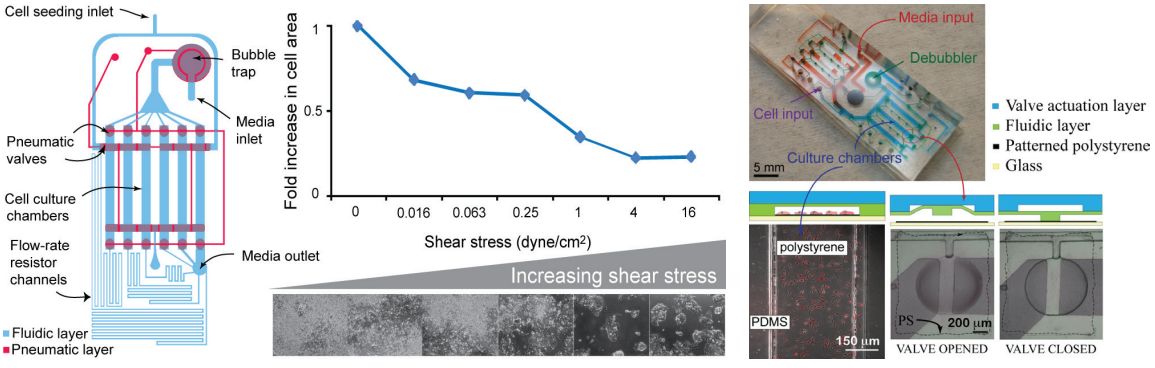


FIGURE 1: Cells grown for 5 days in a device and static culture. Quantitative analysis for self-renewal marker Nanog (RT-PCR) and corresponding phase images of mESC colonies.



(a) (b)

FIGURE 2: (a) 1×6 logarithmic flow-rate microfluidic device for studying the effects of shear stress on mESCs self-renewal. Schematic of a device (a, left). Proliferation of mESCs, experiencing a broad range of shear-stress values, cultured for 72 hours in a device (a, right). (b) Image of a 2-layer microfluidic perfusion device (b, top). Applications of micro-patterned polystyrene (PS): PS patterned cell-culture chambers with NIH-3T3 mouse fibroblasts (b, bottom left) and normally closed valves with PS patterned valve seat (b, bottom right).

REFERENCES

[1] K. Blagović, L.Y. Kim, A. M. Skelley, and J. Voldman, "Microfluidic control of stem cell diffusible signaling," in *Proc. of Twelfth International Conference on Miniaturized Systems for Chemistry and Life Sciences*, San Diego, USA, Oct. 2008, pp. 677-679.

[2] A. M. Skelley and J. Voldman, "An active bubble trap and debubbler for microfluidic systems," *Lab on a Chip*, vol. 8, pp. 1733-1737, Oct. 2008.

[3] A. M. Skelley, and J. Voldman, "An active, integrated bubble trap and debubbler for microfluidic applications," in *Proc. of Twelfth International Conference on Miniaturized Systems for Chemistry and Life Sciences*, San Diego, USA, Oct. 2008, pp. 1360-1362.

[4] E. Y. L. Fok and P. W. Zandstra, "Shear-Controlled Single-Step Mouse Embryonic Stem Cell Expansion and Embryoid Body-Based Differentiation," *Stem Cells*, vol. 23, pp. 1333-1342, Aug. 2005.

Microfluidic Control of Cell Pairing and Fusion

M. Hoehl, A. Skelley, J. Voldman
Sponsorship: NIH

Currently, several different methods have been used to reprogram somatic cells to an embryonic stem-cell-like state, including somatic cell nuclear transfer, forced expression of transcription factors, and cell fusion. Cell fusion is an appealing method by which to study reprogramming as the delivery of cells is easily visualized. However, conventional methods to fuse cells *en masse* do not control the pairing between the cell populations, resulting in heterogeneous output populations that must be further purified.

We have developed a microfluidic system in which thousands of ESCs and somatic cells (SCs) are properly paired and immobilized, resulting in a high number of one-to-one fusions that can be clearly identified for further studies [1]. The device consists of thousands of microscale cell traps in a millimeter-sized area. The traps consist of larger frontside and smaller backside capture cups made from a transparent biocompatible polymer. The key to pairing cells efficiently is to load them sequentially in a 3-step loading protocol enabling capture and pairing of two different cell types (Figure 1). The geometry of the capture comb precisely positions the two cells, and flow through the capture area keeps the cells in tight contact in preparation for fusion. With this approach we have obtained pairing efficiencies of ~70%.

The device is compatible with both chemical and electrical fusion, and, in agreement with the literature, we have obtained higher performance with electrofusion. When we compared fusion performance in our device to commercial approaches, we obtained significant improvements in overall performance for both PEG-mediated fusion and electrofusion. Specifically, we have measured fusion efficiencies of ~80% in our device using electrofusion, about 5× greater than that obtained in commercial systems. We are also able to remove fused cells from the device and culture them, demonstrating that the device creates viable fused cells (Figure 2a-b). Finally, by fusing mouse embryonic stem cells (mESCs) with mouse embryonic fibroblasts (mEFs, a somatic cell type), we have demonstrated the ability to reprogram the somatic cells to a pluripotent state as evidenced by morphology, alkaline phosphatase staining (Figure 2c), and activation of an oct4-GFP reporter present in the somatic cell genome (Figure 2d).

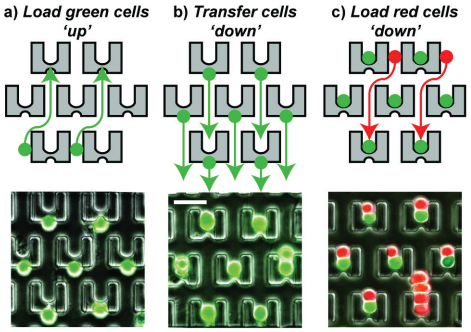


FIGURE 1: Three-step cell loading protocol. (a) Cells are first loaded "up" towards the smaller backside capture cup. (b) The direction of the flow is reversed, and the cells are transferred "down" into the larger frontside capture cup 2 rows below; scale bar, 50 mm. (c) The second cell type is loaded in from the top, and cells are captured in front of the first cell type.

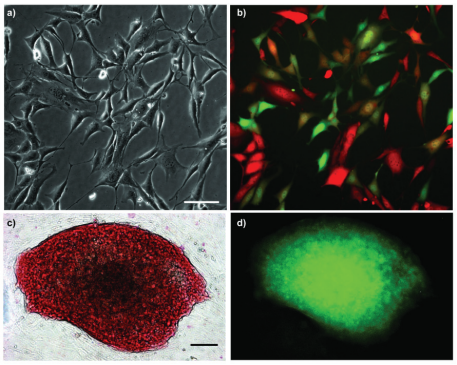


FIGURE 2: Functionality of fused cells. (a-b) Phase and fluorescent image of DSRed/EGFP fibroblasts at day 4 after fusion in the microfluidic device. scale bar, 100 mm. (c-d) Double-resistant hybrids between Hygromycin B-resistant mESCs and Puromycin-resistant mEFs after fusion in the microfluidic device, showing ESC-like morphology, positive alkaline phosphatase, staining, and reactivation of endogenous Oct4-GFP reporter; scale bar, 100 mm.

REFERENCES

[1] A. M. Skelley, O. Kirak, H. Suh, R. Jaenisch, and J. Voldman, "Microfluidic Control of Cell Pairing and Fusion," *Nature Methods,* vol. 6, pp. 147-52, 2009.

Flexible Multi-site Electrodes for Moth Flight

W. M. Tsang, S. Murray, A. I. Akinwande, J. Voldman
Sponsorship: DARPA

Significant interest exists in creating insect-based Micro-Air-Vehicles (MAVs) that would combine advantageous features of insects—small size, effective energy storage, navigation ability—with the benefits of MEMS and electronics—sensing, actuation and information processing. The key part of the insect-based MAVs is the stimulation system, which interfaces with the nervous system of the insect to bias the insect's flight path.

In this work, we have developed a flexible split-ring electrode (FSE) for insect flight control; the FSE uses a set of electrodes arranged around a split ring to provide circumferential stimulation around an insect's nerve cord (Figure 1). The FSE is made of two layers of polyimide with gold sandwiched in between in a split-ring geometry using standard MEMS processing. The stimulation sites are located at the each end of protruding tips that are circularly distributed inside the split-ring structure. These protruding tips penetrate through the cuticle tissues of the nerve cord and enable stimulation on the axon-rich region of the nerve cord.

We have been able to insert the electrode into pupae of *Manduca sexta* as early as 7 days before the adult moth emerges, and we are able to stimulate multi-directional graded abdominal motions in both pupae and adult moths. The direction of the abdominal movements depends on the particular pair of stimulation sites excited. The pupal implantation allows for tissue growth around the FSE before the adult moth emerges, which enhances the attachment of the FSE. Also, as compared to the adult moth, the body of the pupae is relatively immobile, easing the difficulty of insertion surgery. Finally, we have demonstrated that the FSE is able to stimulate abdominal motion that can in turn cause ruddering to alter adult moth flight path (Figure 2) [1].

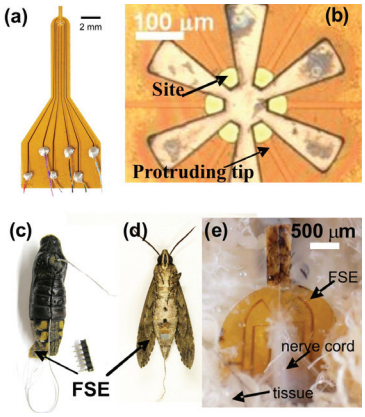


FIGURE 1: (a) Image of the FSE with wire connection; (b) Close-up image of the FSE at the split-ring region; (c) Image of a pupa with inserted FSE; (d) Enclosed adult moth with FSE inserted at the pupal stage; (e) Image of dissected adult moth showing the growth of connective tissue around the FSE.

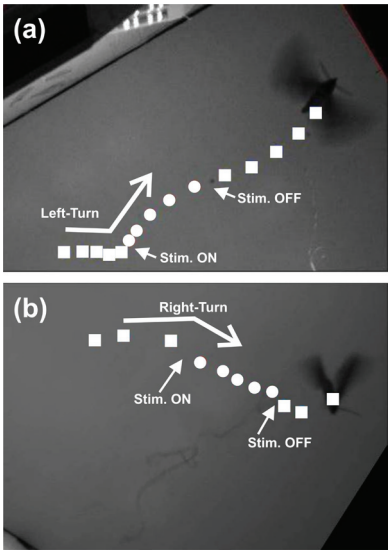


FIGURE 2: Images showing the loosely tethered moth that has been stimulated to perform (a) left and (b) right turns following the stimulation of the FSE. The flight path of the moth with and without FSE stimulation are tracked by solid circle (●) and solid square (■) dots, respectively.

REFERENCES

[1] W.M. Tsang, Z. Aldworth, A. Stone, A. Permar, R. Levine, J.G. Hildebrand, T. Daniel, A.I. Akinwande, and J. Voldman, "Insect flight control by neural stimulation of pupae-implanted flexible multisite electrodes," Micro Total Analysis Systems, 2008, pp. 1922-24.

Measuring the Effects of Electric Fields on Cell Phenotype

S. P. Desai, J. Voldman

Sponsorship: NIH, Singapore-MIT Alliance

One overarching goal of our research group involves using electric fields to manipulate, position, and ultimately sort living biological entities [1], [2]. To enable such exquisite control over living organisms, we leverage a technique called dielectrophoresis (DEP), which uses spatially non-uniform electric fields to "push" or "pull" cells towards or away from electrodes. The processing of biological samples is more readily achieved using systems on the length-scale of the samples themselves. Such biological microelectromechanical systems, or BioMEMS, enable integrated sample preparation and analysis; they leverage techniques such as DEP to enable cell manipulation. Hence, it is imperative that we understand the effects of DEP manipulation on cell physiology to determine whether DEP manipulation itself can alter particular phenotypes of interest and confound downstream biological assays. To this end, we have developed a microfabricated, high-content screening (HCS) platform that can apply a large number of different electrical stimuli to cells and then monitor the molecular effects of those stimuli using automated fluorescence microscopy. The platform consists of a chip with individually addressable arrayed electrodes and support electronics to generate the desired waveforms (Figure 1). Mammalian cells are seeded on the chip and then the entire assembly is clamped and placed in a standard cell culture incubator, where a computer-controlled custom-designed switch box automatically and autonomously applies arbitrary stimulation waveforms (varying voltage, frequency, and duration) to individual electrode sites. Since this platform uses transparent electrode structures, it can equally be used with both inverted and fluorescent microscopy techniques.

Using this HCS platform, we have been able to elucidate the response of cells to electric fields using a custom-designed live-cell stress sensor. This stress sensor was designed using transfection and cloning techniques, and it forms the basis for the read-out of our biological assay. Stressful events in the environment around the cells, such as temperature elevation (due to Joule heating) and the generation of oxygen radicals are sensed by our stress sensor and reported as a distinct fluorescence level. These fluorescent signals are collected for individual cells using automated microscopy and quantified using image-processing algorithms. The results obtained from one such set of experiments are displayed in Figure 2 (adapted from [3]). This HCS platform enables the molecular-level biological assays across a very wide range of electric field conditions, a feat challenging to accomplish with previously developed systems or assay platforms.

REFERENCES

[1] B.M. Taff, S. P. Desai, and J. Voldman, *Applied Physics Letters*, vol. 97, no. 8, pp. 084102-3, 2009.

[2] M. D. Vahey and J. Voldman, *Analytical Chemistry*, vol. 81, no. 7, pp. 2446-2455, 2009.

[3] S. P. Desai and J. Voldman, *Proceedings of Twelfth International Conference on Miniaturized Systems for Chemistry and Life Sciences*, 2008, pp. 1308-1310.

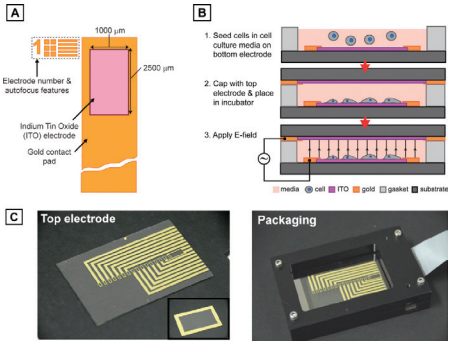


FIGURE 1: HCS platform. (A) Top-down schematic of 16 individually addressable transparent indium-tin oxide (ITO) electrodes. (B) Seeding of cells on electrodes and running the screening assay. (C) Images of bottom electrode (left panel) and top electrode chips (inset). Image of packaged device (right panel), showing bottom electrode chip visible through transparent top electrode.

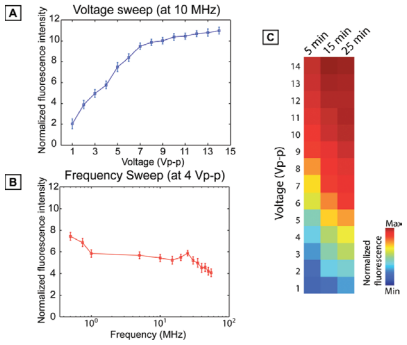


FIGURE 2: Electric-field effects. (A) The voltage sweep shows a dramatic increase in cellular stress with increase in voltage. (B) A frequency sweep indicating that cells are stressed at low frequencies (due to radical generation). (C) A heat map showing a voltage sweep for different durations of field exposure. Longer durations of exposure show increased cellular stress levels.

Image-based Sorting of Cells

J. R. Kovac, Y. Gerardin, B. M. Taff, J. Voldman
Sponsorship: NIH, DoD, NSF, Singapore-MIT Alliance

This research involves the development of architectures for screening complex phenotypes in biological cells. We augment microscopy with the ability to retrieve cells of interest. This capability will permit cell isolation on the basis of dynamic and/or intracellular responses, enabling new avenues for screening. Currently, such sorts require expensive, specialized equipment, widely prohibiting such sorts.

We have explored microfabricated/microfluidic approaches to cell sorting. These approaches employed purely dielectrophoretic (DEP) trap arrays [1], passive hydrodynamic trap arrays with active DEP-based cell release [2], and passive microwell arrays with optical cell release to permit sorting of non-adhered cells [3]. We recently developed a photolithography-inspired method that allows sorting of adherent cells without the use of microfluidics [4], illustrated in Figure 1. Here we plate adherent cells in a dish and assay them, identifying the locations of cells of interest. We then use a computer and standard office printer to automatically generate a transparency mask. After alignment of the transparency mask to the back of the cell culture dish, opaque mask features reside beneath desired cells. We then add a prepolymer to the dish, containing cell culture media, a UV-photoinitiator, and poly(ethylene glycol) diacrylate (PEGDA) monomer. Next we use a standard fluorescence lamp to shine UV light through the mask, crosslinking a hydrogel over all unmasked locations and encapsulating all undesired cells. Desired cells can be enzymatically released (Figure 2) and re-captured. Our sorting process requires standard equipment found in biology labs and inexpensive reagents (<$10 per experiment), simplifying widespread adoption.

We have demonstrated cell release from 500-μm-diameter wells, as well as the isolation of perfectly pure, viable target cells from a background population of undesired cells. Further efforts will reduce well size, enabling the sorting of denser cell populations. The simplicity and inexpensiveness of our method will allow for widespread dissemination and new cell sorting paradigms.

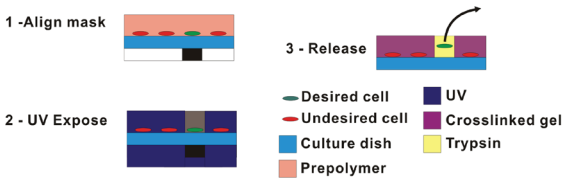


FIGURE 1: Schematic of sorting method. 1) Mask is aligned such that opaque features reside behind desired cells; prepolymer is added. 2) UV light crosslinks polymer in exposed regions, encapsulating undesired cells. 3) Un-encapsulated desired cells are released and reclaimed.

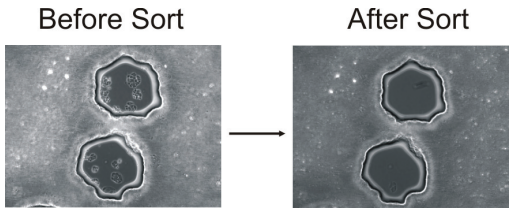


FIGURE 1: Image showing a 500-µm-diameter well surrounding desired MCF7 cells before and after sorting; cells in wells are released while cells within hydrogel remain.

REFERENCES

[1] J. R. Kovac, B. M. Taff, J. Voldman, "Enabling technologies for image-based cell sorting," in ch. "Microdevices in Biology and Medicine," Y. Nahmias, S. Bhatia, Eds. in *Methods in Bioengineering*, M. Yarmush, R. Langer, Eds. to be published.

[2] B. M. Taff, S. P. Desai, J. Voldman, "Electroactive hydrodynamic weirs for micro-particle manipulation and patterning," *Applied Physics Letters*, to be published.

[3] J. R. Kovac and J. Voldman, "Image-based cell sorting using optofluidics," in *Digest of the IEEE/LEOS Summer Topical Meetings*, 2008, pp. 193-194.

[4] J.R. Kovac and J. Voldman, "Microscopy-based sorting of adherent cells using photopolymerization-activated cell sorting (PACS)," presented at the *Biomedical Engineering Society annual meeting*, St. Louis, MO, 2008.

Cell Micropatterns for Studying Autocrine Signaling

S. Sampattavanich, N. Mittal, J. Voldman
Sponsorship: NIH NIBIB, Singapore-MIT Alliance

Autocrine signaling plays a key role in tumorigenesis and in the maintenance of various physiologic states. Due to its intrinsic, closed-loop nature, autocrine signaling is, however, difficult to investigate experimentally. Our research involves the use of cell- patterning techniques to investigate the role of autocrine signaling during *in vitro* maintenance of embryonic stem cells, stem cell differentiation, and uncontrolled expansion of cancer cells.

First we use stencil cell patterning to examine the spatial distribution of autocrine systems. Typical techniques to quantify autocrine signaling rely on bulk measurement of autocrine pathway activation using randomly plated cells. Such random cell positioning usually masks the effects of local ligand concentration gradients, reducing the chance to observe spatially varying cell responses. We fabricated regular arrays of cell patches with varying colony size and spacing and generated graded levels of autocrine ligands in space while maintaining the same global ligand concentration (Figure 1A). Using the TGFα/EGFR paradigm in A431 cells as our model, we have determined the effective length scale where autocrine signaling contributed to promote growth of adjacent cell patterns (Figure 1B) [1]. We are applying the developed platform to determine the contribution of autocrine signaling in preserving a homogeneous population of mouse embryonic stem cells (mESCs) *in vitro*.

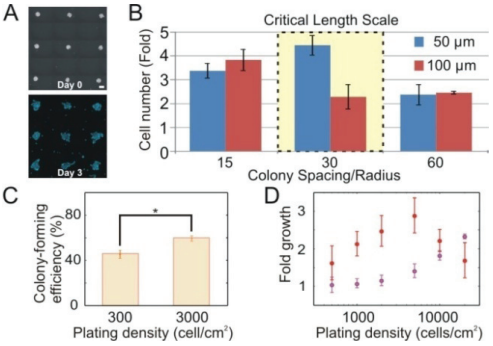


FIGURE 1: A) Stencil cell patterning is used to construct regular arrays of A431 cells with defined colony size and spacing at day 0 and day 3. Scale bar = 200 µm. B) Change in cell number of A431 cells for different geometric configurations. Error bars represent 95% confidence intervals. The result shows elevated cell growth at the colony spacing of 30 colony radii. C) Colony-forming efficiency increases with plating density. D) Fold growth increases with density on Day 0-1 (purple) and Day 1-2 (red).

Expanding on our previous work on Bio Flip Chips, we have used them to create patterns of single cells at varying densities [2]. We then studied the effects of plating density on the colony-forming efficiency of mESCs and found that the colony-forming efficiency increases with density (Figure 1C). We have confirmed this result by performing growth assays in a traditional well-plate format and in a defined medium. In this second set of assays, we found that the growth of mESCs increases with density (for a certain range), both in the first 24 hours and in the next 24 hours after plating of cells (Figure 1D). Finally, we checked that medium that has been conditioned by cells enhances the growth of mESCs. Together, these results prove that mESCs produce at least one diffusible factor that aids survival.

In addition to localization of a single cell type on the substrate, we have also developed a novel technique to fabricate complex heterotypic patterns-within-patterns [3]. Stencil-delineated electroactive patterning (S-DEP) combines dielectrophoresis (DEP) and stencil patterning to create cell clusters with customizable shapes, positions, and internal cell organization (Figure 2). Stencils define overarching tissue-like construct geometries, and negative-dielectrophoretic forcing guides subgroupings of cells to desired positions within constructs. The S-DEP enables correlation of cells' cluster location to phenotype and provides avenues for creating mosaic tissue-like constructs of phenotypically or genetically distinct cells. Such diversified chimeric cell clusters help us evaluate the impact of diffusive signaling on stem-cell differentiation.

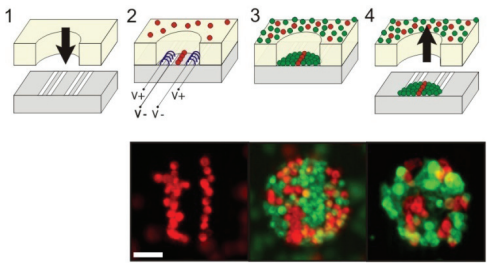


FIGURE 2: The S-DEP procedure. (1) A PDMS stencil is placed over an electroactive substrate. (2) The first cell population (stained with DiI) is seeded onto the device with the electrodes on. (3) With electrodes off, the second cell population (stained with DiO) is loaded onto the device after attachment of the first cell population. (4) After attachment of the cells, the stencil is removed, leaving behind tissue-like constructs with internally patterned subdomains. Scale bar = 50 µm.

REFERENCES

[1] S. Sampattavanich, J. Voldman, "Examining the effective autocrine length scale using stencil cell patterning," presented at *BMES Annual Fall Meeting*, St. Louis, USA, 2008.

[2] N. Mittal, J. Voldman, "Exploring cell-cell communication in mouse embryonic stem cell culture using Bio Flip Chips," presented at *6th Annual Meeting of the International Society for Stem Cell Research*, Philadelphia, USA, 2008.

[3] S. Sampattavanich, B. M. Taff, S. P. Desai, and J. Voldman, "Organizing complex multicellular constructs using stencil-delineated electroactive patterning (S-DEP)," presented in *Proc. Twelfth International Conference on Miniaturized Systems for Chemistry and Life Sciences*, 2008, pp. 567-69.

Iso-dielectric Separation of Cells and Particles

M.D. Vahey, J. Voldman

Sponsorship: NIH NIBIB, MIT Buschbaum Fund, Singapore-MIT Alliance, CSBi/Merck Graduate Fellowship

The development of new techniques to separate and characterize cells with high throughput has been essential to many of the advances in biology and biotechnology over the past few decades. Continuing or improving upon this trend – for example, by developing new avenues for performing genetic and phenotypic screens – requires continued advancements in cell sorting technologies. Towards this end, we are developing a novel method for the simultaneous separation and characterization of cells based upon their electrical properties. This method, iso-dielectric separation (IDS), uses dielectrophoresis (the force on a polarizable object [1]) and a medium with spatially varying conductivity to sort electrically distinct cells while measuring their effective conductivity (Figure 1). It is similar to iso-electric focusing, except that it uses DEP instead of electrophoresis to concentrate cells and particles to the region in a conductivity gradient where their polarization charge vanishes [2],[3].

While dielectrophoresis has been widely used in cell separation [4], iso-dielectric separation offers a unique combination of features that could be potentially enabling for new genetic screens. It is continuous-flow, capable of parallel separations of multiple (>2) subpopulations from a heterogeneous background, and label-free. Additionally, in contrast to many other separation techniques, IDS leverages physical interactions between particles as they are separated to achieve better performance, and it is thus ideally suited to operation at high particle concentrations with correspondingly high throughput (Figure 2A). Finally, using IDS as a tool for cell characterization could identify electrical phenotypes and map them to specific genes. This improved understanding of the relationship between a cell's genotype and its physical properties is critical for developing new screens. We have demonstrated the separation and characterization of particles ranging from polystyrene beads, to the budding yeast *Saccharomyces cerevisiae*, to mouse pro B cells (Figure 2B), representing three orders of magnitude in particle volume (~1-1000 μm^3) and conductivity (~0.001–1 S/m) [5].

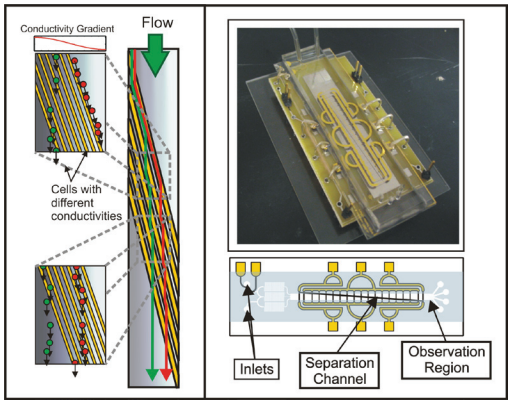


FIGURE 1: (Left) Illustration of IDS, depicting cells with different electric properties following different trajectories in a conductivity gradient. (Top right) Photograph of an assembled device. (Bottom right) Schematic of the device highlighting its primary components.

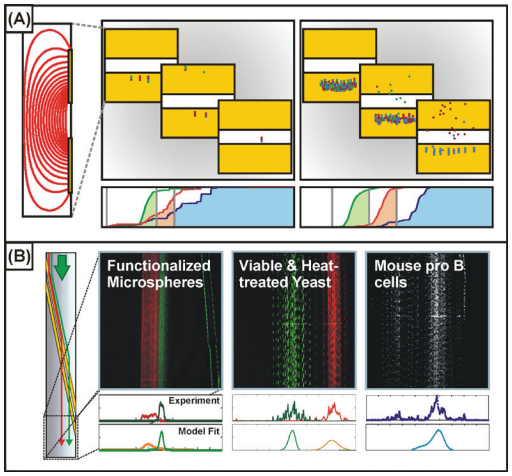


FIGURE 2: (A) Simulation illustrating performance improvement at higher particle concentrations. Larger numbers of particles (right panel) exhibit elution curves with less overlap, indicating higher separation purity. (B) Separation and characterization of cells and particles by measuring the spatial distribution of cells as they exit the device under different conditions.

REFERENCES

[1] H.A. Pohl and J.S. Crane, "Dielectrophoresis of cells," *Biophysical Journal*, vol. 11, pp. 711-727, 1971.

[2] M.D. Vahey and J. Voldman, "An Equilibrium Method for Continuous-Flow Cell Sorting Using Dielectrophoresis," *Analytical Chemistry*, vol. 80, no. 9, pp. 3135-3143, 2008..

[3] M.D. Vahey and J. Voldman, "Iso-dielectric Separation: A new method for the continuous-flow screening of cells," *Micro Total Analysis Systems '06,* vol. 2, pp. 1058-1060, 2006.

[4] P.R.C. Gascoyne and J. Vykoukal, "Particle Separation by Dielectrophoresis," *Electrophoresis,* vol. 23, pp. 1973-1983, 2002.

[5] M.D. Vahey and J. Voldman, "High-Throughput Cell and Particle Characterization Using Isodielectric Separation," Analytical Chemistry, vol. 81, no. 7, pp. 2446-2455.

Fully Integrated Air Pumped Heat Exchanger (PHUMP)

J. Allison, A. Kariya, C. Koveal, D. Jenicek, M. McCarthy, E. N. Wang, J. G. Brisson, J. H. Lang, S. Jacobson
Sponsorship: DARPA, Lockheed Martin

The ever-increasing computational power of modern electronics entails an associated increase in heat generation in the chip; microprocessors without a thermal management system are easily capable of melting themselves. Exotic thermal management systems such as liquid cooling allow high thermal power densities but require large volumes and complex implementations. The Fully Integrated Air-Pumped Heat-Exchanger (PHUMP) heat sink allows this cost-effective technology to keep pace with the cooling demands of the advancing electronics industry.

The PHUMP will provide reduced thermal resistance and reduced power demand in a compact volume. It will be designed to operate in a range of thermal and mechanical shock environments, for an extended period of time. These goals will be achieved by incorporating heat pipes into the extended surface of the heat sink as well as incorporating fan rotors along each wall of the extended surface to maximize heat transfer. Heat pipes are enclosed systems that have a very high effective thermal conductivity by generating a two-phase flow in a working fluid contained within them [1], [2]. The improved heat transfer to the extended surface allows the PHUMP to operate at lower speeds and generate less mass flow than traditional air-cooled heat sinks. This improved heat transfer reduces the power required to turn the fan and allows the PHUMP to achieve high coefficients of performance.

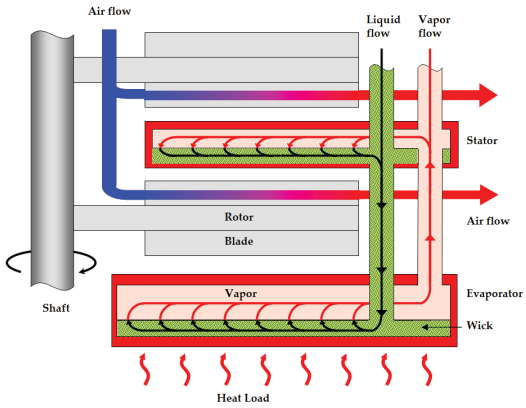


FIGURE 1: Schematic view of one layer of the PHUMP. Air enters axially from above and is blown radially outwards by the fan. Air removes heat from the thermal stators as it passes over them. The stator is the condensing section of a heat pipe whose evaporator is adjacent to the heat load. The condensers and evaporator are connected by vertical pipes.

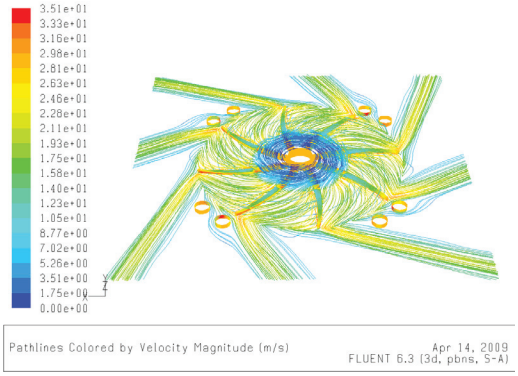


FIGURE 2: A CFD simulation of airflow through a single layer of the PHUMP. Pathlines of airflow are colored by temperature. One rotor with 8 blades is visible, along with sections of the vertical pipes that transfer the working fluid between the condensers and evaporator. Surfaces are colored by static pressure.

REFERENCES

[1] A. Faghri, *Heat Pipe Science and Technology*. Boca Raton: Taylor & Francis Group, 1995.

[2] A. F. Mills, *Heat Transfer.*Upper Saddle River: Prentice Hall, 1999

Model-based Design of MEMS Vibration-energy-harvesters for Wireless Sensors

M. Kim, W. S. Kim, M. Hoegen, S.-H. Kim, B. L. Wardle
Sponsorship: AFOSR, Samsung Fellowship

The recent development of "low power" (10s-100s of μW) sensing and data transmission devices, as well as protocols with which to connect them efficiently into large, dispersed networks of individual wireless nodes, has created a need for a new kind of power source. Embeddable, non-life-limiting power sources are being developed to harvest ambient environmental energy available as mechanical vibrations, fluid motion, radiation, or temperature gradients. While potential applications range from building climate control to homeland security, the application pursued most recently has been that of structural health monitoring (SHM), particularly for aircraft. This SHM application and the power levels required favor the piezoelectric harvesting of ambient vibration energy. Current work focuses on harvesting this energy with MEMS resonant structures of various geometries. Coupled electromechanical models for uniform beam structures have been developed to predict the electrical and mechanical performance obtainable from ambient vibration sources. The optimized models have been verified by comparison to tests on a macro-scale device both without [1] and with a proof mass at the end of the structure (Figure 1) [2]. A non-optimized, uni-morph beam prototype (Figure 2) has been designed and fabricated [3], [4]. Design tools to allow device optimization for a given vibration environment have been under detailed investigation considering various geometries of the device structures and fabrication constraints, especially in microfabrication. Future work will focus on fabrication and testing of optimized uni-morph and proof-of-concept bi-morph prototype beams. System integration and development, including modeling the power electronics, will be included.

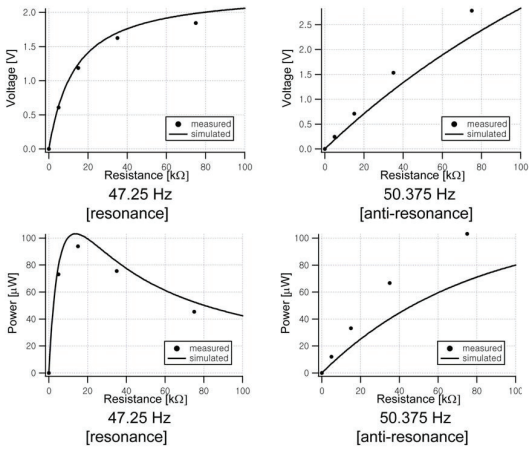


FIGURE 1: Model predictions vs. experimental results: voltage (upper) and power (lower) vs. varying electrical load resistance at resonance and anti-resonance. [2]

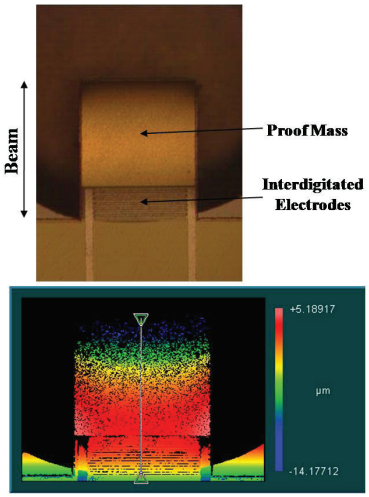


FIGURE 2: Top-down views of fabricated cantilevered MEMS piezoelectric harvester. An SEM of a prototype uni-morph energy harvester device (upper) and ZYGO image of the same device (lower) for curvature measurement.

REFERENCES

[1] N.E. duToit and B.L. Wardle, "Experimental verification of models for microfabricated piezoelectric vibration energy harvesters," *AIAA Journal*, vol. 45, no. 5, May 2007.

[2] M. Kim, M. Hoegen, W. S. Kim, S.-H. Kim, J. Dugundji and B. L. Wardle "Proof mass modeling considerations in cantilevered piezoelectric vibration energy harvesters", *Mater. Res. Soc. Symp. Proc.* vol. 1120, 2009.

[3] N.E. duToit, B.L. Wardle, and S.-G. Kim, "Design considerations for MEMS-scale piezoelectric mechanical vibration energy harvesters," *Integrated Ferroelectrics*, vol. 71, pp. 121-160, 2005.

[4] N.E. duToit and B.L. Wardle, "Performance of microfabricated piezoelectric vibration energy-harvesters," *Integrated Ferroelectrics*, vol. 83, pp.13-23, 2006.

Nanotechnology

Lithographically Defined Isolated CNTs for Field-emission Arrays

S. A. Guerrera, L. F. Velàsquez-Garcìa, A. I. Akinwande
Sponsorship: DARPA

High-current field-emission arrays (FEAs) have garnered much interest in the areas of displays and microwave devices [1]. While most of today's research in field emitters has been performed with field-emission display (FED) applications in mind, there is growing interest in using FEAs as the electron source in high-frequency vacuum electronics to be able to amplify signals extending into the upper millimeter-wave spectral range, where conventional silicon electronics cannot efficiently operate.

State-of-the-art FEAs currently use silicon that has been thinned and sharpened by oxidation to achieve atomically sharp tips or vertically aligned carbon nanotubes (VA-CNTs) [2]-[3] as their emission sources. In the past, the catalyst locations that allow for isolated CNT growth were defined using e-beam lithography and liftoff [4]. However, this method is expensive and low-throughput. Thus, we are moving towards a lithography process that incorporates standard CMOS bulk-processing techniques to attain higher throughput and more repeatable results.

We believe that many field-emitter-array designs are hindered by non-uniform current emission. A central cause of this non-uniform emission could be variations in the radius of each field emitter tip [5]. To combat this variability, we are ballasting each VA-CNT field-emitter tip by incorporating a high-aspect-ratio silicon pillar into each emitter. The current in the silicon pillar saturates at high drain-to-source voltages, resulting in current-voltage characteristics similar to that of an ungated FET. The current source-like behavior of the silicon pillar prevents destructive joule heating in the sharper tips while still allowing duller tips to emit, potentially leading to higher overall current emission, better uniformity, and higher reliability.

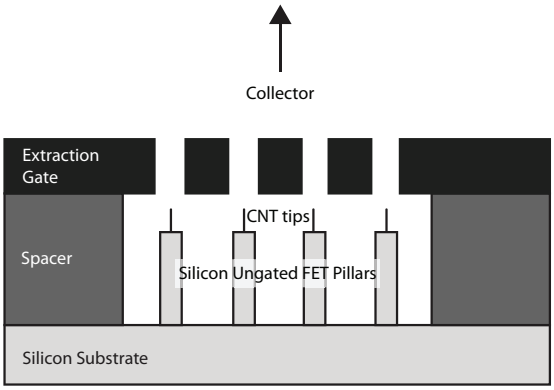


FIGURE 1: Schematic diagram of the CNT field emitters with ballasting ungated FETs.

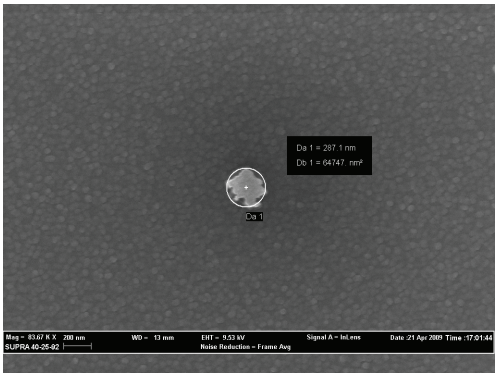


FIGURE 2: One CNT catalyst dot on silicon before etching, part of a 388x888 array with 10µm spacing. The dot is sized such that isolated CNTs will be formed.

REFERENCES

[1] C.A. Spindt, "Field-emitter array development for high frequency applications," IEDM 95-939, 1995.

[2] R.B. Marcus et al., "Atomically sharp silicon and metal field emitters," IEEE Transactions on Electron Devices 38, no. 10, 1991.

[3] L.F. Velàsquez-Garcìa and A.I. Akinwande, "Fabrication of large arrays of high-aspect-ratio single-crystal silicon columns with isolated vertically aligned multi-walled carbon nanotube tips," Nanotechnology 19, no. 40, 2008.

[4] L-Y Chen, "Double-gated isolate vertically aligned carbon nanofiber field emission and field ionization arrays," Ph.D. dissertation, Massachusetts Institute of Technology, Cambridge, MA, 2007.

[5] M. Ding, G. Sha, and A.I. Akinwande, "Silicon field emission arrays with atomically sharp tips: turn-on voltage and the effect of tip radius distribution," IEEE Transactions on Electron Devices 49, no. 12, 2002.

PECVD CNT-based Gas Ionizers for Portable Mass Spectrometry

L. F. Velásquez-García, A. I. Akinwande
Sponsorship: DARPA

MEMS-based analytical instrumentation has been actively researched for over a decade. In particular, efforts have focused on developing rugged gas chromatography and mass spectrometry (GC/MS) systems that are smaller, lighter, cheaper, faster, and more power-efficient [1]. Pumping requirements drive the power consumption, size, and weight of these systems. Therefore, relaxation of the pressure level at which the system components can operate would enable its portability. Portable GC/MS systems, either as individual units or as parts of massive networks, can be used in a wide range of applications including *in-situ* geological survey, law enforcement, environmental monitoring, and space exploration [2]-[3].

The ionizer is a core component of an MS system. We report the fabrication and experimental characterization of a novel low-cost carbon nanotube (CNT)-based electron-impact ionizer (EII) with an integrated gate for portable mass-spectrometry applications. The device achieves low-voltage ionization using sparse forests of plasma-enhanced chemical-vapor-deposited (PECVD) CNT field-emitter tips, and a proximal gate with open apertures to facilitate electron transmission. The gate is integrated using a deep-reactive-ion-etched (DRIE) spring-based high-voltage MEMS packaging technology [4]-[5]. The device also includes a high aspect-ratio silicon structure (μfoam) that facilitates sparse CNT growth and limits the electron current per emitter [6]. The devices were tested as field emitters in a high vacuum (10^{-8} Torr). Electron emission starts at a gate voltage of 110 V and reaches a current of 9 uA at 250 V (2.25 mW) with more than 55% of the electrons transmitted through the gate apertures. The devices were also tested as electron-impact-ionizers using Argon. The experimental data demonstrate that CNT-EIIs can operate at mtorr-level pressures while delivering 60 nA of ion current at 250 V with about 1% ionization efficiency. Figure 1 shows a cross-section schematic and a picture of a fabricated ionizer; Figure 2 shows experimental data that demonstrate that the ionizers work as described by the electron-impact-ionization model.

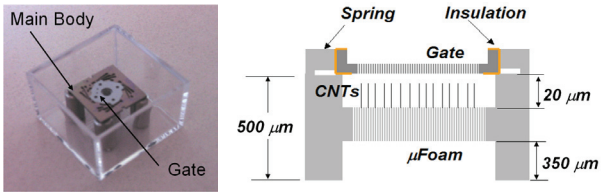


FIGURE 1: A fabricated PECVD CNT-based ionizer (left) and cross-section schematic (right).

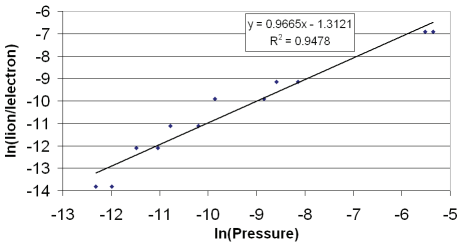


FIGURE 2: Ratio of ion current to electron current vs. pressure. Ideally, the data from electron impact ionization describes a line with slope 1 using a log-log plot. The experimental data describes a line (R^2=0.95) with slope 0.97.

REFERENCES

[1] S. C. Terry et al, "A gas chromatographic air analyzer fabricated on a silicon wafer," in *Proceedings IEEE Trans. Electron Devices*, vol. ED-26, no. 12, pp. 1880–1886, Dec. 1979.

[2] R. R. Reston and E. S. Kolesar, "Miniature gas chromatography system realized using conventional VLSI fabrication techniques applied to quantifying toxic environmental pollutants," in *Proceedings IEEE NAECON*, May 1994, Vol. 1, pp. 327–333.

[3] W. C. Wang, "Micromechanical devices at JPL for space exploration," in *Proceedings IEEE Aerosp. Conf.*, 1998, vol. 1, pp. 461–470.

[4] L. F. Velásquez-García, A. I. Akinwande, and M. Martinez-Sanchez, "Precision Hand Assembly of MEMS Subsystems Using DRIE-Patterned Deflection Spring Structures: An Example of an Out-of-Plane Substrate Assembly", *J. Microelectromech. Syst.*, Vol. 16, No. 3, pp. 598–612, Jun. 2007.

[5] B. Gassend, L. F. Velásquez-García, and A. I. Akinwande, "Precision In-Plane Hand Assembly of Bulk-Microfabricated Components for High Voltage MEMS Arrays Applications", *Journal of Miccroelectromechanical Systems*, Vol. 18, No. 2, pp. 332 – 326, 2009.

[6] L. F. Velásquez-García and A. I. Akinwande, "A PECVD CNT-based open architecture field ionizer for portable mass spectrometry", in *Proceedings IEEE MEMS 2008*, 13-17 Jan. 2008, pp. 742 – 745.

Sub-40-nm Patterning of Au of GaAs for Nanowire Catalysis

J. Leu, M. Brewster, S. Gradečak, K. K. Berggren

Sponsorship: IBM, SRC/FCRP MSD

In this work, we demonstrate sub-40-nm patterning of Au features on GaAs substrates using a bilayer-resist structure. Patterning of small Au features onto GaAs substrates is of particular interest due to their use as metal catalysts for GaAs and GaAs-alloy nanowire growth. Semiconducting nanowires have a variety of potential applications, such as field-effect transistors (FETs) [1], and their size-dependent properties have been exploited for a variety of optoelectronic devices [2]. However, much work remains in creating lithographically-templated nanowires for integration into future manufacturing processes.

Au in particular has shown particular promise in producing oriented, size-selected nanowires [3]. While the patterning of Au features onto other III-V materials, such as InP, has been demonstrated down to 50 nm [4], sub-100-nm patterning of Au on GaAs has not been demonstrated, due to the poor adhesion of Au onto GaAs substrates. Because nanowire diameter exhibits a strong dependence on catalyst particle size [5], the smallest-diameter nanowire that can be grown is limited. With use of a bilayer-resist process and the introduction of a Cr adhesion layer, metal feature sizes under 40 nm were achieved.

The bilayer-resist structures used had a 50-nm-thick top layer of polymethyl methacrylate (PMMA) and a bottom layer of polymethyl glutarimide (PMGI) with thicknesses between 50 and 150 nanometers. The PMMA/PMGI resist stack was exposed by electron-beam lithography, and then the PMMA and PMGI layers were developed in turn. The PMMA layer was first developed by a cold development process [6], and then a controlled undercut was created in the PMGI layer [7]. A metal stack of Au and Cr was evaporated, with the Cr serving as an adhesion layer. Using a 3-nm-thickness of Cr, we were able to create sub-40-nm metal structures. These structures were subsequently used to grow GaAs nanowires by metal-organic chemical-vapor deposition (MOCVD) with diameters as small as 30 nm.

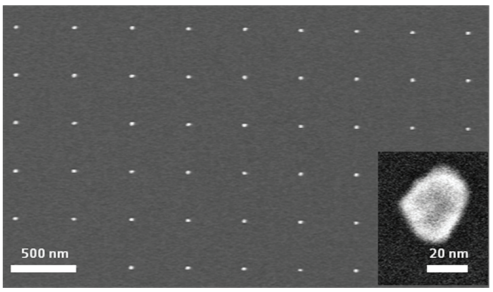


FIGURE 1: An array of sub-40-nm-diameter features consisting of a metal stack of 10-nm Au atop 3-nm Cr on a GaAs substrate, deposited by metal-evaporation onto a patterned PMMA/PMGI bilayer resist stack.

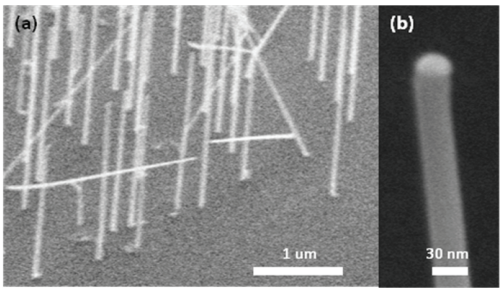


FIGURE 2: (a) An array of GaAs nanowires grown epitaxially by MOCVD, catalyzed by patterned Au/Cr metal features. (b) A 30-nm-diameter GaAs nanowire, with the metal catalyst clearly visible at the top of the nanowire.

REFERENCES

[1] J. Goldberger, A. I. Hochbaum, R. Fan, and P. Yang, "Silicon vertically integrated nanowire field effect transistors," *Nano Letters*, vol. 46, pp. 973-977, May 2006.

[2] X. Duan, Y. Huang, Y. Cui, J. Wang, and C. M. Lieber, "Indium phosphide nanowires as building blocks for nanoscale electronic and optoelectronic devices," *Nature*, vol. 409, pg. 66-69, Jan. 2001.

[3] P. Nguyen, H.T. Ng, and M. Meyyappan, "Catalyst Metal Selection for Synthesis of Inorganic Nanowires," *Advanced Materials*, vol. 17, pp. 1773-1777, July 2005.

[4] T. Mårtensson, M. Borgström, W. Seifert, B. J. Ohlsson, and L. Samuelson, "Fabrication of individually seeded nanowire arrays by vapour-liquid-solid growth," *Nanotechnology*, vol. 14, pp. 1255-1258, Oct. 2003.

[5] Y. Cui, L. J. Lauhon, M. S. Gudiksen, J. Wang, and C. M. Lieber, "Diameter-controlled synthesis of single-crystal silicon nanowires," *Applied Physics Letters*, vol. 78, pp-2214-2216, April 2001.

[6] B. Cord, J. Lutkenhaus, and K. K. Berggren, "Optimal temperature for development of poly (methylmethacrylate)," *J. Vac. Sci. Technol. B*, vol. 25, pp. 2013-2016, Nov. 2007

[7] B. Cord, C. Dames, and K. K. Berggren, "Robust shadow-mask evaporation via lithographically controlled undercut," *J. Vac. Sci. Technol. B*, vol. 24, pp. 3139-3143, Nov. 2006.

High-resolution Lithography with a Focused Helium-ion Beam

D. Winston, B. M. Cord, M. K. Mondol, J. K. W. Yang, K. K. Berggren, {B. Ming, A. E. Vladar, M. T. Postek} (National Institute of Standards and Technology, Gaithersburg, MD), D. C. Bell (Harvard University), {W. F. DiNatale, L. A. Stern} (Carl Zeiss SMT, Peabody, MA)
Sponsorship: NSF GRFP (D. Winston), NSF NNIN, NRI/INDEX

Focused-ion-beam lithography [1] is not as widely practiced as scanning-electron-beam lithography for resist-patterning, in part due to resolution constraints and in part due to substrate sputtering. However, helium ions in particular may enable nanostructure fabrication with higher resolution than electrons. The over-three-orders-of-magnitude higher mass of helium ions relative to electrons should reduce lateral scattering in the resist, thus conceivably enabling patterning of small features at higher density than is possible with electron-beam lithography. Helium ions achieved ~ 200 nm lithographic resolution as early as twenty years ago [2], but only recently has a scanning-helium-ion-beam column been engineered with a focused spot size on par with electron beam columns [3]; the specified spot size of this commercial system is below 1 nm. We have used a commercial scanning helium-ion microscope to demonstrate lithography of hydrogen silsesquioxane (HSQ) on silicon. The HSQ is already used as a high-resolution electron-beam resist [4], and it permits high-resolution inspection after development in a scanning-electron microscope without requiring pattern transfer. As shown in Figure 1 and Figure 2, sub-20-nm feature sizes were achieved.

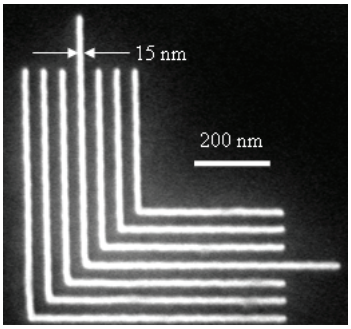


FIGURE 1: Scanning-electron micrograph of 46-nm-pitch nested "Ls," patterned in a 30-nm-thick layer of HSQ on silicon.

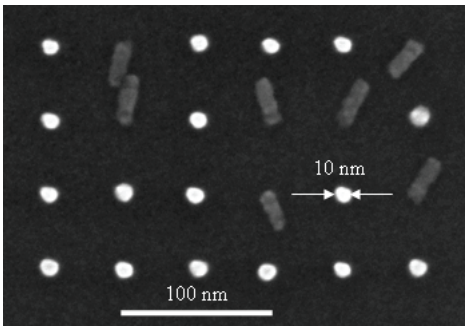


FIGURE 2: Scanning-electron micrograph of a 46-nm-pitch pillar array, patterned in a 30-nm-thick layer of HSQ on silicon. This image was chosen to show the pillars' 3:1 aspect ratio and good edge profile, as some of them have fallen. Exposing with a higher dose prevents pillar collapse.

REFERENCES

[1] J. Melngailis, "Focused ion beam lithography," in Eighth International Conference on Ion Beam Modification of Materials, 1993, pp. 1271-80.

[2] K. Horiuchi, T. Itakura and H. Ishikawa, "Fine pattern lithography using a helium field ion source," in 31st International Symposium on Electron, Ion, and Photon Beams, 1988, pp. 241-4.

[3] B. W. Ward, J. A. Notte and N. P. Economou, "Helium ion microscope: a new tool for nanoscale microscopy and metrology," Journal of Vacuum Science & Technology B (Microelectronics and Nanometer Structures), vol. 24, pp. 2871-4, 11. 2006.

[4] J. K. W. Yang and K. K. Berggren, "Using high-contrast salty development of hydrogen silsesquioxane for sub-10-nm half-pitch lithography," Journal of Vacuum Science & Technology B (Microelectronics and Nanometer Structures), vol. 25, pp. 2025-9, 11. 2007.

Controlled Self-assembly of Linear Structures for Nanoscale-device Fabrication

J. K. W. Yang, Y. S. Jung, J. Chang, C. A. Ross, K. K. Berggren
Sponsorship: NRI/INDEX, ONR

Electron-beam lithography (EBL) has sub-10-nm patterning performance with good pattern registration. However, it is slow and not economical for patterning dense structures over large areas. Alternatively, block-copolymer (BCP) self-assembly can form nanostructures economically and in parallel over large areas, but it lacks global registration. Fortunately, EBL can be combined with BCP self-assembly to overcome their collective shortcomings. The result is a nano-manufacturing approach that achieves high resolution, registration accuracy, and throughput. This approach was demonstrated previously using sparse arrays of EBL-patterned templates to guide BCPs into ordered periodic structures [1-3]. However, periodic structures have limited utility, and one needs controlled but arbitrary patterns in device fabrication.

Here, we controlled cylindrical morphology BCP into line structures that resembled integrated-circuit interconnects and dense nanowire arrays. In addition to achieving long-range order, we were also able to direct the local orientation of individual BCP microdomains into various geometries. In the examples shown here, the structures were made with an effective increase in throughput, as the EBL exposed only a fraction of the patterns and the BCP completed the missing structures.

Without a guiding template, the BCP lines were locally ordered but globally disordered. To achieve global ordering, we used a template consisting of a sparse array of nanoposts fabricated by EBL patterning of hydrogen silsesquioxane (HSQ) resist [4]. As shown in Figure 1, an array of EBL-patterned HSQ nanoposts (bright dots) arranged in a rectangular array successfully guided a subsequently applied film of PS-PDMS BCP into well-ordered lines. The different orientations of the lines were achieved by increasing the spacings between the posts in the template.

To achieve arbitrary pattern formation, we broke the symmetry of the template by using "dash" structures instead of circular posts, and strategic positioning of the posts. Figure 2A shows that an array of dashes was able to guide the BCP into accurately-positioned bends. Furthermore, as shown in Figure 2C, we were able to locally control individual BCP microdomains into meandering lines by strategic positioning of posts. The resulting well-controlled linear structures have potential for use in the fabrication of integrated circuit interconnects and dense nanowire arrays.

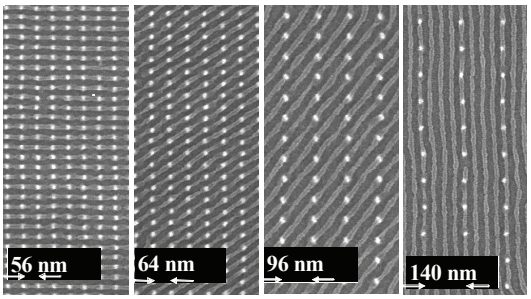


FIGURE 1: An SEM of the self-assembly of cylindrical-phase block copolymers (BCP) that were guided by an electron-beam-patterned template of HSQ nanoposts (bright dots) to form ordered gratings of lines. The progression of grating orientations from horizontal to vertical from left to right occurred due to the tendency of the BCP to preserve its natural period of ~35 nm even as the template-spacing was increased.

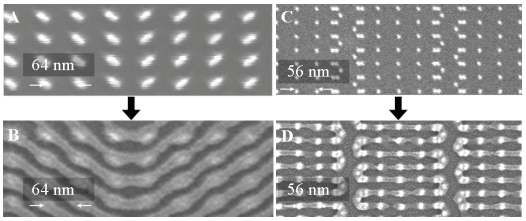


FIGURE 2: (A) An SEM of a template consisting of dashes arranged such that the BCP that aligns along the dashes will form bends as shown in (B). (C) An SEM of a template consisting of an arrangement of posts designed to guide the BCP into an array of meandering structures as shown in (D).

REFERENCES

[1] I. Bita, J. K. W. Yang, Y. S. Jung, C. A. Ross, E. L. Thomas, and K. K. Berggren, "Graphoepitaxy of self-assembled block copolymers on two-dimensional periodic patterned templates," *Science*, vol. 321, pp. 939-943, 2008.

[2] R. Ruiz, H. M. Kang, F. A. Detcheverry, E. Dobisz, D. S. Kercher, T. R. Albrecht, J. J. de Pablo, and P. F. Nealey, "Density multiplication and improved lithography by directed block copolymer assembly," *Science*, vol. 321, pp. 936-939, 2008.

[3] J. Y. Cheng, C. T. Rettner, D. P. Sanders, H. C. Kim, and W. D. Hinsberg, "Dense self-assembly on sparse chemical patterns: Rectifying and multiplying lithographic patterns using block copolymers," *Advanced Materials*, vol. 20, pp. 3155-3158, 2008.

[4] J. K. W. Yang and K. K. Berggren, "Using high-contrast salty development of hydrogen silsesquioxane for sub-10-nm half-pitch lithography," *Journal of Vacuum Science & Technology*, vol. 25, pp. 2025-2029, 2007.

Understanding Hydrogen Silsesquioxane Resist for Sub-5-nm Half-pitch Electron-beam Lithography

J. K. W. Yang, B. Cord, J. Klingfus, J. Chang, S. Nam, K. Kim, M. J. Rooks, K. K. Berggren
Sponsorship: NRI/INDEX, INSIC

Electron-beam lithography (EBL) provides one of the highest achievable patterning resolutions. As demonstrated by electron-beam induced deposition (EBID) methods, patterns as small as 1.6-nm-half-pitch can be achieved [1]. However, EBID methods are typically orders of magnitude slower, due to the high exposure doses required, and less reproducible than resist-based processes. Therefore, EBID is less practical in patterning high-resolution structures over large areas.

On the other hand, the resist-based process using EBL exposure of hydrogen silsesquioxane (HSQ) resist is a promising approach for patterning high-resolution structures due to its higher speed (compared to EBID) and the high etch-resistance of HSQ. In the past, we demonstrated the patterning of 7-nm-half-pitch structures using this process followed by a high-contrast salty-development step [2]. However, the development mechanism of HSQ was not well understood.

Here, we report on progress in understanding the contrast enhancement mechanism in HSQ and demonstrate 4.5-nm half-pitch structures using this resist-based process. Figure 1 shows a SEM of 4.5-nm half-pitch nested-"L" structures patterned using Raith's latest EBL tool, the Raith 150TWO at 10 kV acceleration voltage in 10 nm-thick HSQ resist. Patterning at 10 kV instead of higher acceleration voltages sped-up our exposures without significant loss in resolution. To the best of our knowledge, this is the highest resolution achieved using resist-based EBL to date.

The development of HSQ is self-limiting, i.e., development stops beyond a certain development time. This self-limiting nature of the development process often results in footing between closely spaced structures and limits resolution. However, as shown in Figure 2, the addition of NaCl salt to the NaOH developer appears to allow continued resist development, which resulted in further contrast enhancement with increasing development time. This effect was not seen in development in NaOH alone without salt.

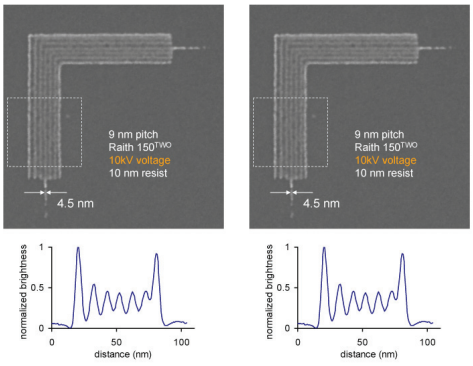


FIGURE 1: (Left) An SEM of 4.5-nm-half-pitch nested-"L" structures patterned using a Raith 150TWO EBL at 10 kV acceleration voltage in 10-nm-thick HSQ. (Right) The plots of normalized brightness vs. distance at the bottom of both images were obtained by averaging the brightness values of the SEM image along the length of the HSQ lines within the dashed rectangles shown.

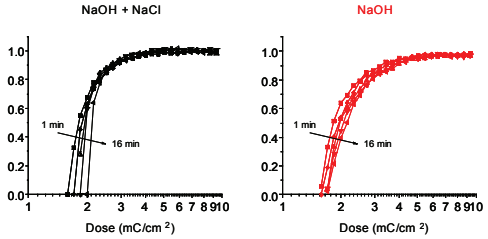


FIGURE 2: Contrast curves for HSQ developed in 1% wt NaOH, 4% wt NaCl solution for HSQ exposed by 100 keV energy electrons and developed for 1, 2, 4, 8, and 16 mins. Plots show improvement in contrast with increasing development time. The addition of salt appears to enable continued development.

REFERENCES

[1] W. F. van Dorp, B. van Someren, C. W. Hagen, and P. Kruit, "Approaching the resolution limit of nanometer-scale electron beam-induced deposition," *Nano Letters*, vol. 5, pp. 1303-1307, 2005.

[2] J. K. W. Yang and K. K. Berggren, "Using high-contrast salty development of hydrogen silsesquioxane for sub-10-nm half-pitch lithography," *Journal of Vacuum Science & Technology*, vol. 25, pp. 2025-2029, 2007.

Advanced Planarization Technology

J. Johnson, W. Fan, D. S. Boning

Sponsorship: SEMATECH/SRC Engineering Research Center for Environmentally Benign Semiconductor Manufacturing, National Semiconductor, JSR

Benchmark modeling work has been conducted in the Boning Group investigating a critical and costly process in silicon integrated circuit (IC) fabrication process. chemical mechanical polishing or planarization (CMP). However, challenging device dimensions, novel materials, and advanced toolsets call for a deeper level of physical understanding and more empirically sensitive models. Therefore, two transformative approaches to better understanding and modeling of CMP have been undertaken.

First, die-level modeling of STI CMP using novel slurries like Ceria are currently being explored. However, in experiments using traditional Silica slurries, more effective ways of modeling have been discovered. Pattern-density models in the Boning Group have evolved; however, none of these models have explored the evolution of pattern density itself. Current work is seeking to model the change in pattern density and deposition profiles as a response to step-height reduction over time in order to enhance the model specificity and, consequently, accuracy. We believe that pattern density will increase parabolically as the step height decreases (i.e., time increases), and have proved this experimentally as shown in Figure 1.

Second, previous assumptions that the CMP pad surface has the same Young's modulus as the bulk were reassessed. Comparison of the most current CMP model with the direct measurement of a JSR pad shows that the model's extracted bulk modulus proved to be on the order of five times higher than the actual measured result. In order to attribute this discrepancy to either a high surface modulus or a high bulk Poisson's ratio, a preliminary experimental study was performed using nanoindentation measurement techniques as shown in Figure 2. Current work is exploring the statistical confidence of the technique and its incorporation of the proper modulus towards a more physically accurate die-level CMP model.

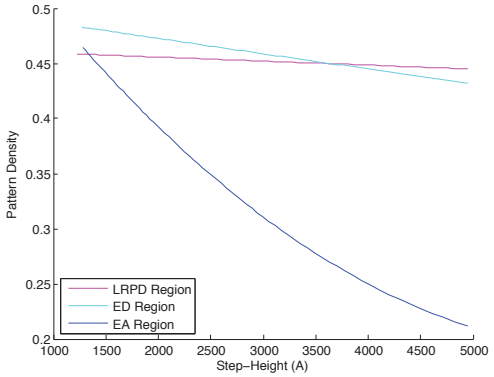


FIGURE 1: Local pattern density, ρ, as a function of step height, h, observed a decrease of almost 40% over the course of the STI CMP process in areas with structures <10μm in length.

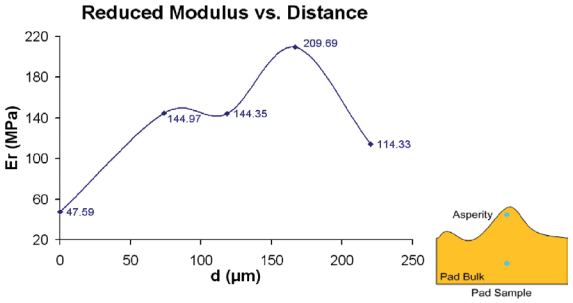


FIGURE 2: The first successful scan of nanoindentation on a JSR pad follows the hypothesized trend of pad asperity effective modulus being significantly less than that of the pad bulk effective modulus.

REFERENCES

[1] X. Xie, "Physical Understanding and Modeling of Chemical Mechanical Planarization in Dielectric Materials," PhD thesis, Massachusetts Institute of Technology, Cambridge, MA, 2007.

Modeling of Nanoimprint Lithography

H. K. Taylor, D. S. Boning

Sponsorship: Singapore-MIT Alliance

Nanoimprint lithography (NIL) enjoys growing interest, particularly for the fabrication of bit-patterned hard disk drives and solid-state memories. In NIL, a thermoplastic or ultraviolet-curing resist material is imprinted with a re-usable stamp. Full adoption of the technique is difficult to envisage without reliable methods for simulating the parasitic elastic distortions of the stamp that occur during imprinting, as well as for predicting any locations of incomplete pattern replication. Conventional mechanical simulation techniques are far too slow to extend to the feature-rich patterns of complete devices. Building on our earlier work simulating pattern dependencies in thermoplastic micro-embossing [1], [2], we are developing a computationally inexpensive method for simulating NIL.

Our work currently models the imprinting of spun-on thermoplastic resists and is being extended to the so-called "step-and-flash" ultraviolet-curing variant of nanoimprint. We describe the mechanical behaviors of the resist and the stamp using the responses of their surface profiles to a normally-applied impulse in space and in time. The overall topography of the resist for any given stamp pattern is predicted through a series of steps in which the resist's impulse response is convolved with an iteratively-found estimate of the time-evolving stamp–resist contact-pressure distribution. Preliminary experiments conducted in the MTL show that the method successfully captures key pattern interactions at the micron scale (Figure 1) [3]. A simple modification of the simulation method has shown promise for modeling the shear-thinning resist behavior that can occur in NIL (Figure 2). Using this simulation method, we expect to be able to explore a set of design-correction strategies with the aim of reducing parasitic stamp deflections. We are currently seeking to calibrate the method for a range of nanoimprint resist materials and to this end are keen to work with any interested industrial NIL users.

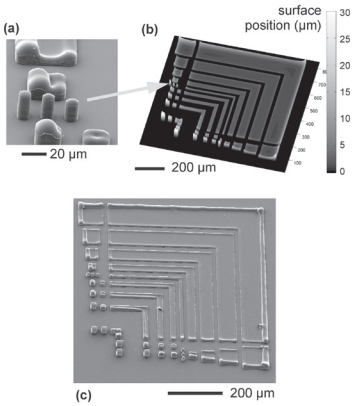


FIGURE 1: Comparison of experiment with simulation in the micron-scale embossing of a 2.2-μm polysulfone layer, spun onto silicon. Embossing was performed at 205 °C under 30 MPa for 2 minutes. Scanning electron micrographs of the sample (a, c) and a 3-D plot of the simulated topography (b) show close agreement.

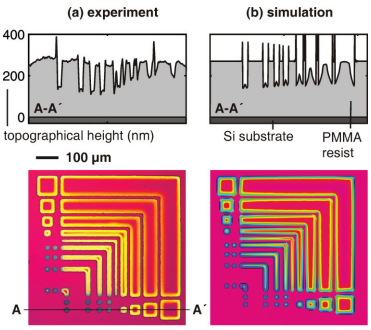


FIGURE 2: Comparison of experiment (a) with simulation (b) in the micron-scale embossing of a 270-nm-thick PMMA layer, spun onto silicon. Embossing was performed at 165 °C under 40 MPa for 2 minutes. Optical interferograms (lower) and cross-sections (upper) are shown. The experimental cross-section was obtained, using white-light interferometry, from an elastomeric casting of the imprinted layer. The simulation incorporates elastic deflections of the silicon stamp and shear-thinning of the PMMA resist.

REFERENCES

[1] H. Taylor, D. Boning, C. Iliescu, and B. Chen, "Computationally efficient modelling of pattern dependencies in the micro-embossing of thermoplastic polymers," *Microelectronic Engineering*, vol. 85, 2008, pp. 1453-6.

[2] H. Taylor, Y.C. Lam, and D. Boning, "A computationally simple method for simulating the micro-embossing of thermoplastic polymers," *Journal of Micromechanics and Microengineering*, vol. 19, no. 7, p. 075007 (16 pp), July 2009.

[3] H. Taylor, C. Iliescu, M. Ni, C. Xing, Y.C. Lam, and D. Boning, "Modeling pattern dependencies in the micron-scale embossing of polymeric layers," *Micro- and Nanotechnology: Materials, Processes, Packaging, and Systems IV*, Melbourne, Australia: SPIE, 2008, pp. 726909-15.

Carbon Nano-switches for Low-leakage Circuit Applications

K. M. Milaninia, C. E. Schmitt, L. F. Velásquez-García, A. I. Akinwande, M. A. Baldo, A. P. Chandrakasan
Sponsorship: SRC/FCRP IFC, DARPA

Nanoelectromechanical switches (NEMS) exhibit minimal leakage current in the off state. Consequently, they may find application in low-power electronics. This work focuses on the fabrication of a vertically oriented nano-switch using a carbon fiber or nanotube as the active component. Figure 1 shows the device schematic, and Figure 2 shows an SEM image of a fabricated nano-switch. The device consists of a line of carbon nanofibers grown directly on a highly doped silicon substrate between two contacts that are electrically isolated from the substrate by an insulator. The device is actuated when a voltage is applied between the substrate and one of the contacts. This voltage causes the nanofibers to be pulled into and eventually make physical contact with one of the contacts, which allows current to flow between the substrate and the contact.

One of the primary benefits of the nano-switch is that it has extremely low leakage current because a physical gap separates the nanotube from the contact during the off state. One possible application that takes advantage of the reduced leakage is power-gating idle circuit blocks. The nano-switch is connected as a header switch between the power supply and the load circuit. During normal operation, the nano-switch acts as a short circuit and power is supplied to the load circuit. When the circuit is not in use, the nano-switch is opened and the supply voltage is disconnected to reduce power consumption. This technique is similar to power-gating with a high threshold CMOS device, but the nano-switch provides extra power savings because it has even less leakage current.

A CMOS test chip has been designed to quantify the power savings of the nano-switch for this power-gating application. The chip also implements proof-of-concept SRAM and reconfigurable interconnect circuits that explore other potential benefits of the nano-switch. The basic device fabrication process has been developed, and the nano-switches are currently being optimized for performance.

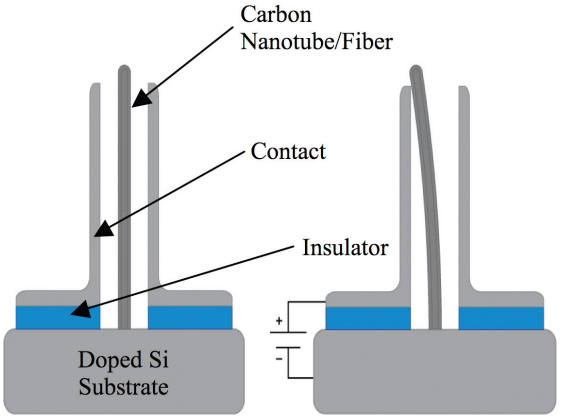


FIGURE 1: Left) Schematic of a vertically oriented carbon nano-switch. Right) Carbon nano-switch upon actuation using an applied voltage between the substrate (i.e., tube) and a contact.

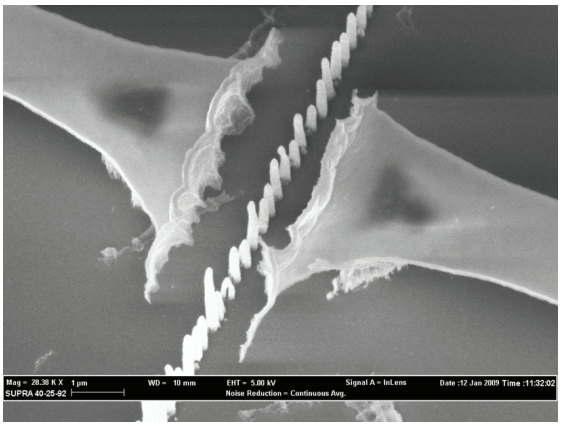


FIGURE 2: An SEM image of a fabricated carbon nanofiber-based nano-switch.

REFERENCES

[1] L.-Y. Chen, L.-F. Velasquez-Garcia, X. Wang, K. Teo, and A.-I. Akinwande, "A micro ionizer for portable mass spectrometers using double-gated isolated vertically aligned carbon nanofiber arrays," in Proc. International Electron Devices Meeting, 2007, pp. 843-846.

Control of Carbon Nanotube Geometry via Tunable Process Parameters

M. A. Cullinan, M. L. Culpepper
Sponsorship: Chang Innovation Grant, Pappalardo Fellowship

Carbon nanotubes (CNTs) are well–suited for use in flexure-based nanomechanical devices because CNTs possess both a high elastic modulus (~1 TPa) and failure strains of up to 40%. These properties, combined with CNTs' low mass-per-unit volume, make it possible for CNT–based devices to exhibit three characteristics that are useful in nano–scale devices: (1) vibration frequencies in lateral bending that may exceed of 10s of GHz, (2) high energy storage per unit mass, and (3) large ranges of motion relative to their size. In this research we created a growth model that was generated via statistical and experimental analysis. Using this growth model, a method was created for selecting fabrication process parameters that may be used to grow carbon nanotubes with a specified outside diameter and number of walls. The diameter and number of walls are controlled by adjusting several growth parameters: temperature, catalyst film thickness, and hydrocarbon concentration. Figure 1 shows the results of the CNT growth for one set of process parameters; Figure 2 shows the relationship between CNT diameter and wall thickness for a variety of process parameters. The capability to control diameter and number of walls enables the control of rigidity, which in turn makes it possible to control a CNT's lateral vibration behavior and bending stiffness. The growth model was therefore used to design growth process for specific applications. Experimental results showed that the models predicted average outside diameter and number of walls within the growth with less than 6% and 7% error, respectively. Based on the measured geometries, it was estimated that the stiffness and natural frequency can be accurately controlled to within 1.5% of the desired values.

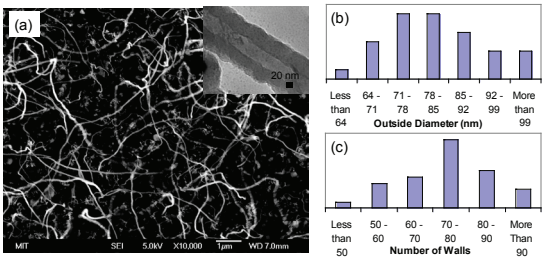


FIGURE 1: (A) SEM image with inset TEM image of sample from run 15 with F = 3nm, T = 800°C, and Cm = 68.5%. (B) Histogram of CNT outside diameter for run 15. (C) Histogram of number of walls in CNT for run 15.

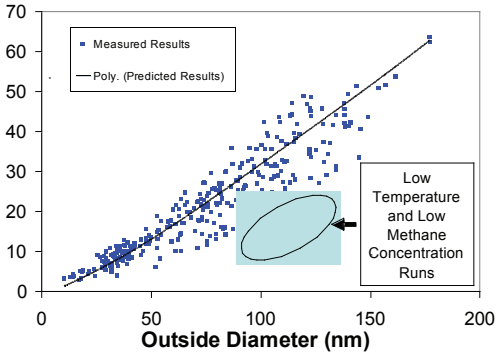


FIGURE 2: Model predictions vs. measured values for CNT growth.

Towards Controlled Doping in III-V Semiconductor Nanowires

M J. Tambe, M. J. Smith, S. Gradečak
Sponsorship: NSF, MITEI, MTL

Nanowires are quasi-one-dimensional single crystals with lateral dimensions that can be scaled-down to only a few nanometers. They can simultaneously act as active components and interconnects and therefore fulfill the two basic functions of any active device. However, controlled doping of III-V nanowires is challenging due to strong Fermi-level pinning as well as the kinetic and thermodynamic requirements for dopant incorporation through the metal catalyst. To enable flexible and controllable doping of nanowires we are studying two doping approaches: doping through the deposition of a doped epitaxial shell around the nanowire [1] and *ex-situ* post-growth diffusion doping. Here we concentrate on GaAs nanowires as a model system, although our approaches are applicable to other III-V nanowires.

Shell doping is proposed as a simple *in-situ* doping method. After GaAs nanowires are grown at 420°C, the reactor temperature is increased to 750°C and silane is introduced during the growth of a conformal GaAs shell, as shown in Figure 1a. Experiments have shown that uniform shells can be achieved, as shown in Figure 1b. To overcome Fermi-level pinning, the shells must be thick and/or heavily doped. Schrödinger-Poisson models predict that at $N_D = 10^{18} cm^{-3}$, the minimum shell thickness to achieve doping is 48nm. Experimental studies to validate this prediction and determine the dependence of carrier concentration on shell thickness are currently in progress. We have optimized the design and fabrication of robust, Ohmic electrical contacts onto GaAs nanowires with sufficiently low contact resistance. The contacts are patterned using e-beam lithography followed by e-beam evaporation of Ni(20 nm), Ge (20 nm), and then Au (120 nm). The contacts are then annealed at 420°C for 30 seconds.

To achieve precise control over diffusion doping at the nanoscale, we propose a platform for finely tunable dopant dosages via the creation of a monolayer of dopant-containing molecules [2] on GaAs. First, the GaAs surface is hydrolyzed [3] to create reactive sites for monolayer formation. A controlled dose of silicon is introduced by reacting (3-Mercapto-propyl) trimethoxysiloxane (MPTMS) with the hydroxyl groups on the surface (Figure 2). Silicon atoms are then driven in by a rapid thermal anneal. X-ray Photoelectron Spectroscopy analysis supports the proposed surface functionalization. Preliminary sheet resistance measurements suggest that this platform can be used to dope GaAs. An investigation of dopant dosage control is underway.

REFERENCES

[1] H. – Y. Li. O. Wunnicke, M. T. Borgstrom, W. G. G. Immink, M. H. M. van Weert, M. A. Verheijen and E. P. A. M.Bakkers, "Remote p-doping of InAs nanowires," *Nano Letters*, vol. 7, pp. 1144-1148, May 2007.

[2] Ho, J. C., R. Yerushalmi, et al. (2008). "Controlled nanoscale doping of semiconductors via molecular monolayers," *Nature Materials*, vol. 7, pp. 62-67, Jan. 2008.

[3] Gallo, P., B. Viallet, et al. (2005). "Efficient aminosilane adhesion promoter for soft nanoimprint on GaAs," *Applied Physics Letter*, vol. 87, pp.183111:1-2, Oct. 2005.

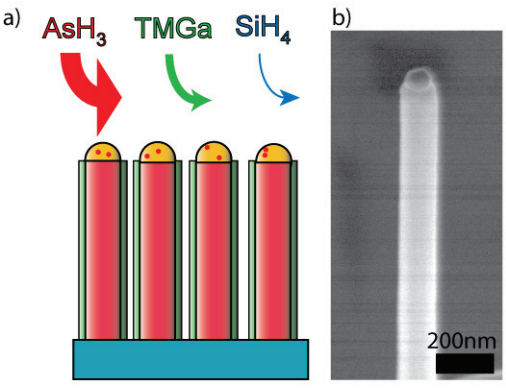


FIGURE 1: a) Schematic of shell doping via co-introduction of silence during epitaxial shell deposition. b) An SEM image of shell-doped GaAs NW. The dark object on the top of the nanowire is the Au catalyst nanoparticle.

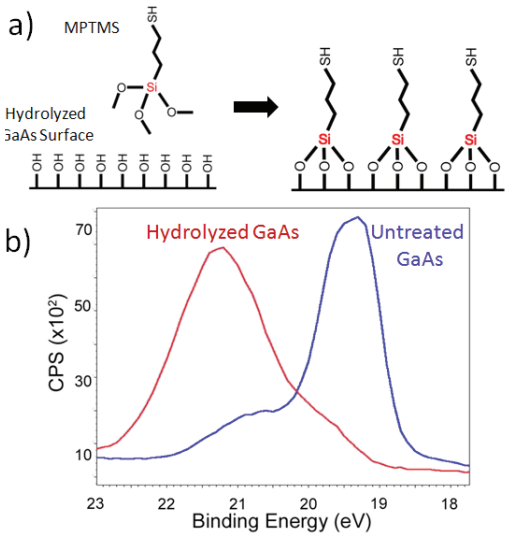


FIGURE 2: a) Idealized reaction between MPTMS and hydrolyzed GaAs. Silicon, the n-type dopant, is highlighted in red. b) X-ray Photoelectron Spectroscopy peak shifts suggest a hydrolyzed GaAs surface.

Supercritical Microfluidic Synthesis of Nanomaterials

S. Basak, S. Marre, J. Bake, M. Bawendi, K. F. Jensen
Sponsorship: NSF, ARO – ISN

Nano-sized materials are of interest for modern technological applications such as reinforced lightweight materials, catalysts, sensors, fuel cells, and medical diagnosis and treatments due to improved chemical, mechanical, optical and functional properties compared to bulk materials. Significant effort has been focused on the ability to control the nanoscale structures via innovative synthetic approaches. Synthesis of nano-sized specialty materials using a multistep batch process suffers from problems in reproducibility of size, size distribution, and purity. Under such situations, the challenge is to find alternate methods or make improvements in the existing processes.

Continuous laminar flow reactors based on microfluidics, integrated with fluid flow, heat, and pressure control elements offer a solution to these problems as well as additional advantages, including feedback control of temperature and feed streams, reproducibility, potential for *in situ* detection for reaction monitoring, rapid screening of parameters, and low reagent consumption during optimization. We have demonstrated a continuous supercritical microfluidic method for synthesis of nanosized oxide materials (Figure 1). Decomposition of iron pentacarbonyl in hexane to produce iron oxide under 70 bar pressure and between 220 – 300°C temperature is studied as a model system. Oleic acid and lauric acid are used as surfactant to reduce the agglomeration of nanoparticles inside the reactor channels. At operating pressure, the solvent hexane turns supercritical above 234°C. The supercritical hexane provides a better control over the particle size distribution and morphology, which makes this technology advantageous compared with conventional techniques.

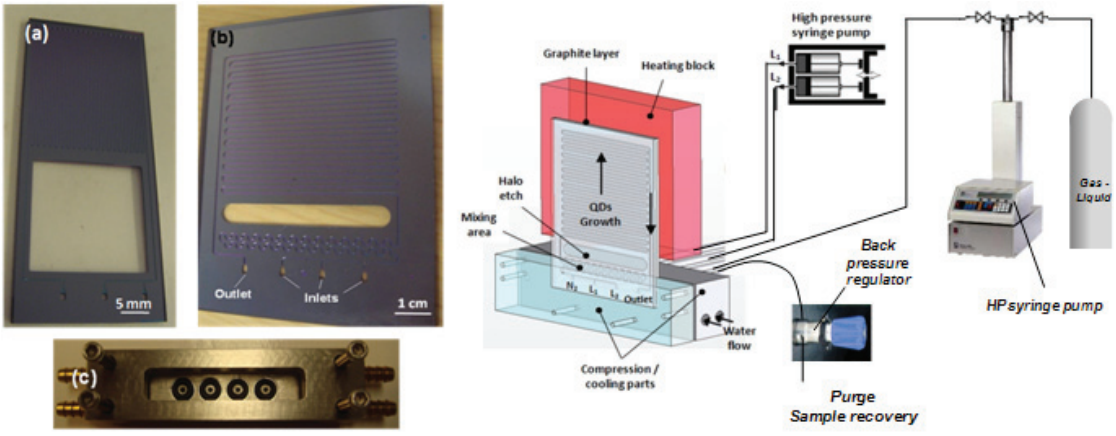


FIGURE 1: Left: High-pressure microreactors for nanomaterials synthesis: (a) 45-µL microreactor, (b) 100-µL microreactor and (c) modular high-pressure fluidic connections. Right: High-pressure experimental set-up including a high-pressure, high-temperature microreactor, a compression-cooling aluminum part, two high-pressure syringe pumps, and a back-pressure regulator.

Synthesis of Single-walled Carbon Nanotube Thin Films via Electrostatic-spray-assisted Chemical Vapor-deposition

M. Hofmann, Y. P. Hsieh, J. Kong
Sponsorship: SRC/FCRP IFC, Intel Corporation

In our work, electrostatic-spray-assisted chemical vapor-deposition is used to grow floating single-walled carbon nanotubes and directly deposit nanotube thin films on a substrate.

The catalyst solution was finely dispersed by a strong electrical field and injected into the heated reaction zone during the growth. The size of the aerosol was found to be affected by electrospraying parameters. Carbon nanotubes are nucleating from these aerosols and grow as they travel through the reaction zone. This process offers a versatile test bed for fundamental studies of nanotube growth since the aerosol is found to be unperturbed from substrate interaction and individual carbon nanotubes are produced.

The nanotubes can be efficiently deposited on a cooled sample holder that is reaching into the reaction zone. This result is promising for thin-film application since nanotubes can be deposited on a variety of cooled substrates that are otherwise not compatible with the CVD environment. Finally, the fabrication of free-standing suspended nanotube films was demonstrated.

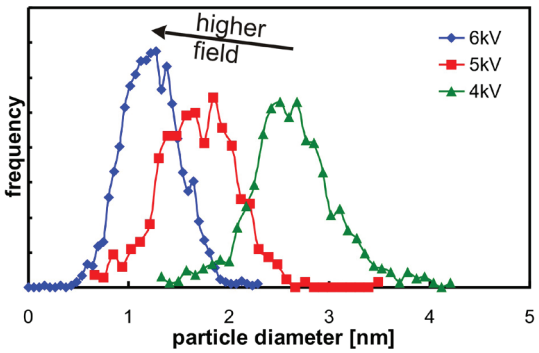


FIGURE 1: Diameter distributions of aerosol generated with different acceleration voltages.

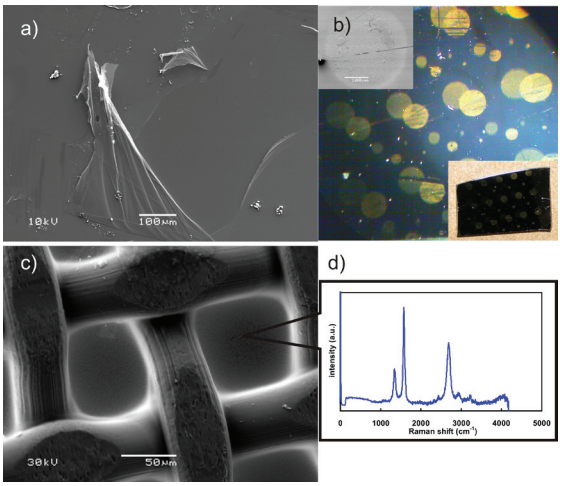


FIGURE 2: a) An SEM image of damage in the continuous CNT film, b) CNT patterns generated by shadow-masking technique, c) SEM image of a suspended nanotube film on stainless steel mesh, and d) Raman spectrum and indication of position obtained.

REFERENCES

[1] Y.-P. Hsieh, M. Hofmann, H. Son, X. Jia, Y.-F. Chen, C.-T. Liang, M.S. Dresselhaus, and J. Kong, "Direct deposition of single-walled carbon nanotube thin films via electrostatic spray assisted chemical vapor deposition," *NANOTECHNOLOGY*, vol. 20, no. 6, pp. 065601, February 2009.

[2] M. Hofmann, "Synthesis of single-walled carbon nanotube thin films via electrostatic spray assisted chemical vapor deposition," presented at *4th Workshop on Nucleation and Growth Mechanisms of Single Wall Carbon Nanotubes*, San Antonio, USA, 2009.

Integrated Graphene Interconnects

K.-J. Lee, A. P. Chandrakasan, J. Kong
Sponsorship: SRC/FCRP IFC

As process technology scales, the importance of material and architectural innovation on interconnect performance will continue to increase. Graphene has gathered much interest as a possible replacement for copper interconnects due to its large carrier mobility and current carrying capacity. Graphene sheets are also an attractive alternative to carbon nanotube-based interconnects as they are more compatible with conventional lithography methods. This project proposes to integrate high-density graphene ribbons and characterize their properties as global interconnects. The main objectives of this project are to achieve high density integration of graphene with CMOS, reduce overall power consumption by low-swing signaling, and characterize the performance (delay, energy, noise, etc.) of graphene interconnects.

This project will focus on low-swing signaling, primarily as a power-reduction technique for on-chip communication. During the design phase, low-swing drivers/receivers will be benchmarked using existing graphene circuit models [1]. Similar to work in [2], graphene sheets are grown on a separate substrate by chemical vapor deposition, and then they are transferred on top of the completed CMOS chip using an adhesion layer. Unlike the integration process of carbon nanotubes [3], the use of graphene enables lithographic patterning, which allows the large graphene sheet to be patterned and etched into mm-length interconnect wires. Bare SiO_2/Si chips have been used as prototypes to fabricate graphene wires up to 1 mm in length, with an effective sheet resistance of 700 – 900 Ohms/sq.

REFERENCES

[1] A. Naeemi and J. Meindl, "Performance benchmarking for graphene nanoribbon, carbon nanotube, and Cu interconnects," in *2008 International Interconnect Technology Conference*, 2008, pp. 183-185.

[2] A. Reina *et al.*, "Large area, few-layer graphene films on arbitrary substrates by chemical vapor deposition," *Nano Letters*, vol. 9, pp. 30-35, Dec. 2008.

[3] G. Close *et al.*, "A 1 GHz integrated circuit with carbon nanotube interconnects and silicon transistors," *Nano Letters*, vol. 8, pp. 706-709, Feb. 2008.

Fabrication of Graphene Nanostructures Using Thermally-activated Nickel Nanoparticles

L. C. Campos, V. R. Manfrinato, J. D. Sanchez-Yamagishi, J. Kong, P. Jarillo-Herrero
Sponsorship: Department of Physics, MIT; Department of Electrical Engineering and Computer Science, MIT; Departamento de Física, Universidade Federal de Minas Gerais; Departamento de Engenharia de Sistemas Eletrônicos, Escola Politécnica, Universidade de São Paulo

Graphene, a single atomic layer of graphite, holds many exciting possibilities for demonstrating new physics as well as novel electronic applications [1], many of which can be realized only by confining graphene into nanoribbons and other nanostructures. When confined on the nanometer scale, the edges of a graphene device play an important role in determining its electronic and magnetic properties. For example, it is predicted that graphene nanoribbons with crystallographically-defined edges could be key to realizing fast ballistic field-effect transistors [2] or room-temperature spintronic devices [3]. To date, though, no effective method to produce single-layer graphene structures with well-defined crystallographic edges has been found.

Our research has focused on this problem, and we have successfully developed the first anisotropic etching process in isolated single-layer graphene. This etching process produces nanoribbons and other continuously connected nanostructures with edges aligned along a single crystallographic-direction. The nanoribbons are obtained in sub-10nm geometries, with edges smooth on the nanometer scale, and they should provide a wealth of interesting new experiments from its unique crystallographic orientation. For example, previous graphene nanoribbon field effect transistors were limited by having disordered edges; since our nanoribbons are aligned along crystallographic directions with smooth edges, they should feature much better FET operation. Moreover, we often obtain nanoribbons and other nanostructures connected in continuous graphene circuits, one example being a nanometer-scale equilateral triangle connected to a series of nanoribbons and other more complicated geometries. Previous studies have worked on tailoring graphene into nanocircuits, but these are the first graphene nanocircuits that can exploit the potential of graphene's edge-physics.

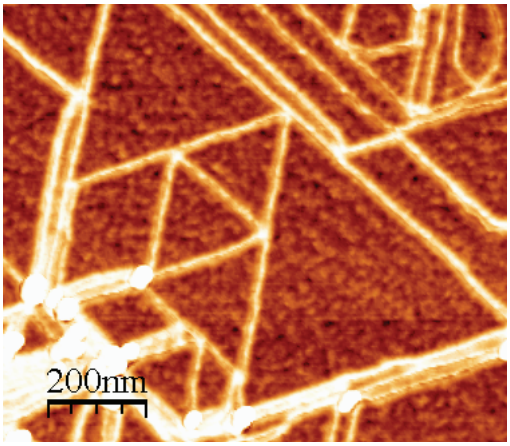


FIGURE 1: An AFM image of the trenches produced by thermally-activated nickel nanoparticles etching across single-layer graphene. The trenches run along straight lines, following a single crystallographic orientation.

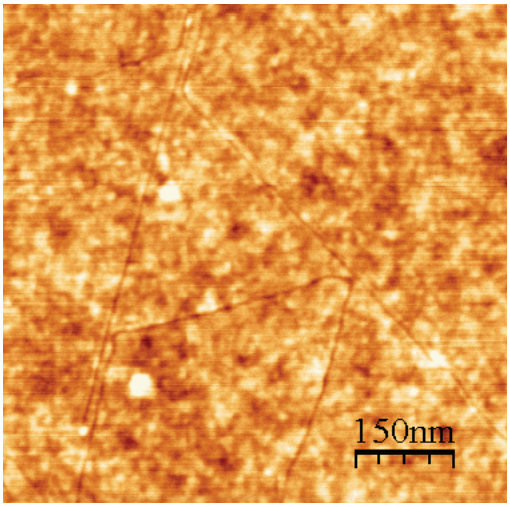


FIGURE 2: Nickel nanoparticles avoid crossing previously etched trenches, producing graphene nanostructures such as equilateral triangles and nanoribbons that should feature interesting electronic properties.

REFERENCES

[1] A. K. Geim and K. S. Novoselov, "The rise of graphene," *Nature Materials*, vol. 6, pp. 183-191, Mar 2007.

[2] D. A. Areshkin, D. Gunlycke, and C. T. White, "Ballistic Transport in Graphene Nanostrips in the Presence of Disorder: Importance of Edge Effects," *Nano Letters*, vol. 7, pp. 204-210, 2007.

[3] Y. W. Son, M. L. Cohen, and S. G. Louie, "Half-metallic graphene nanoribbons," *Nature*, vol. 444, pp. 347-349, 2006.

Templated Self-assembly of Block Copolymers for Nanolithography

C. A. Ross, H. I. Smith, E. L. Thomas, V. Chuang, Y. S. Jung

Sponsorship: NSF, Singapore-MIT Alliance, SRC

Self-organized macromolecular materials can provide an alternative pathway to conventional lithography for the fabrication of devices on the nanometer scale. In particular, the self-assembly of the microdomains of diblock copolymers within lithographically-defined templates to create patterns with long range-order has attracted considerable attention, with the advantages of cost-effectiveness, large-area coverage, and compatibility with pre-established top-down patterning technologies. Block copolymers consist of two covalently bound polymer chains of chemically distinct polymer materials. The chains can self-assemble to form small-scale domains whose size and geometry depend on the molecular weights of the two types of polymer and their interaction [1]. With the purpose of fabricating arrays of magnetic nanosized dots, which are a potential candidate for magnetic hard-drive media, we are templating the block copolymers in a removable template. Previously, sphere-forming poly(styrene-b-ferrocenyldimethylsilane) (PS-PFS) diblock copolymers were successfully aligned in 2-D [2] or 3-D [3] templates. In addition, the spherical morphology of poly(styrene-b-dimethylsiloxane) (PS-PDMS) block copolymers can be templated using an array of nanoscale topographical elements that act as surrogates for the minority domains of the block copolymer, as demonstrated in Figure 1[4]. The PS-PDMS diblock copolymers have a large interaction parameter and a high etch-contrast between two blocks, which are desirable for long-range ordering and pattern-transfer into functional materials. Concentric ring patterns can also be obtained by using circular templates [5]. Beyond rather limited morphologies of diblock copolymers, an appropriate combination of block sequence, interaction parameter of the adjacent blocks, volume fraction, and molecular weights of ABC triblock polymer thin films provides a diversity of new structures. For example, core-shell structured triblock terpolymer can be obtained by designing the block sequence and volume fraction of the blocks. Figure 2a presents vertically oriented high-density nanorings from PS-PFS-P2VP polymers after the selective removal of PS and P2VP [6]. Square arrays of dots can also be achieved from a PI-PS-PFS self-assembled triblock terpolymer, as shown in Figure 2c.

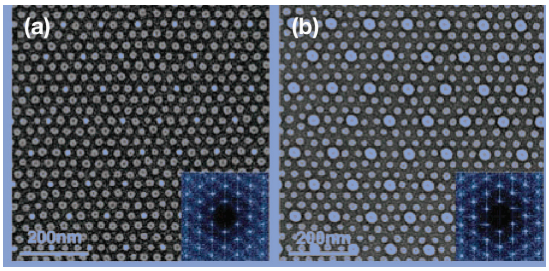


FIGURE 1: SEM images of ordered BCP spheres formed within a sparse 2D lattice of HSQ posts (brighter dots). The substrate and post surfaces were functionalized with a PDMS brush layer in (a), which corresponds to the schematic in (A), and with a PS brush layer in (b). The insets show the 2D Fourier transforms.

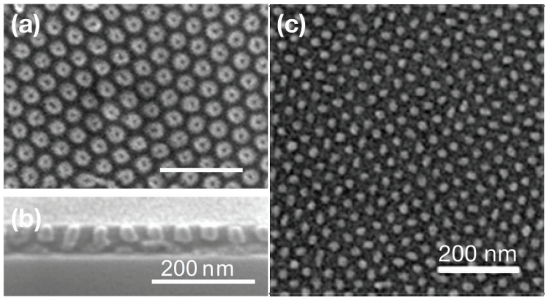


FIGURE 2: Ring arrays of PFS from a thin film of a core-shell cylindrical-morphology PS-b-PFS-b-P2VP triblock terpolymer. (a) top view (b) side view. (c) Square array of PFS dots from a thin film of PI-b-PS-b-PFS triblock terpolymer. PI and PS have been removed by O2 RIE.

REFERENCES

[1] E.L. Thomas and R.L. Lescanec, "Phase morphology in block copolymer systems," *Phil. Trans. R. Soc. Lond. A*, vol. 348, pp.146-164, 1994.

[2] J. Cheng, C.A. Ross, and A. Mayes, "Nanostructure engineering by templated self-assembly," *Nat. Mater.*, vol. 3, pp. 823-828, 2004.

[3] V.P. Chuang, J.Y. Cheng, T.A. Savas, and C.A. Ross, "Three-dimensional self-assembly of spherical block copolymer domains into V-shaped grooves," *Nano Lett.*, vol. 6, pp. 2332-2337, 2006.

[4] I. Bita, J.K.W. Yang, Y.S. Jung, C.A. Ross, E.L. Thomas, and K.K. Berggren, "Graphoepitaxy of self-assembled block copolymers on two-dimensional periodic patterned templates," *Science*, vol. 321, pp. 939-943, 2008 .

[5] Y.S. Jung, W. Jung and C.A. Ross, "Nanofabricated concentric ring structures by templated self-assembly of a diblock copolymer," *Nano Lett.*, vol. 8, pp. 2975-2981, 2008.

[6] V.P. Chuang, C.A. Ross, J. Gwyther, and I. Manners, "Self-assembled nanoscale ring arrays from a polystyrene-b-polyferrocenylsilane-b-poly(2-vinylpyridine) triblock terpolymer thin film," *Adv. Mater.* 2009 (in press).

Nanofabricated Reflection and Transmission Gratings

M. Ahn, S. K. Slater, P. Mukherjee, R. K. Heilmann, M. L. Schattenburg
Sponsorship: NASA, NSF

Diffraction gratings and other periodic patterns have long been important tools in research and manufacturing. Diffraction is due to the coherent superposition of waves—a phenomena with many useful properties and applications. Waves of many types can be diffracted, including visible and ultraviolet light, x-rays, electrons, and even atom beams. Periodic patterns have many useful applications in fields such as optics and spectroscopy; filtering of beams and media; metrology; high-power lasers; optical communications; semiconductor manufacturing; and nanotechnology research in nanophotonics, nanomagnetics, and nanobiology.

A long-standing problem with transmission gratings in the extreme ultraviolet (EUV) and soft x-ray bands has been the strong absorption of photons upon transmission, and thus a low diffraction efficiency in this important wavelength band. We have recently solved this problem with the invention and fabrication of critical-angle transmission (CAT) gratings. This new design for the first time combines the high broadband efficiency of blazed grazing-incidence reflection gratings with the superior alignment and figure tolerances and the low weight of transmission gratings [1], [2]. The CAT gratings consist of ultrahigh-aspect-ratio, nm-thin freestanding grating bars with sub-nm smooth sidewalls that serve as efficient mirrors for photons incident at graze angles below the angle for total external reflection (see Figures 1 and 2). Blazing can concentrate diffracted power into a single or a few desired diffraction orders and has been confirmed through x-ray tests. Blazing also enables the use of higher diffraction orders and leads to manifold increases in spectral [3] and spatial resolution in spectrometer or focusing applications, respectively. We have achieved grating bar aspect ratios of ~ 150 in 200-nm-period CAT gratings and are currently focusing on optimizing internal support structures.

Work is also ongoing in the area of high-precision pattering of silicon-immersion echelle gratings for high-resolution (R ~ 100,000) applications in infrared telescopes for astronomy [4].

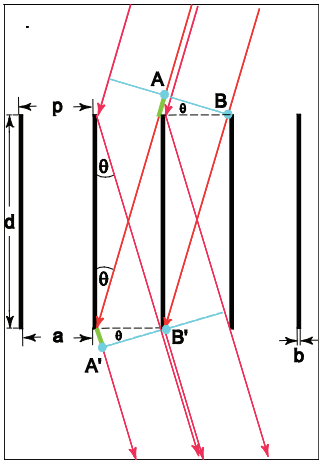


FIGURE 1: Schematic of the CAT grating principle. Diffraction peaks appear where the path length difference AA'-BB' equals an integer multiple of the wavelength.

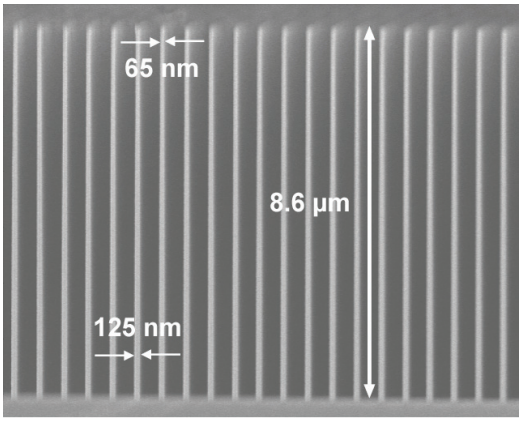


FIGURE 2: Scanning electron micrograph of a cleaved cross-section through a 574 nm-period silicon CAT grating that was (intentionally) not etched all the way through. The grating bar aspect ratio is close to 100 and is increased to ~ 150 for the final grating.

REFERENCES

[1] R. K. Heilmann, M. Ahn, E. M. Gullikson, and M. L. Schattenburg, "Blazed High-Efficiency X-Ray Diffraction via Transmission through Arrays of Nanometer-Scale Mirrors," *Optics Express*, vol. 16, pp. 8658-8669, June 2008.

[2] M. Ahn, R. K. Heilmann, and M. L. Schattenburg, "Fabrication of 200 nm period blazed transmission gratings on silicon-on-insulator wafers," *Journal of Vacuum Science and Technology B*, vol. 26, pp. 2179-2182, Dec. 2008.

[3] R. K. Heilmann, M. Ahn, and M. L. Schattenburg, "Fabrication and performance of blazed transmission gratings for x-ray astronomy," in *Proceedings SPIE* 7011, 2008, 701106.

[4] J. P. Marsh *et al.*, "Fabrication and performance of silicon immersion gratings for infrared spectroscopy," in *Proceedings SPIE* 6269, 2006, 62694J.

Nanometrology

R. Heilmann, Y. Zhao, D. Trumper, M. L. Schattenburg
Sponsorship: NSF

Manufacturing of future nanodevices and systems will require accurate means to pattern, assemble, image, and measure nanostructures. Unfortunately, the current state-of-the-art of dimensional metrology, based on the laser interferometer, is grossly inadequate for these tasks. While it is true that when used in carefully-controlled conditions interferometers can be very precise, they typically have an accuracy measured in microns rather than nanometers. Achieving high accuracy requires extraordinarily tight control of the environment and thus high cost. Manufacturing at the nanoscale will require new technology for dimensional metrology that enables sub-1-nm precision and accuracy in realistic factory environments.

A recently formed MIT-UNC–Charlotte team is developing new metrology technology based on large-area grating patterns that have long-range spatial-phase coherence and ultra-high accuracy. Our goal is to reduce errors in gratings by 10-100 times over the best available today. These improved gratings can be used to replace interferometers with positional encoders to measure stage motion in new nanomanufacturing tools and to calibrate the dimensional scales of existing nanofabrication tools. This increased precision and accuracy will enable the manufacturing of nanodevices and systems that are impossible to produce today. Improved dimensional accuracy at the nano-to-picometer scale will have a large impact in many nanotechnology disciplines including semiconductor manufacturing, integrated optics, precision machine tools, and space research.

As part of this effort, we will utilize a unique and powerful tool recently developed at MIT called the Nanoruler that can rapidly pattern large gratings with a precision well beyond other methods. Another unique high-precision tool, the UNCC-MIT-built Sub-Atomic Measuring Machine (SAMM), is being brought to bear to research new ways to quantify and reduce errors in the gratings. Recent work at MIT has focused on improving the thermal controls in the Nanoruler lithography enclosure and developing an improved interferometer system to reduce errors in the stage metrology frame. At UNCC, the SAMM is undergoing extensive refurbishment and improvements designed to boost interferometer accuracy.

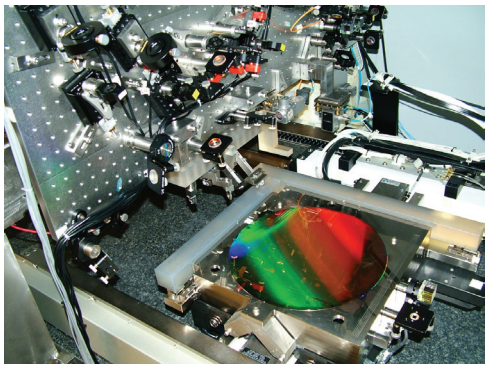


FIGURE 1: Photograph of the Nanoruler lithography and metrology system built by MIT students. This unique tool is the most precise grating patterning and metrology system in the world.

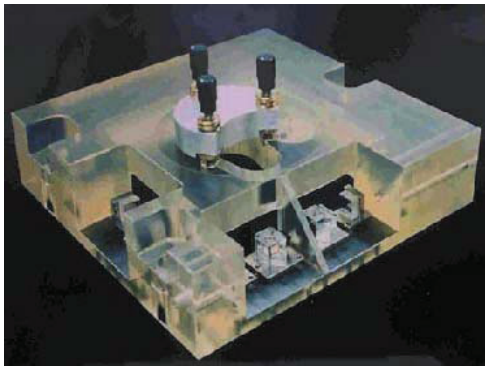


FIGURE 2: Photograph of reference block/sample holder for the Sub-Atomic Measuring Machine at the University of North Carolina – Charlotte.

REFERENCES

[1] "Nanometer-level repeatable metrology using the Nanoruler," P. Konkola, C. Chen, R.K. Heilmann, C. Joo, J. Montoya, C.-H. Chang and M.L. Schattenburg, *J. Vac. Sci. Technol. B* 21, 3097-3101 (2003).

[2] "Dimensional metrology for nanometer-scale science and engineering: towards sub-nanometer accurate encoders," R.K. Heilmann, C.G. Chen, P.T. Konkola and M.L. Schattenburg, *Nanotechnology* 15, S504-S511 (2004).

[3] "Measuring two-axis stage mirror non-flatness using linear/angular interferometers," J. Montoya, R.K. Heilmann and M.L. Schattenburg, *Proc. of the 19th Annual Meeting of the American Society for Precision Engineering*, Vol. 34, 382-385 (2004).

[4] "Optimization and temperature mapping of an ultra-high thermal stability environmental enclosure," Y. Zhao, D.L. Trumper, R.K. Heilmann and M.L. Schattenburg, *J. Precision Engineering* (*in press*).

Sub-Wavelength Interference Lithography with Absorbance Modulation

T. B. O'Reilly, R. Menon, H. I. Smith
Sponsorship: Lincoln Laboratory Integrated Photonics Initiative

The minimum period of the pattern that can be produced in interference lithography is generally restricted to half the wavelength of the light being used. While shorter wavelength sources are available, the properties of short wavelength lasers are not always suitable for use in interference lithography. As a result, there is great interest in finding ways to write patterns with periods below the diffraction limit, so that very fine pitch patterns can be written with sources that are easy to work with. We are pursuing an approach to patterning below the diffraction limit by combining a dual-wavelength IL (DWIL) system and absorbance-modulation technology [1]. In absorbance-modulation optical lithography (AMOL), an absorbance-modulation layer (AML), is placed on top of the photoresist layer. The absorbance-modulation layer is a polymer film containing reversible photochromic molecules that can be switched between two isomeric states using different wavelengths of light. An example of such a material is bis(bithienylethene) (BTE) which has two forms, as shown in Figure 1. If an AML containing BTE is simultaneously exposed to standing waves in both UV and red wavelengths, as shown in Figure 2, it is possible to set up dynamic competition between the open and closed states, forming regions in the AML, with sizes much smaller than the wavelength, that are transparent to UV light. These regions effectively serve as subwavelength apertures in the AML through which the photoresist is exposed by the UV wavelength.

REFERENCES

[1] R. Menon and H.I. Smith, "Absorbance-modulation optical lithography," *J. Opt. Soc. Am.* A 23, 2290-2294 (2006)

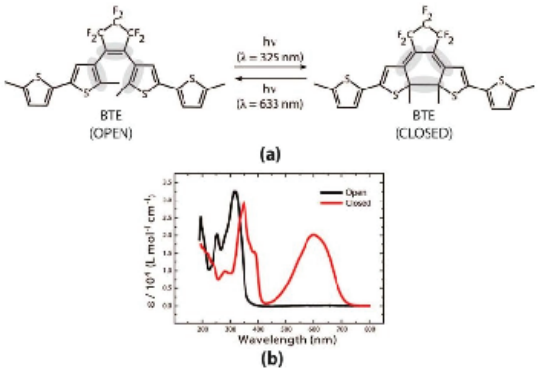


FIGURE 1: Molecular structure of the open and closed states of BTE. Exposure to UV wavelengths cause BTE to switch to the closed state, while exposure to longer wavelengths, red light for example) causes BTE to switch to the open state.

Since the states of the photochromic molecules are reversible, it is possible to shift the sets of fringes on the substrate, forming a new set of subwavelength apertures, and exposing a new set of lines in the resist. In effect, each exposure divides the spatial period of the original fringes, reducing the pitch of the final pattern. For example, if the initial spatial period were 400 nm, four exposures could be performed, shifting the fringes by 90 degrees between the exposures, to reduce the final period of the pattern to 100 nm. Ultimately, the extent to which the period can be divided will be limited by the performance of both the absorbance modulation layer and the photoresist, making a system to test and characterize AMOL materials an important tool. We are presently developing a DWIL system to be used both to test materials for use with AMOL and to provide a means of achieving sub-100nm period interference lithography with a relatively simple system and relatively long wavelengths. The planned system will form two standing waves, one using 351 nm light from an argon ion laser and a second from a longer wavelength red laser. In essence, the system consists of two independent Mach-Zehnder style IL systems, simultaneously forming standing waves of the same period that are 180 degrees out of phase with each other.

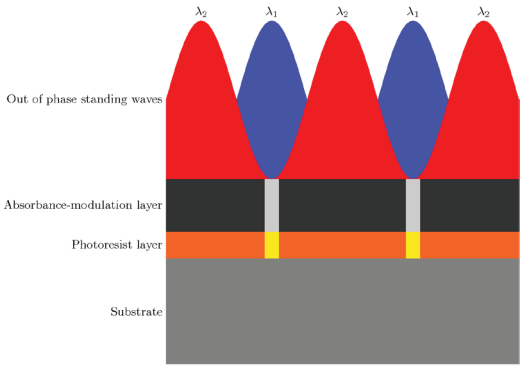


FIGURE 2: Schematic of the interaction of red and UV (shown in blue) wavelengths with an absorbance modulation layer. Out-of-phase standing waves formed by the two wavelengths result in the formation of narrow regions at the null of the red standing wave that are transparent to the UV light which serves to expose the photoresist. The AML narrows the width of the exposed regions compared to what would be possible with conventional IL exposures.

Interference Lithography

T. B. O'Reilly, H. I. Smith
Sponsorship: Lincoln Laboratory Integrated Photonics Initiative

Interference lithography (IL) is a means of rapidly writing periodic and quasi-periodic patterns , such as gratings and grids, over large areas using the coherent interference of light. The NanoStructures Laboratory has conducted research in this field for many years, developing IL systems capable of making patterns with a wide range of spatial periods, and helping to develop some of the applications of those patterns.

The lab currently operates three IL systems. Two of them, the Lloyd's mirror and Mach-Zehnder IL systems use 325 nm light from Helium-Cadmium lasers. The Lloyd's mirror IL system is a flexible and robust system that can be easily configured to write gratings with periods as small as 165 nm or as large as many microns. The ability to quickly change the period pf the pattern produced, coupled with the ease of use of this system, has made it possible for a large number of researchers to use the Lloyd's mirror system to produce patterns required for their research without having be become IL experts. Applications of these structures have included patterned magnetic media, patterned surfaces for templated self-assembly processes, and photonic crystals.

The Mach-Zehnder IL system, while less flexible than the Lloyd's mirror, produces higher quality patterns that are suitable for metrological applications. The third system, the Achromatic IL system (AIL) is a grating-based interferometer that writes 100 nm period gratings using 193 nm light from an ArF excimer laser. In addition, the NSL has close ties to the Space Nanotechnology Lab at MIT which operates the NanoRuler, which is among the most precise IL systems in the world.

We have recently developed a method to characterize photoresist performance by double-exposing a sample on an IL system; the sample is rotated slightly between the two exposures [1]. By analyzing the resulting pattern it is possible to determine how linewidth varies with exposure dose and dose modulation in fewer exposures than are required by previously described methods. The data collected from this method can be applied to models of specific IL systems to predict the variation of linewidth across the exposure area [2], which makes it possible to select IL system design and exposure parameters to improve exposure uniformity.

REFERENCES

[1] T. B. O'Reilly and H. I. Smith, "Photoresist characterization using double exposures with interference lithography," *J. Vac. Sci. Technol. B,* vol. 26, no. 1, p. 128, Jan. 2008.

[2] T. B. O'Reilly and H. I. Smith, "Linewidth uniformity in Lloyd's mirror interference lithography systems," *J. Vac. Sci. Technol. B*, 26, no.6, p.2131, Nov. 2008.

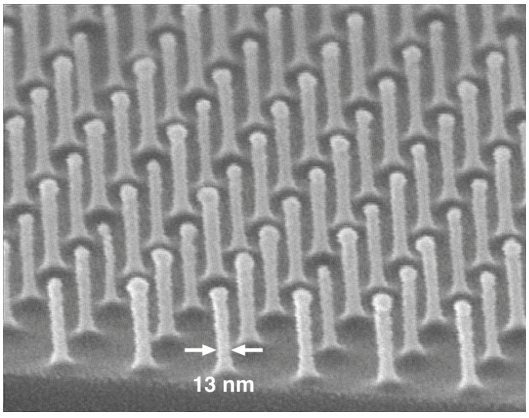


FIGURE 1: Scanning electron micrograph of a 100 nm-period grid produced with the AIL system. PMMA was exposed on top of an antireflection coating and the pattern was transferred into Si by reactive ion etching.

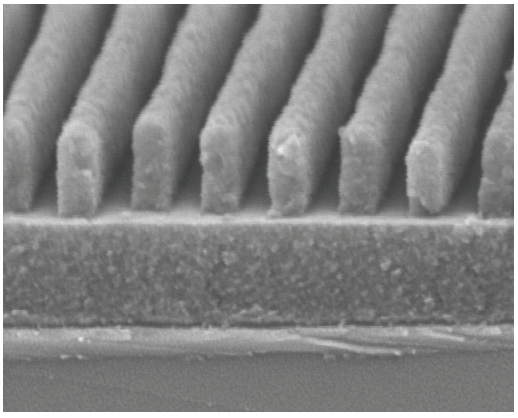


FIGURE 2: Micrograph of 165 nm period grating produced with the Lloyd's mirror. This system can be used to write patterns with periods ranging from 165 nm up to several microns.

Catalyst Engineering and Growth Mechanisms of Si and III-V Nanowires

S. T. Boles, E. A. Fitzgerald, C. V. Thompson
Sponsorship: Singapore-MIT Alliance

The vapor-liquid-solid mechanism for growth of single-crystal whiskers and wires was originally discovered in the 1960s, but it has gained new interest in the last decade as a way to fabricate high-performance nanoscale electronic devices below the limits of photolithography. Although a great deal of attention has been focused on the electronic properties of Si and III-V nanowires, many of the physical mechanisms involved in growing these single-crystal wires remain unclear. We have been investigating the importance of catalyst size and shape in growth morphology by using evaporated island catalysts, catalysts derived from dewetted thin films, and commercially available nanoparticles. Optimizing catalyst processing conditions and combining them with specific topographies or templates, such as inverted pyramid arrays or silicon dioxide gratings achieves precise control over catalyst placement and subsequent nanowire placement. This study also examines the role of growth conditions by controlling temperature, partial pressures of reactants and pre-growth annealing. These parameters have been determined to be critical not only to stable and repeatable growth of Si and III-V nanowires, but also to controlling the relative orientation and defect generation at the substrate-wire interface [1].

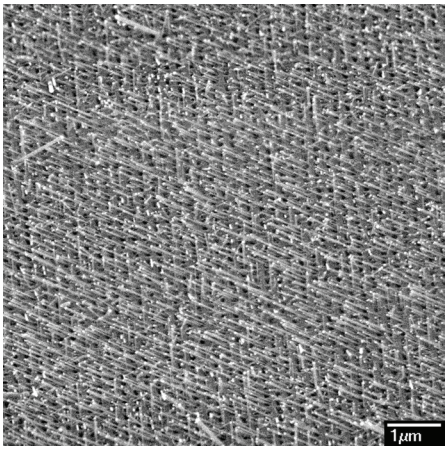


FIGURE 1: The Si nanowires grown on a Si <100> substrate with an inverted pyramid array and e-beam-evaporated Au-catalyst particles.

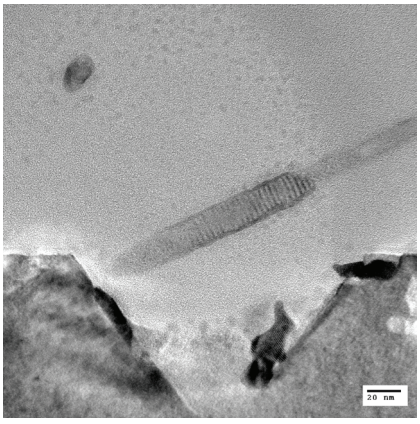


FIGURE 2: The InP/GaP core/shell nanowire heterostructures grown on a Si <100> substrate with an inverted pyramid array and e-beam- evaporated Au-catalyst particles.

REFERENCES

[1] S. T. Boles, C. V. Thompson and E. A. Fitzgerald, "Influence of indium and phosphine on Au-catalyzed InP nanowire growth on Si substrates," *Journal of Crystal Growth*, vol. 311, pp. 1446-1450, Feb. 2009.

Ultra-high-density Silicon Nanowire Arrays Fabricated by Metal-assisted Etching and Block Copolymer Lithography

S.-W. Chang, V. P. Chuang, S. T. Boles, C. A. Ross, C. V. Thompson
Sponsorship: Singapore-MIT Alliance

Semiconductor nanowires have attracted considerable attention due to potential applications arising from their quasi-one-dimensional structure. In particular, silicon nanowires (SiNWs) are potential candidates for applications in nanoscale electronics, sensors, and other devices. The most commonly used method for the fabrication of SiNWs is the vapor-liquid-solid (VLS) technique, in which metal nanoparticles are used as catalysts for growth by chemical vapor deposition. One major concern for VLS-grown wires is the diffusion of catalyst metal, typically gold, into the wires at the high temperatures usually required for growth. Another challenge is getting vertical epitaxial growth on Si(100) wafers. This problem limits the integration of VLS nanowires with current CMOS technology. To circumvent these problems, an electrochemical etching method, known as metal-assisted etching (MAE), has recently received significant attention. In this approach metal catalysts are used to enhance local Si etching at the metal-silicon interface in a mixture of hydrofluoric acid and an oxidant. The process can be used to fabricate high-aspect-ratio Si structures through patterned etching of silicon wafers. For example, we have used metal-assisted etching in conjunction with block copolymer lithography and post-etching critical-point-drying to create silicon nanowire arrays with very high density and aspect ratio.

In this approach, a diblock copolymer, polystyrene (PS)-block-polyferrocenyldimethysilane (PFS) is spun onto a silicon substrate coated with an oxide layer, followed by vacuum annealing to allow for phase separation. The PFS block forms spherical microdomains surrounded by a PS matrix, which is removed by oxygen-reaction ion-etching (RIE). The PFS spheres are then used as a dry etching mask to pattern-transfer into the underlying oxide layer. Using the resulting oxide nanopillars as a metal-deposition mask, a metal catalyst antidot array is obtained after film deposition and lift-off. Finally, ordered arrays of SiNWs with good fidelity to the original block copolymer pattern are obtained by etching the silicon under the gold in a mixed solution of hydrofluoric acid and hydrogen peroxide. Post-etching drying is done in a critical-point drier to reduce capillary-force-induced clustering at wire tips. We are currently exploring application of these structures in electrochemical devices.

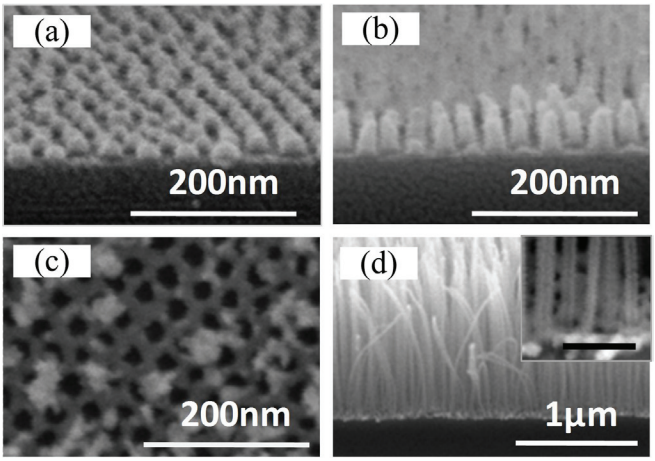


FIGURE 1: Scanning electron microscope images showing steps in SiNW fabrication: (a) *PS-b-PFS* on a silicon substrate coated with silicon oxide after PS matrix has been removed by oxygen RIE; (b) Oxide pillars after CF4 RIE; (c) Au anti-dot array after liftoff of the pillars; and (d) Silicon nanowire array after metal-assisted etching.

REFERENCES

[1] S.-W. Chang, V.P. Chuang, S.T. Boles, C.A. Ross, and C.V. Thompson, "Densely-packed arrays of ultrahigh-aspect-ratio silicon nanowire fabricated using block copolymer lithography and metal-assisted etching", *Advanced Functional Materials*, in press.

Growth and Characterization of Carbon Nanotubes for Integrated Circuit Interconnects

R. R. Mitchell, G. D. Nessim, A. F. Al-Obeidi, C. V. Thompson
Sponsorship: SRC/FCRP IFC, Intel Corporation

As integrated circuit technology is developed at dimensions below 32 nm, carbon nanotubes (CNTs) represent an ideal replacement for copper interconnects as they can carry higher current densities, do not need liners, and do not suffer from electromigration. However, fabrication issues such as growing the desired type of CNTs, using CMOS-compatible processes (e.g., ideally at temperature below 400°C), and making electrical contacts and interconnections remain major technical challenges.

For electrical applications, it is important to grow CNTs on conductive substrate [1], [2]. Using appropriate catalyst/substrate metallic thin films, we have grown vertically-aligned, crystalline CNTs using thermal chemical vapor deposition at 475°C (Figure 1). Preliminary electrical measurements show ohmic contact of the CNTs with the metallic substrate. Additionally, our group hopes to decrease the processing temperature further using plasma enhanced chemical vapor deposition.

We have also grown CNTs on conductive substrates into an insulating alumina scaffold with regularly spaced pores (Figure 2). The insulating scaffold is fabricated using interference lithography and anodization of aluminum. This structure simulates an array of nanometer-scale vias filled with CNTs. In order to have CNTs with uniform height (length) and to make electrical contact with all the walls in the multi-wall tubes, we ion-milled the top after CNT growth. The electrical properties of these CNTs can be collectively characterized through deposition of a conducting overlayer on all the CNTs or individually characterized using an AFM on uncapped CNTs. We plan to characterize electrical properties as a function of CNT diameter and length and as a function of contact metallurgy.

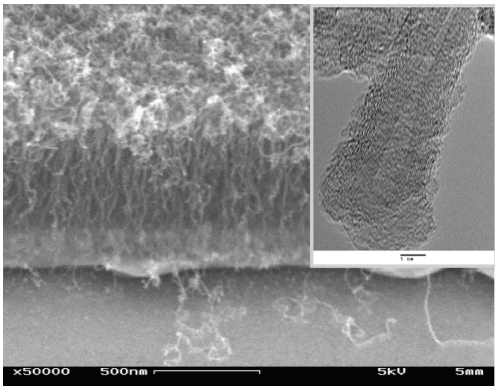


FIGURE 1: Carpet of vertically-aligned CNTs on conductive substrate grown at 475°C. The catalyst/underlayer system is Fe/Ta. The HRTEM image on the inset shows the crystalline nature of the CNTs (scale bar 5 nm).

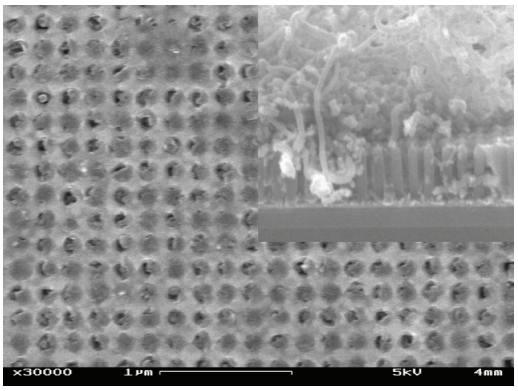


FIGURE 2: CNTs grown into alumina scaffold with pores regularly spaced. The CNTs are flush with the top surface after ion milling. The inset shows the CNTs prior to ion milling.

REFERENCES:

[1] H.T. Ng, B. Chen, J.E. Koehne, A.M. Cassell, J. Li, J. Han, and M. Meyyappan, "Growth of carbon nanotubes: A combinatorial method to study the effects of catalysts and underlayers," *Journal of Physical Chemistry B*, vol. 107, no. 33, pp. 8484-8489, 2003.

[2] S. Talapatra, S. Kar, S.K. Pal, R. Vajtai, L. Ci, P. Victor, M.M. Shaijumon, S. Kaur, O. Nalamasu, P.M. Ajayan, "Direct growth of aligned carbon nanotubes on bulk metals," *Nature Nanotechnology*, vol. 1, no. 2, pp. 112-116, 2006.

Nano-particle Formation via Solid-state Dewetting

J. Ye, A. L. Giermann, D. Kim, W.-K. Choi, Y. J. Oh, H. I. Smith, C. A. Ross, C. V. Thompson
Sponsorship: Singapore-MIT Alliance

We are investigating solid-state dewetting of thin films as a technique for producing ordered arrays of metal nano-particles over large areas. Such arrays are used as catalysts for nanowire and nanotube growth and may also be of interest in memory or plasmon device applications. In order to obtain ordered dewetting with polycrystalline films, we employ physical templates. One technique is to physically constrain the area of film that dewets by pre-patterning a polycrystalline gold film on silicon dioxide. By pre-patterning a film into various geometries and observing the morphological evolution of each pattern, we found that certain geometries lead to self-ordering and alignment of the dewetted nano-particles (Figure 1). Further characterization of the effects of film thickness and pattern dimensions on self-alignment is underway.

Another technique for ordered dewetting of polycrystalline films is the use of topographic templates to modulate the curvature of as-deposited films. Topographic templates regularly modulate the curvature of as-deposited polycrystalline thin films, leading to an ordered dewetting process. Gold films dewetted on di-periodic arrays of oxidized pyramidal pits in silicon result in one-to-one self-assembly of ordered arrays of gold particles over large areas. Compared to dewetting on flat substrates, the templates impose a significant decrease in average particle size and ensure a narrow size and spatial distribution (Figure 2). In this case, this technique results in crystallographic ordering of the particles, imposing an in-plane texture and changing the out-of-plane texture [1]. We have demonstrated similar morphological and crystallographic results for gold dewetting on mono-periodic saw-tooth gratings. Similar results ordering results (but without crystallographic alignment) have been obtained for Co [2]. In addition, we have developed a combination of patterned deposition on topography and controlled dewetting, to produce ordered arrays of particle arrays with dimensions of a few ten's of nanometers [3].

In the case of a single crystalline film, the dewetted islands show regular patterns. We observe a strong dependence of the morphological evolution of single crystalline nickel thin films on the thickness of the film and on the crystallographic orientation of the film. The latter is determined by an epitaxial relationship with a magnesium oxide substrate. The resulting nano-particles remain epitaxial and thus share both in- and out-of-plane crystallographic alignment. Therefore, we believe that this work could give us an opportunity to study the effect of crystallographic orientation of catalysts on the growth of nanotubes and nanowires.

REFERENCES

[1] A.L. Giermann and C.V. Thompson, "Solid-state dewetting for ordered arrays of crystallographically oriented metal particles," *Applied Physics Letters*, vol. 86, p. 121903, Mar. 2005.

[2] W.K. Choi, T.H. Liew, H.G. Chew, F. Zheng, C.V. Thompson. Y. Wang, M.H. Hong, X.D. Wang, L. Li and J. Yun, "A Combined Top-down and Bottom-up approach for Precise Placement of Metal Nanoparticles on Silicon," *Small* 4, 330 (2008).

[3] Yong-Jun Oh, C. A. Ross, Yeon Sik Jung, Yang Wang, Carl V. Thompson, "Co Nanoparticle Arrays made by Templated Solid-State Dewetting," *Small* 5, 860 (2009).

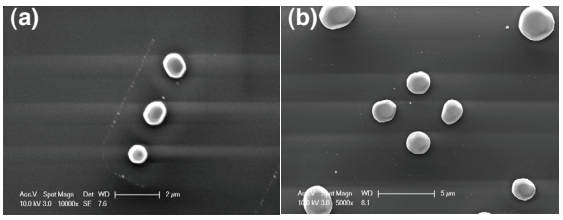


FIGURE 1: The SEM images of self-aligned Au dots through solid-state dewetting process. Solid-state dewetting process changes a rectangular Au pattern to self-aligned dots during thermal annealing. (a) Self-aligned 3 dots with single row from the pattern dimension of 3 μm x 7 μm x 30 nm. (b) Self-aligned 4 dots with double row from the pattern dimension of 9.3 μm x 9.3 μm x 120 nm. All scale bars represent 5 μm.

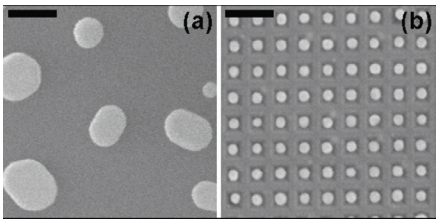


FIGURE 2: The effect of topography on particle morphology. The results of dewetting a 10-nm-thick Au film on (a) a flat substrate and (b) a topographic substrate. Micrographs are displayed at the same magnification to emphasize the effect of topography on particle size. Scale bars are 200 nm in length.

Nanostructured Resistor- and Transistor-based Gas Sensors

G. Whitfield, Y. S. Jin, H. L. Tuller in collaboration with I. D. Kim (KIST), A. Rothschild (Technion), J. Lewis (U. Illinois)
Sponsorship: KIST, NSF, US-Israel Binational Science Foundation

Gas sensors play a vital role in public health and safety, industrial process control, and the reduction of toxic emissions into the environment [1]. Conductometric gas sensors based on semiconducting metal-oxide thin films are of high interest in many applications due to their high sensitivity, small size, and simplicity of measurement. Reproducibility, however, often suffers due to generally uncontrolled electronic properties of the film-substrate interface. Several approaches are being taken to overcome this limitation including the use of microsphere templating [2], or meshes of interconnected nanofibers [3]. In the case of dense films, thin-film transistor (TFT) configurations are being investigated to achieve improved control [4].

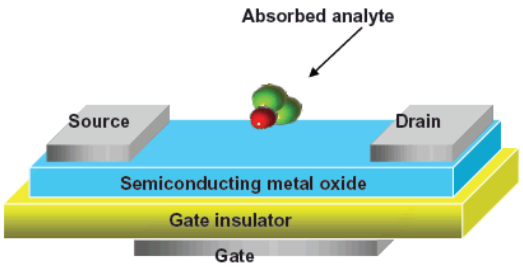


FIGURE 1: Schematic of gas sensor.

REFERENCES

[1] F. Rock, N. Barsan, U. Weimar, *Chemical Reviews* 108, 705 (2008)
[2] I.D. Kim, A. Rothschild, T. Hyodo, H.L. Tuller, *Nano Letters* 6, 193 (2006)
[3] I.D. Kim, A. Rothschild, D.J. Yang, H.L. Tuller, *Sens Act B* 130, 9 (2008)
[4] Y.S. Jin, Masters Thesis, MIT Department of Materials Science and Engineering 2009.

Directional Liquid Spreading on Asymmetric Nanostructured Surfaces

K. Chu, R. Xiao, E. N. Wang

The controllability of liquid-spreading and droplet wettability on surfaces have been of significant interest for a broad range of applications, including inkjet printing, biological microfluidics, and fluidic-based thermal management devices [1-5]. In this research, we investigated the ability to manipulate the directionality of liquid-spreading by using asymmetric nanostructured surfaces. The nanostructures were composed of silicon pillars with diameters of 250 nm with one side coated with a gold film of thicknesses ranging from 250 nm to 400 nm. Due to the thermal expansion mismatch of the materials, the pillars deflected to angles ranging from 7 to 52 degrees, where the deflection angle was dependent on the thickness of the gold layer. Figure 1 shows an example of asymmetric nanopillar array with a 12-degree deflection angle. We demonstrated that such asymmetrical structures allow the advancing side (+X side) of the droplet to spread, while pinning the receding side (-X side) of the droplet, as shown in Figure 2 (a) and (b). Detailed experiments were performed to characterize the effect of material properties and nanostructure deflection angle on spreading dynamics. The surface tension of the liquid was also varied to examine the effect on spreading velocity. In sum, the directional propagation of the liquid film in the nanopillars allows control of the droplet spreading process. This work offers new opportunities to develop tunable nanostructures to control directional liquid droplet spreading and film propagation for microfluidic systems.

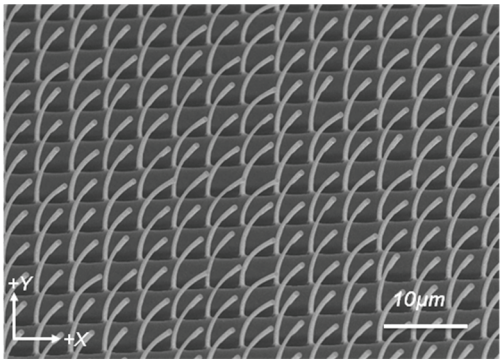


FIGURE 1: Scanning electron micrograph of a surface with uniform array of asymmetric nanopillars of 12° deflection angle. The diameter and spacing of pillars are ~500nm and 3.5μm, respectively.

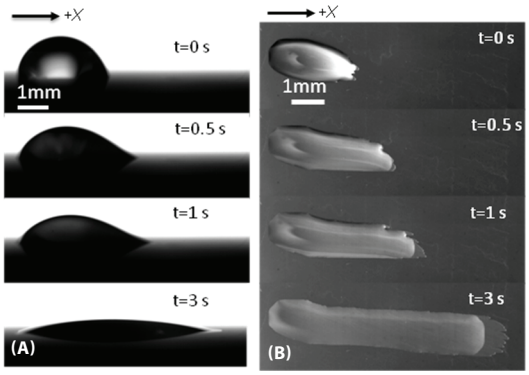


FIGURE 2: (a) Side view and (b) top view of time-lapse images of directional spreading phenomenon of a liquid droplet. The images show that the initial (t=0 s) position with the final (t=3 s) position of contact line of a liquid droplet on the -X side was pinned while the liquid spreads only in the +X direction.

REFERENCES

[1] SP. G. de Gennes, "Wetting: statics and dynamics," *Review of Modern Physics*, vol. 57, no. 3, pp. 827-863, July 1985.

[2] A. L. Biance, C. Clanet, and D. Quere, "First steps in the spreading of a liquid droplet," *Physical Review E*, vol. 69, pp. 016301, 2004.

[3] D. Quéré, "Rough ideas on wetting," *Physica A*, vol. 313, pp. 32-46, 2002.

[4] D. Quéré, "Non-sticking drops," *Reports on Progress in Physics*, vol. 68, pp. 2495–2532, 2005.

[5] T. N. Krupenkin, J. A. Taylor, T. M. Schneider, and S. Yang, "From Rolling Ball to Complete Wetting: The Dynamic Tuning of Liquids on Nanostructured Surfaces," *Langmuir*, vol. 20, no. 10, pp. 3824-3827, February 2004.

High-lux Cooling on Nanoengineered Surfaces

R. Xiao, E. N. Wang

The demand for increased performance of integrated circuits has introduced a growing demand for new thermal management solutions [1], [2]. Various thermal management schemes have been studied, among which thin-film evaporation has received recent attention due to its potential in achieving high heat dissipation rates (~1000 W/cm^2) with low thermal resistance. Traditional methods of forming thin liquid films, including jet-impingement or spray, usually consume considerable power or require significant space, which limit their applications [3], [4]. In this work, we investigated microstructures consisting of micro-pillar arrays as a new method to achieve thin-film evaporation. The microstructures have diameters ranging from 5 μm to 10 μm, separated by spacings ranging from 5 μm to 10 μm (Figure 2a). Liquid is driven by capillarity to form a thin film whose thickness is the same as the height of the pillars (Figure 1). A semi-analytical model was developed to predict the propagation rate of the liquid film and the model was validated with experiments. Heaters were fabricated on the backside of the chips with micro-fabrication technology to simulate the non-uniform heat flux on integrated chips. The temperature distribution over the chip was measured by distributed thermoresistors (Figure 2b). Experiments show that with same super-heat, the heat dissipation rates on microstructured surfaces are higher than on smooth surfaces. The heat dissipation rate is positively related to the propagation rate of the liquid film. Optimizing pillar geometries according to the model in this work achieves an optimized heat dissipation rate of several hundreds of Watts per cm^2 at local heat spots. This work provides opportunities to meet the high heat- dissipation demand for future high-performance integrated circuits.

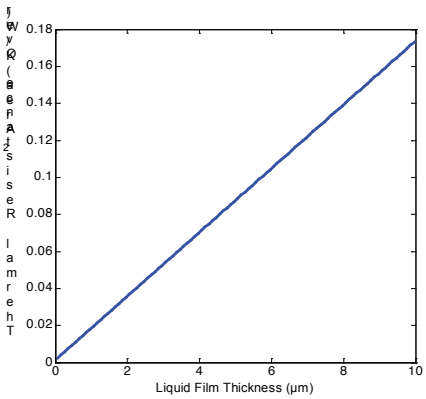


FIGURE 1: Thermal resistance of water film as a function of the film's thickness. To achieve a thermal resistance below 0.1 K/W, the film's thickness should be below 6 μm.

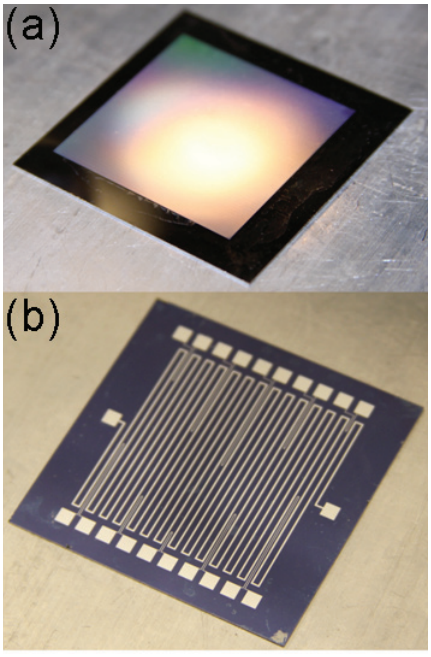


FIGURE 2: a) Image of front-side device with the micropillar array with diameters of 10 μm and spacings of 5 μm. b) Image of back-side devices with ten temperature sensors and one heater.

REFERENCES

[1] S. Krishnan, S. V. Garimella, G. M. Chrysler and R. V. Mahajan, "Towards a Thermal Moore's Law", IEEE Transaction on Advanced Packaging, Vol. 30, No. 3, pp. 462-474, August 2007

[2] B. Agostini, M. Fabbri, J. E. Park, L. Wojtan, J. R. Thome, B. Michel, "State of the Art of High Heat Flux Cooling Technologies", Heat Transfer Enigeering, Vol. 28, No. 4, pp. 258-281, April 2007

[3] I. Mudawar, "Assessment of High-Heat-Flux Thermal Management Schemes", IEEE Transaction on Components and Packaging Technologies, Vol. 24, No. 2, pp. 122-141, June 2001

[4] S. G. Kandlikar, A. V. Bapat, "Evaluation of Jet Impingement, Spray and Microchannel Chip Cooling Options for High Heat Flux Removal", Heat Transfer Engineering, Vol. 28, No. 11, pp. 911-923, November 2007

Aligned CNT-based Microstructures and Nano-engineered Composite Macrostructures

B. L. Wardle, R. Guzman de Villoria, N. Yamamoto, H. Cebeci, J. Blanco, H. M. Duong, F. Fachin, S. L. Figueredo, K. Ishiguro, W. Kim, L. Megalini, S. P. Pont, S. A. Steiner III, S. Vaddiraju, S. Wicks

Sponsorship: Nano-Engineered Composite aerospace STructures (NECST) Consortium, NSF, Fulbright IS&T Fellowship

Carbon nanotube (CNT) composites are promising new materials for structural applications thanks to their mechanical and multifunctional properties. We have undertaken a significant experimentally-based program to understand both microstructures of aligned-CNT nanocomposites and nano-engineered advanced composite macrostructures hybridized with aligned CNTs.

Aligned nanocomposites are fabricated by mechanical densification and polymer wetting of aligned CNT forests [1]. Polymer wetting is driven by capillary forces that arise upon contact of the polymer with the nanostructured CNT forest [2], [3], the rate of which depends on properties of the CNT forest (e.g., volume fraction) and the polymer (viscosity, contact angle, etc.). Here the polymer is unmodified aerospace-grade epoxy. CNT forests are grown to mm-heights on 1-cm^2 Si substrates using a modified chemical vapor deposition process. Following growth, the forests are released from the substrate and can be handled and infiltrated. The volume fraction of the as-grown CNT forests is about 1%; however, the distance between the CNTs (and thus the volume fraction of the forest) can be varied by applying a compressive force along the two axes of the plane of the forest to give volume fractions of CNTs exceeding 20%.

Variable-volume fraction-aligned CNT nanocomposites were characterized using optical, scanning electron (SEM) and transmission electron (TEM) microscopy to analyze dispersion and alignment of CNTs as well as overall morphology. Physical property testing is underway.

Nano-engineered composite macrostructures hybridized with aligned CNTs are prepared by placing long (>20 μm) aligned CNTs at the interface of advanced composite plies as reinforcement in the through-thickness axis of the laminate. Three fabrication routes were developed: transplantation of CNT forests onto pre-impregnated plies [4] (the "nano-stitch" method), placement of detached CNT forests between two fabrics followed by subsequent infusion of matrix, and *in situ* growth of aligned CNTs onto the surface of ceramic fibers followed by infusion or hand-layup [5]. Aligned CNTs are observed at the composite ply interfaces and give rise to significant improvement in interlaminar strength, toughness, and electrical properties. Interestingly, toughness improvement has demonstrated a favorable nano-scale size effect [6]. Analysis of the multifunctional properties and nanoscale interactions between the constituents in both the nanocomposites and hybrid macrostructures is underway. A new route to fabricate these materials in a continuous way is being developed.

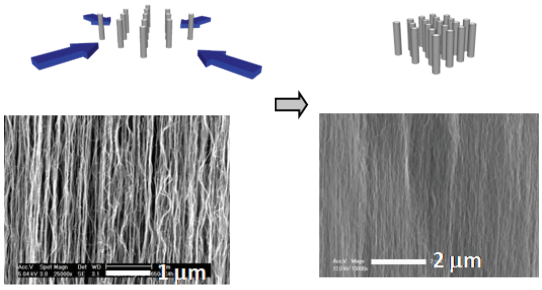


FIGURE 1: Aligned-CNT nanocomposites via biaxial mechanical densification of CNT forests.

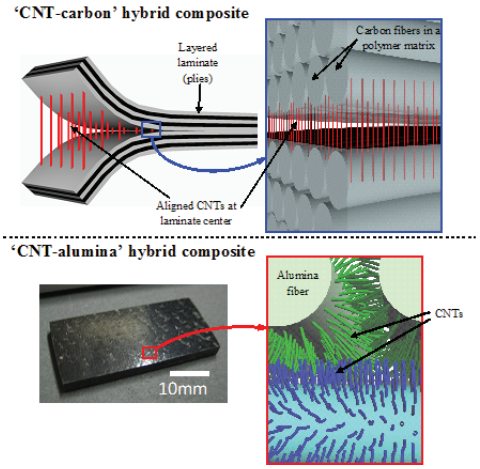


FIGURE 2: Aligned-CNT nano-engineered composite macro-scale architectures.

REFERENCES

[1] B. L. Wardle, D. S. Saito, E. J. Garcia, A. J. Hart and R. Guzman de Villoria, "Fabrication and Characterization of Ultra-High Volume Fraction Aligned Carbon-Nanotube-Polymer Composites", Advanced Materials, vol. 20, pp. 2707-2714, 2008.

[2] E. J. García, A. J. Hart, B. L. Wardle and A. H. Slocum, "Fabrication of composite microstructures by capillarity-driven wetting of aligned carbon nanotubes with polymers", Nanotechnology, vol. 18, pp. 165602-165613, 2007.

[3] E. J. García, A. J. Hart, B. L. Wardle and A. H. Slocum, "Fabrication and Nanocompression Testing of Aligned Carbon-Nanotube-Polymer Nanocomposites", Advanced Materials, vol. 19, pp. 2151-2156, 2007.

[4] E. J. Garcia, B. L. Wardle and A. J. Hart, "Joining Prepreg Composite Interfaces with Aligned Carbon Nanotubes", Composites Part A vol. 39, pp. 1065-1070, 2008.

[5] N. Yamamoto, A. J. Hart, S. S.Wicks, E. J. Garcia, B. L.Wardle and A. H. Slocum, "High-yield atmospheric-pressure growth of aligned carbon nanotubes on ceramic fibers for multifunctional enhancement of structural composites", Carbon , vol. 47, pp. 551-560, 2009.

[6] J. Blanco, E. J. Garcia, R. Guzman deVilloria and B. L. Wardle, "Limiting Mechanisms in Mode I Interlaminar Toughness of Composites Reinforced with Aligned Carbon Nanotubes", Journal of Composite Materials, vol. 43, no. 8, pp. 825-841, 2009.

Photonics

High Efficiency Organic Multilayer Photodetectors based on Singlet Fission

J. Lee, P. Jadhav, M. A. Baldo
Sponsorship: DOE

Organic optoelectronic devices are favorable for applications that require low-cost manufacturing processes or compatibility with flexible plastic substrates. For example, efficient organic photodetectors may find application in integrated organic optoelectronic circuits. Peumans *et al.* reported multilayer organic photodetectors with external quantum efficiencies of 75% across visible spectrum using an ultrathin (~10Å) donor-acceptor (DA) junction [1]. In multilayer photodetectors, photogenerated excitons efficiently dissociate via rapid charge transfer at a close DA interface. Photogenerated carriers escape via tunneling or percolating pathways before recombination, achieving high efficiency.

We aim to enhance the efficiency of an organic multilayer photodetector by exploiting exciton fission. In pentacene, the energy of a singlet exciton (an excited state with a total spin of 0) is higher than two triplets (with a total spin of 1). Thus the spin-allowed transition of a singlet into two triplets, called singlet fission, is energetically possible and occurs rapidly (<1ps), as Figure 1A shows [2]. If charge transfer takes place after singlet fission, one photon can lead to two carriers, doubling the efficiency.

To implement this idea, we built a multilayer photodetector composed of pentacene and C_{60} for donor and acceptor, respectively. Each layer thickness is 2nm, thin enough to allow efficient exciton separation and charge extraction. Figure 2 shows the external quantum efficiency (EQE) at a voltage bias of -2V. We fitted the EQE spectrum using optical interference modeling, obtaining the charge collection efficiencies of 1.15 and 0.85 for pentacene and C_{60}, respectively. This suggests that the EQE enhancement from singlet fission is ~35%, normalized for the charge collection efficiency. Furthermore, photocurrent due to selective illumination of pentacene decreases by up to ~3% under a magnetic field, which suppresses singlet fission. The magnetic field dependence confirms that the efficiency enhancement is due to singlet fission in pentacene/C_{60} multilayer photodetectors, widening the feasibility of exciton fission to improve various organic photodiodes such as organic light-emitting diodes, small-molecule photovoltaic cells, and dye-sensitized solar cells.

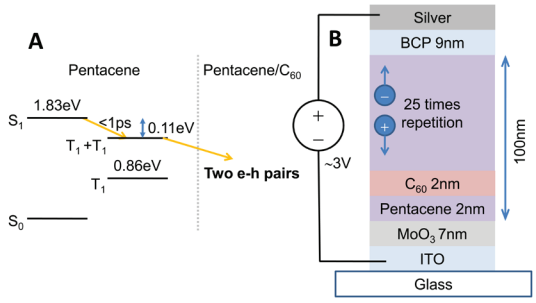


FIGURE 1: A: Energy transfer process in the pentacene/C_{60} photodetector. A singlet exciton created upon photoexcitation on pentacene undergoes singlet fission, leading to two triplets. They are separated at the pentacene/C_{60} heterojunction, generating photocurrent. B: Multilayer device structure.

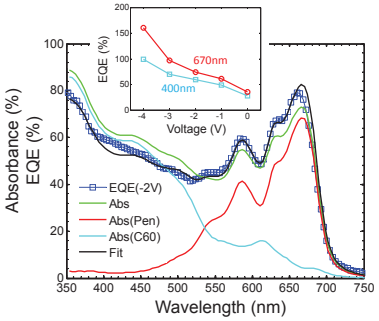


FIGURE 2: The external quantum efficiency (EQE) spectrum at a voltage of -2V and the absorbance of pentacene, C_{60} layers, and both. The EQE was modeled assuming the charge collection efficiencies are 1.15 and 0.85 for pentacene and C_{60}, respectively. The inset shows the EQE at 400nm and 670nm as a function of voltage.

REFERENCES

[1] P. Peumans, V. Bulović, and S. R. Forrest, "Efficient, high-bandwidth organic multilayer photodetectors," *Applied Physics Letters,* vol. 76, pp. 3855, June 2000.

[2] M. Pope and C. E. Swenberg, *Electronic Processes in Organic Crystals and Polymers.* Oxford: Oxford University Press, 1999.

Neodymium for Infrared Luminescent Solar Concentrator

P. D. Reusswig, C. Rotschild, M. A. Baldo
Sponsorship: DOE

Photovoltaic solar concentrators aim to increase the electrical power obtained from solar cells. Conventional solar concentrators track the sun to generate high optical intensities, often by using large mobile mirrors that are expensive to deploy and maintain. Solar cells at the focal point of the mirrors must be cooled and the entire assembly wastes space around the perimeter to avoid shadowing neighboring concentrators.

High optical concentrations without excess heating in a stationary system can be achieved with a luminescent solar concentrator (LSC) [1]. The LSC consist of a dye dispersed in a transparent waveguide. Incident light is absorbed by the dye and then reemitted into a waveguide mode. The energy difference between absorption and emission prevents reabsorption of light by the dye, isolating the concentrated photon population in the waveguide. Unfortunately, the performance of LSCs has been limited by two factors: self-absorption losses and a scarcity of dyes that absorb and emit efficiently in the infrared region. We have previously made significant progress on the problem of self-absorption losses [2]. Now we address operation in the infrared region.

Neodymium (Nd^{3+}) is nearly the optimal infrared LSC material: inexpensive, abundant, efficient, and spectrally well matched to high-performance silicon solar cells. It is a natural four-level system, reasonably transparent to its own radiation, and therefore capable of generating high optical concentrations. Neodymium is stable and well-understood because of its extensive application to high-power lasers. Neodymium's one disadvantage is its relatively poor overlap with the visible spectrum, meaning that it will require sensitization in the visible spectrum, as Figure 2 shows. The numerous possibilities for sensitizing Neodymium include inorganic nanocrystals for a fully inorganic LSC or organic dye molecules as used in conventional LSC technology. Figure 1 shows a schematic of the system. Neodymium should enable single LSC matched to silicon with efficiencies exceeding 10%.

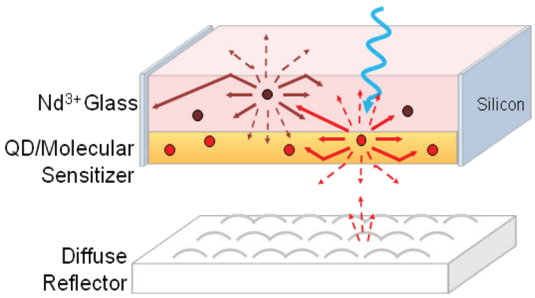


FIGURE 1: A schematic representation of an LSC. The LSC consists of Nd^{3+}-doped glass coated with a thin-film sensitization layer of organic dye or quantum-dot molecules and a diffuse back reflector. Solar radiation incident on the LSC is absorbed by the Nd^{3+} and reemitted as infrared radiation. The solar spectrum not absorbed by Nd^{3+} is captured and collected by the sensitization layer through radiative energy transfer to the Nd^{3+}.

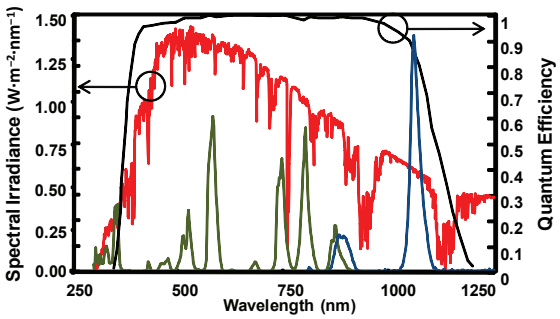


FIGURE 2: A comparison between the emission and absorption spectra (a.u.) of Nd^{3+} (green and blue, respectively); the AM1.5 solar radiation spectrum (red); and the external quantum efficiency of a Sunpower photovoltaic cell (black) [3].

REFERENCES

[1] W. H. Weber, and J. Lambe,"Luminescent greenhouse collector for solar radiation," Applied Optics, vol. 15, pp. 2299-2300 October 1976.

[2] M. J. Currie, J. K. Mapel, T. D. Heidel, S. Goffri and M. A. Baldo, "High-efficiency organic solar concentrator for photovoltaics," Science, vol. 321, pp. 226-228, July 2008.

[3] W. P. Mulligan, D. H. Rose, M. J. Cudzinovic, D. M. De Ceuster, K. R. McIntosh, D. D. Smith, and R. M. Swanson, "Manufacture of Solar Cells with 21 percent Efficiency," SunPower Corporation, 2004.

Efficiently Coupling Light to Superconducting Nanowire Single-photon Detectors

X. Hu, T. Zhong, F. Najafi, C. Herder, F. N. C. Wong, K. K. Berggren
Sponsorship: IARPA

We developed a superconducting nanowire single-photon detector (SNSPD) system in a close-cycled cryocooler with an overall detection efficiency above 20% and a dark count rate ~ 1000 counts/sec, as shown in Figure 1. The efficiency measurement was done for the wavelength of 1315 nm. This demonstration will enable many applications of SNSPDs such as quantum key distribution, deep-space optical communication, and defect-detection for integrated circuits.

In the past, we successfully developed a robust process to fabricate SNSPDs and demonstrated device detection efficiency above 50% at near-infrared wavelengths [1]. However, one of the technical challenges is how to efficiently couple light into SNSPDs because of the small active area of the SNSPD and its low temperature operation. To achieve efficient coupling, we fabricated a device with a relatively large area and, at the same time, a decent device detection efficiency; we also designed a chip package in a cryocooler. The detector was a circular one with a diameter of 9 µm (Figure 2 a) and b)) and its device efficiency was ~ 31%. In the chip package (Figure 2 c)), a fiber-focuser was used to shrink the spot-size of the light from a single-mode fiber down to 5 µm, and the nanopositioners were used to accurately adjust the position of the light spot *in-situ* three-dimensionally. The detector was directly connected with an SMA connector through wire bonding. The temperature of the chip was cooled down to 2.7 K in the cryocooler.

Using this plug-in SNSPD system (Figure 2 d)), we were able to measure flux and coincidence of entangled photons at infrared telecom wavelengths. Compared with other detection technologies (e.g., semiconductor avalanche photodiode counters), our detector system made these measurements an order of magnitude faster.

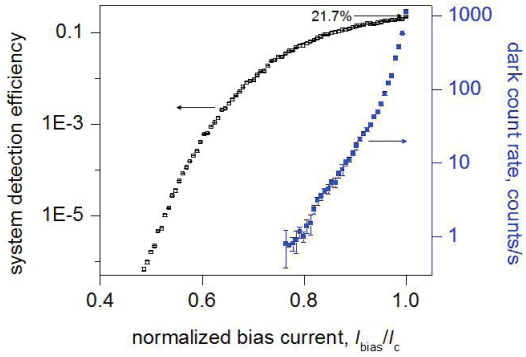


FIGURE 1: System detection efficiency and dark count rate of a single-photon detector inside a close-cycled cryocooler. The incident light is at the wavelength of 1315 nm.

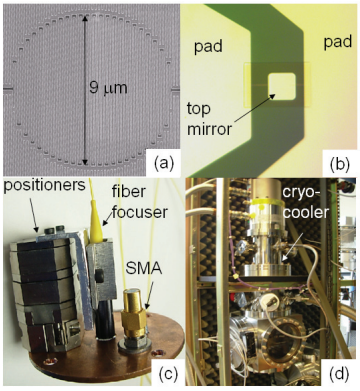


FIGURE 2: a) A scanning-electron microscope image of a circular nanowire single-photon detector with a diameter of 9 mm; b) A top view, optical microscope image of the detector with cavity-integration [1]. c) The chip package. Note that it is back-illumination, and the chip, aligned with the fiber-focuser, sits on the other side of the chip plate. d) The SNSPD system in a close-cycled cryocooler.

REFERENCES

[1] K.M. Rosfjord, J. K.W. Yang, E.A. Dauler, A. J. Kerman, V. Anant, B. M. Voronov, G. N. Gol'tsman, and K. K. Berggren, "Nanowire single-photon detector with an integrated optical cavity and anti-reflection coating," *Optics Express*, vol. 14, issue 2, pp. 527-534, Jan. 2006.

Guided-wave Devices for Holographic Video Display

D. Smalley, V. M. Bove, Jr., Q. Smithwick
Sponsorship: CELab, Digital Life, and Things That Think Research Consortia and Center for Future Storytelling, MIT Media Laboratory

We are developing a guided-wave optical modulator [1], [2] with 1-GHz composite bandwidth Surface Acoustic Wave (SAW) transducer arrays for use in video displays. This device is designed to diffract light horizontally and deflect it vertically through mode conversion by creating surface acoustic waves that interact with light trapped in waveguides on the surface of a lithium niobate substrate. To fabricate this modulator, we first mask a wafer of Z-cut lithium niobate with SiO_2 through a plasma-enhanced chemical vapor deposition (PECVD) process and then immerse it in heated benzoic acid and lithium benzoate to create single polarization waveguides. The waveguides are subsequently annealed to restore their acoustic properties. Finally, we pattern aluminum transducers onto the waveguides by conformal contact lithography employing a negative resist lift-off technique.

The goal of this work is to enable the inexpensive manufacturing of Scophony-architecture video displays [3] (both 2D and holographic video [4-7]) without the need for the horizontal scanning mirrors that typically limit the scalability of this technology.

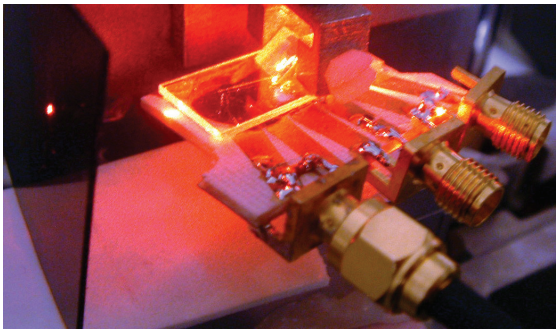


FIGURE 1: A device undergoing testing.

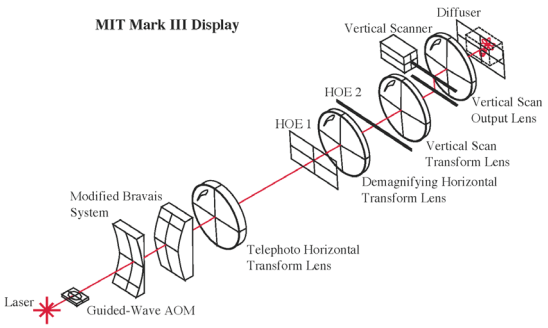


FIGURE 2: Architecture of our display system.

REFERENCES

[1] C.S. Tsai, Q. Li, and C.L. Chang, "Guided-wave two-dimensional acousto-optic scanner using proton-exchanged lithium niobate waveguide," *Fiber and Integrated Optics*, vol. 17, pp. 57-166, 1998.

[2] D. Smalley, "Integrated-optic holovideo," Master's thesis, Massachusetts Institute of Technology, Cambridge MA, 2006.

[3] H.W. Lee, "The Scophony television receiver," *Nature,* vol. 142, pp. 59-62, July 1938.

[4] D.E. Smalley, Q.Y.J. Smithwick, and V.M. Bove, Jr., "Holographic video display based on guided-wave acousto-optic devices," *Proc. SPIE Practical Holography XXI,* vol. 6488, p. 64880L, 2007.

[5] Q.Y.J. Smithwick, D.E. Smalley, V.M. Bove, Jr., and J. Barabas, "Progress in holographic video displays based on guided-wave acousto-optic devices," *Proc. SPIE Practical Holography XXII,* v. 6912, p. 69120H, 2008.

[6] Q.Y.J. Smithwick, J. Barabas, D.E. Smalley, and V.M. Bove, Jr., "Real-time shader rendering of holographic stereograms," *Proc. SPIE Practical Holography XXIII,* v. 7233, p. 723302, 2009.

[7] W. Plesniak, M. Halle, V.M. Bove, Jr., J. Barabas, and R. Pappu, "Reconfigurable image projection (RIP) holograms," *Optical Engineering,* vol. 45, p. 115801, Nov. 2006.

Exciton-exciton Annihilation in Organic Polariton Microcavities

G. M. Akselrod, J. R. Tischler, E. R. Young, M. S. Bradley, D. G. Nocera, V. Bulović

Sponsorship: CMSE, RLE, Hertz Foundation

Excitons in a solid can be coupled to the electromagnetic field by placing the material inside a resonantly tuned microcavity. If the decay rates of the excitons and the cavity mode are slower than the rate of energy exchange, the system takes on new eigenstates that are light-matter superpositions known as exciton-polaritons, and the limit of strong coupling is achieved. Recent work has demonstrated the use of organic thin films [1], [2] as the excitonic layer in polaritonic structures and the characteristic linear properties of these devices showed strong coupling. We present the first in-depth study of high-intensity optical excitation of such organic exciton-polariton devices.

The excitonic component of our devices was made of the 5.1 ± 0.1 nm film of J-aggregated cyanine dye TDBC assembled using layer-by-layer growth [3], giving an extremely high absorption coefficient of 10^6 cm^{-1}. The cavity was formed by sputter-depositing a 4.5 pair distributed Bragg reflector (DBR) on a quartz substrate, followed by a $\lambda/4n$ SiO_2 spacer layer, where n is the index of refraction and λ = 595 nm, the peak of the J-aggregate emission (Figure 1a). The J-aggregate film was then deposited, followed by a 100±1 nm spin coated layer of polyvinyl alcohol, which enhances the photoluminscence quantum yield of the J-aggregate film and acts as a spacer layer. A transparent thermally evaporated organic layer forms the remainder of the spacer, and the structure is capped with silver mirror, giving a cavity Q of ~60. The reflectivity as well as the photoluminscence (PL) of these devices shows two distinct resonances, which is characteristic of strong coupling (Figure 1).

To test for evidence of polariton lasing, the devices were pumped at λ = 535 nm at 60° relative to normal and the PL was collected at normal incidence. To fully characterize the behavior of the devices in a wide range of power regimes, three pump sources were utilized: a CW laser at 532 nm, a 10-ns pulsed laser at 535 nm, and a 150-fs pulsed laser at 535 nm. With CW excitation, all of the devices showed linear PL intensity as a function of input power. With 10-ns excitation, the PL began to show a sublinear power law dependence (p = 0.535), with the effect becoming more pronounced with 150-fs excitation (p = 0.348) (Figure 2a and b). Devices with a range of tunings as well as cavities with higher Q (~115) were tested and all showed the same qualitative sublinear behavior. A similar sublinear behavior was observed in J-aggregate thin films that were not situated in a cavity. We propose the process of exciton-exciton annhilation as a possible mechanism to explain the reduction of quantum yield with increasing intensity. Previous studies have shown the existence of exciton-exciton annihilation in cyanine dye J-aggregates [5], and it is a phenomenon observed in other excitonic materials that are candidates for organic polariton lasing. Annihilation would be a process directly in competition with polariton-polariton scattering—inherently an exciton-exciton interaction—which is a possible mechanism for populating the k = 0 state of the polariton dispersion and achieving room-temperature organic polariton lasing.

REFERENCES

[1] D. G. Lidzey, D. D. C. Bradley, M. S. Skolnick, T. Virgili, S. Walker, and D. M. Whittaker, "Strong exciton-photon coupling in an organic semiconductor microcavity," *Nature*, vol. 395 pp. 53-55, 1998.

[2] J. R. Tischler, M. S. Bradley, Q. Zhang, T. Atay, A. Nurmikko, and V. Bulović, "Solid state cavity QED: Strong coupling in organic thin films," *Organic Electronics* vol. 8, no. 2-3, pp. 94-113, 2007.

[3] M. S. Bradley, J. R. Tischler, and V. Bulović, "Layer-by-layer J-aggregate thin films with a peak absorption constant of 10(6) cm(-1)," *Advanced Materials*, vol. 17, no. 15, pp. 1881-1884, 2005.

[4] L. Kelbauskas, S. Bagdonas, W. Dietel, and R. Rotomskis, "Excitation relaxation and structure of TPPS4 J-aggregates," *Journal of Luminescence*, vol. 101, pp. 253-262, 2003.

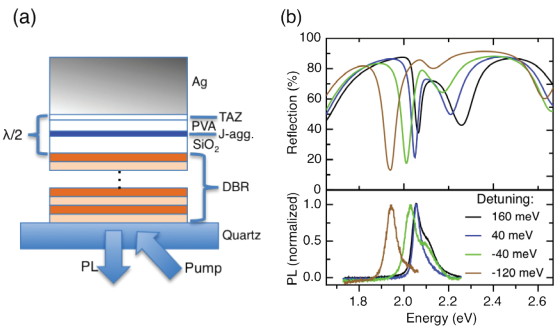


FIGURE 1: (a) A DBR-metal microcavity with a J-aggregate excitonic layer and a total optical thickness of ~λ/2 where λ = 595 nm. (b) The reflectivity of devices having different cavity-exciton detunings and the corresponding PL.

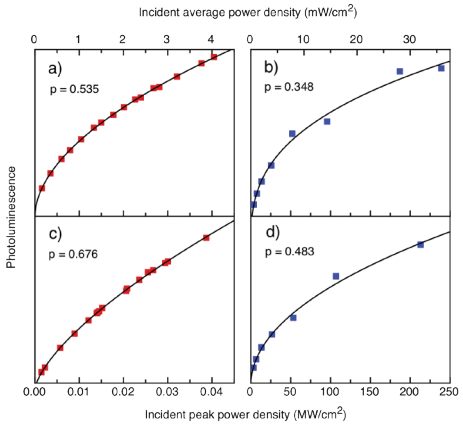


FIGURE 2: The PL vs. intensity for: microcavity pumped with 535 nm (a) 10 ns laser (b) 150 fs laser; and a J-aggregate thin film pumped same two lasers.

Heterojunction Photovoltaics Using Printed Colloidal Quantum Dots as the Photosensitive Layer

A. C. Arango, S. Geyer, M. G. Bawendi, V. Bulović
Sponsorship: ISN, DOE Solar America Program

Colloidal quantum dot (QD) systems offer distinct optical and electronic properties that are not easily attained by other nanostructured semiconductors, such as highly saturated emission in QD light-emitting-diodes, access to infrared radiation in QD photodetectors, and the prospect of optically optimized solar cell structures [1]. The prevailing deposition method for colloidal QD systems is spin-casting, which introduces limitations such as solvent incompatibility with underlying films and the inability to pattern side-by-side pixels for multispectral photodetector arrays. In the present work we employ a non-destructive microcontact printing method [2], which allows for deposition of a thin quantum dot film onto a wide-band-gap organic hole transport layer, N,N'-Bis (3-methylphenyl)-N,N'-bis-(phenyl)-9,9-spiro-bifluorene (spiro-TPD), thus producing an inorganic/organic heterojunction that serves to enhance charge separation in the device. The top and bottom contacts are provided by ITO electrodes, allowing for near-transparency (Figure 1).

Restrictions imposed by transport losses in the QD film are found to limit charge generation. Measurements of the external quantum efficiency (EQE) and internal quantum efficiency (IQE) as a function of QD film thickness, plotted in Figure 2, reveal a marked dependence on thickness. The IQE is determined by dividing the EQE by the absorption of the QD film, all of which are measured at the first absorption peak of the QD film (λ = 590 nm). Following excitation and exciton diffusion to an interface, dissociation of the exciton produces free carriers that must diffuse to opposite electrodes in order to produce a photocurrent. A model that accounts for both exciton and charge diffusion reproduces the general thickness trend, assuming an exciton diffusion length L_{Ex} = 43 nm, an electron diffusion length L_{EI} = 61 nm, and near-zero contribution from the first two QD monolayers. Further development will require reducing exciton and charge transport losses in order to permit efficient charge-generation from thicker QD films with improved absorption.

REFERENCES

[1] D.C. Oertel, M.G. Bawendi, A.C. Arango, and V. Bulović. "Photodetectors based on treated CdSe quantum-dot films," *Applied Physics Letters*, vol. 87, no. 21, p. 213505, Nov. 2005.

[2] A. C. Arango, D. C. Oertel, Y. Xu, M. G. Bawendi, and V. Bulović. "Heterojunction photovoltaics using printed colloidal quantum dots as a photosensitive layer," *Nano Letters*, vol. 9, no. 2, pp. 860–863, Feb. 2009.

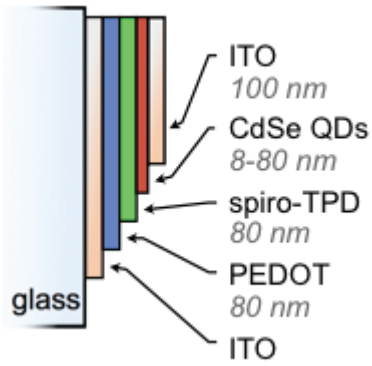


FIGURE 1: The QD heterojunction device architecture used in this work accommodates QD film thicknesses varying from 8 to 80 nm.

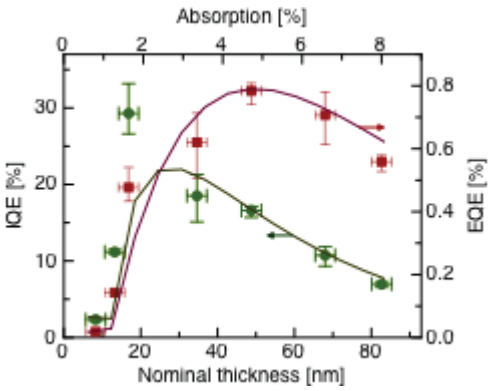


FIGURE 2: External quantum efficiency (EQE) (red squares) and internal quantum efficiency (IQE) (green circles) at l = 590 nm versus nominal QD film thickness and device absorption at l = 590 nm. An analytical model for the EQE (red line) and IQE (green line) reproduces the general trend with thickness. Nominal thicknesses are calculated assuming an absorption coefficient of 104 cm-1 at l = 590 nm.

Patterned Organic Microcavities for Confinement of Exciton-Polaritons

M. S. Bradley, J. R. Tischler, G. Akselrod, V. Bulović
Sponsorship: NDSEG, ISN

We demonstrate fabrication of organic laterally-patterned microcavity devices with lateral sizes on the micron scale using PDMS lift-off patterning. Recently, low-threshold lasing was demonstrated from pillars formed by thermally evaporating thin films of Alq_3 (aluminum tris(8-hydroxyquinoline)) doped with the laser dye DCM (4-(dicyanomethylene)-2-methyl-6-(4-dimethylaminostyryl)-4H-pyran) through thin nickel shadow masks with square, 5- x 5-μm^2 openings [1]. Additionally, recent research efforts in microcavity exciton-polariton devices based on inorganic active materials such as GaAs or CdTe quantum wells have focused on the lateral patterning of microcavity exciton-polariton systems [2]. Such 0D cavities allow for symmetry-breaking of the in-plane wave vector, opening new pathways for parametric generation of photon pairs [3]. For the same reason, laterally-patterned organic microcavity exciton-polariton devices are also of interest. The PDMS lift-off patterning, as opposed to shadow masking, allows standard lithography techniques to be used to define pattern features in silicon PDMS molds [4], [5]. Additionally, smaller features than are achievable through shadow masking are theoretically feasible even with PDMS due to the generally low aspect ratio in PDMS needed for embossing small features on the patterned organic film.

We use PDMS lift-off patterning of a thin film of thermally-evaporated TPD (N'-bis(3-methylphenyl)-N,N'-diphenyl-1,1'-biphenyl-4,4'-diamine) doped with DCM to form embossed pillars in the TPD film of 20-25 nm in thickness. Figure 1a shows the device structure, Figure 1b shows PDMS lift-off patterning technique, and Figure 1c shows the molecular diagrams of the device constituents. When the sample is optically excited with a λ=408 nm light source, emission from both the unpatterned (λ~630 nm) and patterned areas (λ~655 nm) is observed, as seen in Figure 2. The background emission dominates since its cavity resonance is closer to the resonance of DCM, as shown; use of different organic materials with larger lift-off amounts can increase this wavelength shift.

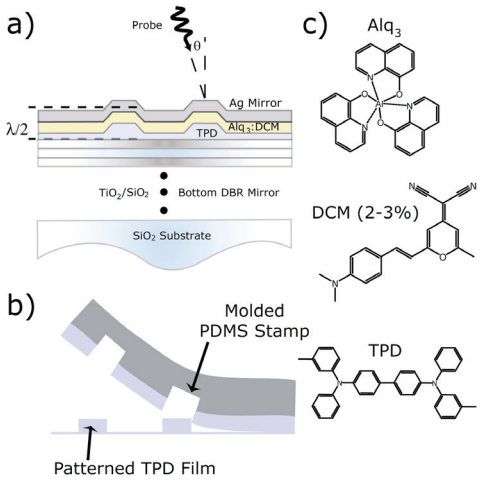


FIGURE 1: (a) Patterned microcavity structure. (b) The PDMS lift-off patterning process. (c) Molecular structures of constituent materials.

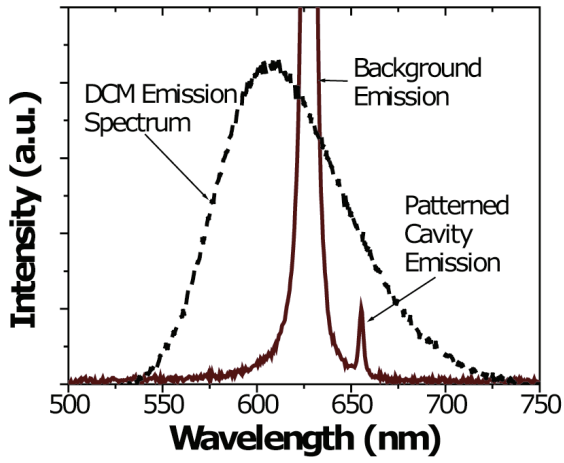


FIGURE 2: Emission spectrum of DCM with unpatterned (background) and patterned microcavities when excited with λ=408 nm.

REFERENCES

[1] M. Sudzius, M. Langner, S. I. Hintschich, V. G. Lyssenko, H. Frob, and K. Leo, "Multimode laser emission from laterally confined organic microcavities," *Applied Physics Letters*, vol. 94, 2009.

[2] O. El Daif, A. Baas, T. Guillet, J. P. Brantut, R. I. Kaitouni, J. L. Staehli, F. Morier-Genoud, and B. Deveaud, "Polariton quantum boxes in semiconductor microcavities," *Applied Physics Letters*, vol. 88, 2006.

[3] D. Bajoni, E. Peter, P. Senellart, J. L. Smirr, I. Sagnes, A. Lemaitre, and J. Bloch, "Polariton parametric luminescence in a single micropillar," *Applied Physics Letters*, vol. 90, 2007.

[4] J. Yu and V. Bulović, "Micropatterning metal electrode of organic light emitting devices using rapid polydimethylsiloxane lift-off," *Applied Physics Letters*, vol. 91, 2007.

[5] J. Yu, "Improving OLED Technology for Displays," Doctoral thesis, Elec. Eng. and Comp. Sci., Mass. Inst. of Tech., Cambridge, MA, 2008.

Heterojunction Photodetector Consisting of Metal-oxide and Colloidal Quantum-dot Thin Films

T. P. Osedach, N. Zhao, L.-Y. Chang, S. M. Geyer, A. C. Arango, J. C. Ho, M. Bawendi, V. Bulović

Sponsorship: ISN, DOE Solar America Program

We demonstrate a heterojunction photodetector consisting of a metal-oxide charge transport layer and a colloidal quantum-dot (QD) charge-generation layer. To make the device, a metal-oxide semiconductor, SnO_2, is sputter-deposited over an array of interdigitated gold electrodes. A thin film of PbS QDs is then spin-coated over the structure (see Figure 1a). The optical and electrical characteristics of the device can be optimized independently through the modification of these two layers.

The metal-oxide and QD layers form a type-II hetero-interface (Figure 1b) suitable for dissociating photogenerated excitons. Exciton dissociation at the interface results in the generation of holes in the QD layer and electrons in the metal-oxide layer. A bias corresponding to a field of $\sim 10^4$ V/cm is applied across the electrodes to facilitate carrier collection. The increased electron density increases the metal-oxide film conductivity, which in turn manifests an increase in lateral current through the device. A plot of the spectrally resolved external quantum efficiency is shown in Figure 2, with high efficiency response matching the spectral response of quantum-dot absorption.

This work builds on previous reports from our laboratory in which an organic/organic photodetector [1] and an organic/QD photodetector [2] were described. The present device can be driven at reduced bias and extends spectral sensitivity into the infrared region. The unique ability to independently tune the optical and electrical characteristics of these structures makes them a valuable platform with which to study the physical processes at QD hetero-interfaces.

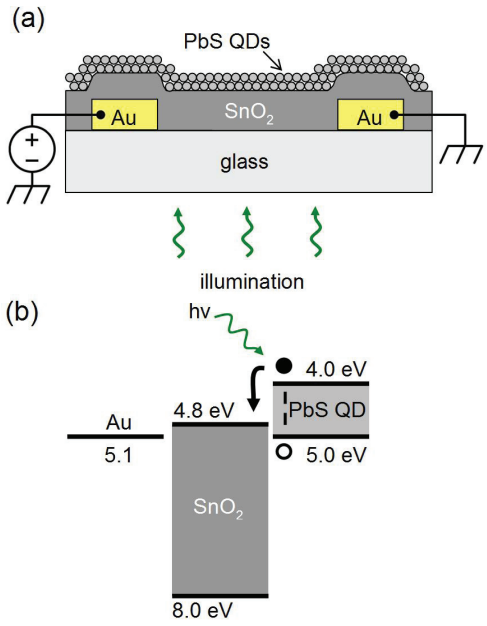


FIGURE 1: (a) Schematic of the device structure. (b) Energy band diagram. Excitons dissociate at the interface between the metal-oxide film and the quantum dots.

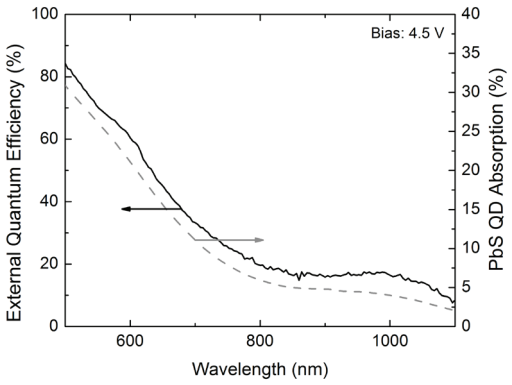


FIGURE 2: External quantum efficiency spectrum (solid) and PbS QD absorption (dashed).

REFERENCES

[1] J. Ho, A. Arango, and V. Bulović, "Lateral organic bilayer heterojunction photoconductors", *Applied Physics Letters*, August 2008.

[2] T. P. Osedach, S. M. Geyer, J. C. Ho, A. C. Arango, M. G. Bawendi, V. Bulović, "Lateral heterojunction photodetector consisting of molecular organic and colloidal quantum dot thin films", *Applied Physics Letters*, January 2009.

Heterojunction Photoconductors for Chemical Detection

J. C. Ho, J. A. Rowehl, V. Bulović
Sponsorship: ISN, CMSE

We have developed and demonstrated a solid-state sensor platform that directly transduces the chemosignal of a fluorescent polymer-chemical interaction into photocurrent. In addition to the direct transduction mechanism, the sensor separates the chemosensing and conduction processes across the two different films, enabling independent optimization of each film to serve a specific function [1]. Conceptually, the device consists of a Type-II bilayer heterojunction deposited on planar electrodes that enables the application of an electric field in-plane with the interface. The bilayer heterojunction is realized by spin-casting a chemosensitive fluorescent polymer on top of a sputtered metal oxide film.

Figure 1 depicts device operation: 1) absorption of illumination creates excitons, 2) excitons diffuse to the interface, 3) band offsets enable efficient exciton dissociation into free carriers, and 4) transport of photogenerated, free carriers in the photoconductive channel. The presence of an analyte will strongly modulate the photoluminescence (PL) efficiency of the chemosensitive fluorescent polymer, which signifies a change in the population of excitons that can radiatively decay [2]. Altering the exciton population changes the carrier concentration at the heterointerface, which results in a change in the measured photocurrent.

Initial testing of bilayer sensors, incorporating various polymers as the EGL and SnO_2 (doped 30% O_2) as the CTL, demonstrates an upper sensitivity limit to TNT detection of approximately 10 picograms of material in a few seconds. Figure 2 compares the spectral response of a 100-nm film of SnO_2 to a bilayer device (100 nm SnO_2/5nm HW polymer) before and after exposure to saturated TNT vapor. The inset shows the real-time change in photoconductivity at the absorption peak of the polymer when TNT vapor is introduced at time t = 0. These results prove the bilayer sensor concept and hold promise for the development of a sensitive, highly specific, portable chemical sensor platform with potential for a wide array of applications.

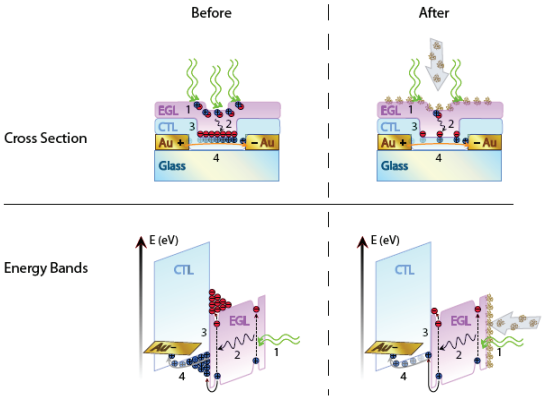


FIGURE 1: Energy band diagrams and cross-sections of bilayer sensor consisting of an exciton generation layer (EGL) and a charge transport layer (CTL) before and after exposure to a particular analyte.

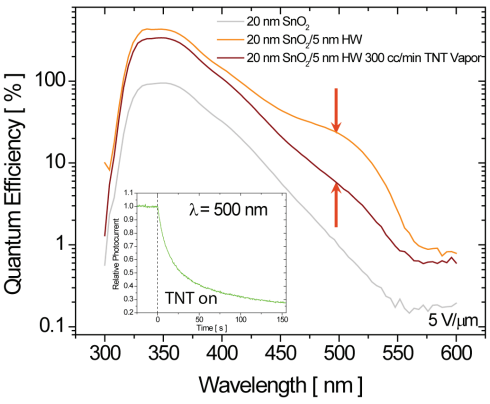


FIGURE 2: Semilogarithmic spectral response plot of HW polymer/SnO2 bilayer sensor before (orange) and after (brown) saturated TNT vapor exposure. Response of 20-nm SnO2 film (grey) is shown for comparison. Inset: Time response of TNT sensing action at ë = 500 nm. TNT vapor is introduced at time t = 0 s.

REFERENCES

[1] J. Ho, A. Arango, and V. Bulović, "Lateral Organic Bi-layer Heterojunction Photoconductors," *Applied Physics Letters*, vol. 93, 063305, August 2008.

[2] S. W. Thomas, G. D. Joly, and T. M. Swager, "Chemical Sensors Based on Amplifying Fluorescent Conjugated Polymers," *Chemical Review*, vol. 107, pp. 1339-1386, March 2007.

Multi-layer Heterojunction Photoconductors

J. C. Ho, J. A. Rowehl, V. Bulović
Sponsorship: ISN, CMSE

We fabricate a two-terminal, lateral multi-layer photoconductor consisting of three molecular organic thin films with cascading energy bands (see Figure 1): the charge transport layer (CTL), N,N'-bis(3-methylphenyl)-N,N'-diphenyl-1,1'-biphenyl-4,4'-diamine (TPD); the charge spacer layer (CSL), N,N'-bis-(1-naphthyl)-N,N' –diphenyl-1,1-bipheny1-4,4'-diamine (NPD); and the exciton-generation layer (EGL), 3,4,9,10-perylenetetracarboxylic bis-benzimidazole (PTCBI). Placing an interstitial spacer layer between the CTL and the EGL improves the photogenerated current of tri-layer photoconductors over bi-layer, Type-II heterojunction photoconductors.

Light excitation acts as a pseudo- "gate electrode" by generating excitons in PTCBI (EGL). Those excitons diffuse to the PTCBI/NPD interface, where they dissociate, leaving the electron behind in PTCBI, while the hole is initially injected into NPD from where it can transfer to the more energetically favorable states in TPD. Excess holes in the TPD film raise the hole-carrier concentration in the TPD film and increase the device conductance by forming a channel of excess carriers at the TPD/NPD interface. The thin film of NPD (CSL), between TPD (CTL) and PTCBI (EGL), spatially separates the dissociated carriers, reducing the likelihood of bimolecular recombination across the TPD/PTCBI interface. Bi-layer heterojunction photoconductors consisting of TPD and PTCBI alone have been shown to improve the external quantum efficiency over single layers of TPD and PTCBI by several orders of magnitude [1], [2]. Measurement of the current at an optical excitation wavelength of 532 nm from a biased multi-layer, lateral heterojunction device [Au/TPD(50 ± 0.5) nm/NPD(4 ± 1) nm/PTCBI(50 ± 0.5) nm] displays improvement by a factor of eight over the bi-layer without a CSL (see Figure 2). A thickness study of the NPD spacer layer experimentally demonstrates the dependence of the photoresponse efficiency on the spatial separation of the dissociated charge.

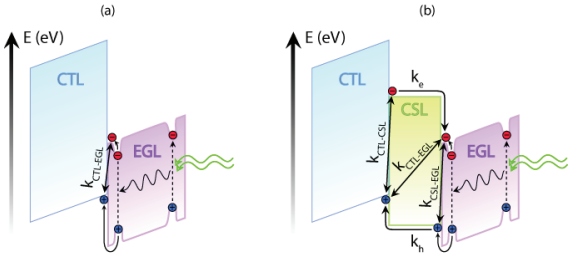


FIGURE 1: Energy-band diagrams of (a) a bilayer device consisting of CTL/EGL and (b) a trilayer device consisting of CTL/CSL/EGL. Relevant interfacial recombination rates and carrier diffusion rates are depicted.

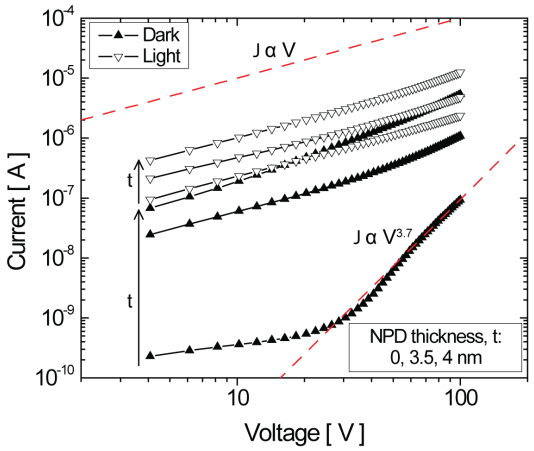


FIGURE 2: Log-log current-voltage characteristics of TPD 50 ± 0.5 nm TPD/NPD/50 ± 0.5 nm PTCBI, with 0, 3.5, and 4 nm of NPD. Arrows indicate increasing NPD thickness and dashed red lines are guides that depict ohmic and trap-limited conduction.

REFERENCES

[1] J. Ho, J. Rowehl, and V. Bulović, "Organic Multi-layer Lateral Heterojunction Phototransistors," presented at Electronic Materials Conference, Santa Barbara, CA, June 2008.

[2] J. Ho, A. Arango, and V. Bulović, "Lateral Organic Bi-layer Heterojunction Photoconductors," Applied Physics Letters, vol. 93, 063305, August 2008.

3-molecular-layers-thick J-aggregate Photoconductor

Y. Shirasaki, J. Ho, M. S. Bradley, J. R. Tischler, V. Bulović

Sponsorship: ISN, Solar Revolutions Center at MIT, NSF MRSEC

Due to their record high absorption constant and narrow photoluminescence linewidth [1], thin films of J-aggregated cyanine dyes have been extensively studied with respect to their potential applications in novel opto-electronic devices, such as organic light emitting diodes, optical switches, and lasers. J aggregates' strong absorption is especially interesting for use in light sensing devices like a photoconductor. A J-aggregate film that is only a few nanometers thick, in conjunction with a dielectric mirror, has an ability to absorb almost 100% of incoming light [2] at normal incidence.

We demonstrate in this study an efficient lateral J-aggregate photoconductor. Our device structure is a bi-layer heterojunction consisting of an optically active 5 nm thick TDBC J-aggregate thin film, which serves as the primary exciton generation layer, and a 50 nm layer of zinc indium oxide (ZIO) underneath, which serves as a charge transport layer. The contacts which sit below the ZIO are series of gold interdigitated fingers photolithographically defined on glass. The bi-layer structure physically separates the light absorption and charge transport regions of the device, taking advantage of the J aggregates' unique optical properties and the ZIO's charge transport properties. We observe that the heterojunction significantly increases the efficiency of the device by assisting the dissociation of the excitons, similar to the work reported by J. Ho *et al* [3]. External quantum efficiency (EQE), defined as the change in number of electrons passing through the bi-layer device per incident photon is shown in Figure 1. EQE greater than 100 % suggests that the exciton recombination lifetime is greater than the transit time of the electrons passing through the device. The curve follows the absorption curve of ZIO and the J aggregates shown in the inset. Figure 2 shows the time response of the bi-layer device.

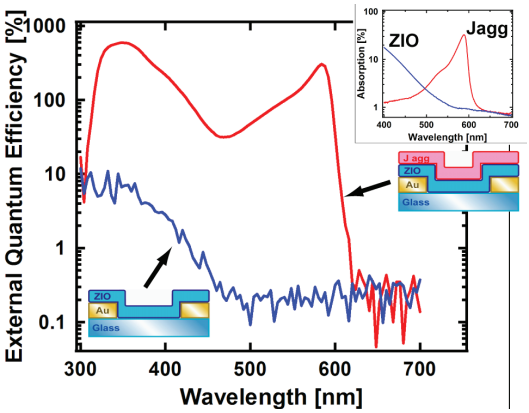


FIGURE 1: External quantum efficiency of the bi-layer device as a function of the incident light wavelength. The inset is the absorption curves of ZIO and TDBC J aggregates. The efficiency of the device is significantly improved where the J aggregates absorb light.

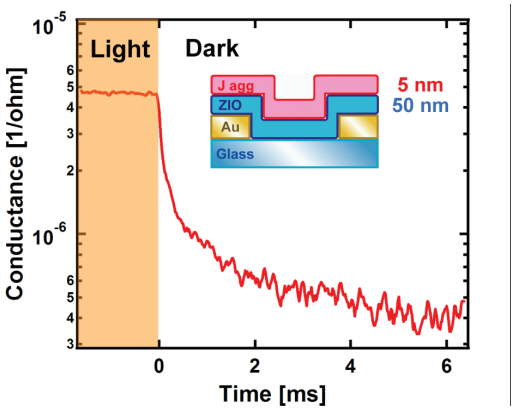


FIGURE 2: Time response of the bi-layer device using a LED light source peaked around 595 nm.

REFERENCES

[1] M. S. Bradley, J. R. Tischler and V. Bulović, "Layer-by-layer J-aggregate thin films with a peak absorption constant of 10^6 cm^{-1}," *Advanced Materials, vol. 17, no. 15, pp. 1881-1886, August 2005.*

[2] J. R. Tischler, M. S. Bradley and V. Bulović, "Critically coupled resonators in vertical geometry using a planar mirror and a 5 nm thick absorbing film," *Optics Letters*, vol. 31, no. 13, pp. 2045-2047, July 2006.

[3] J. C. Ho, A. Arango and V. Bulović, "Lateral organic bilayer heterojunction photoconductors," *Applied Physics Letters*, vol. 93, no. 6, pp. 063305, August 2008.

Strong Light-matter Coupling Using a Robust Non-cyanine Dye J-aggregate Material

J. R. Tischler, G. M. Akselrod, M. S. Bradley, J. Chan, E. R. Young, D. G. Nocera, T. M. Swager, V. Bulović

Sponsorship: ISN

We demonstrate strong light-matter coupling using a promising new J-aggregate material based on a dibenz[a,j]anthracene macrocycle [1], Figure 1a, that is robust under high power optical excitation. Strong light-matter coupling leads to polaritonic resonances that are superpositions of the underlying excitonic and photonic states [2] and can exhibit laser-like coherent light emission at remarkably low excitation densities due to polariton condensation [3]. A key hindrance to achieving polariton condensation thus far using cyanine dye J-aggregates has been exciton-exciton annihilation [4], which quenches excitations from the polaritonic states before they can condense. The J-aggregates of the dibenz[a,j]anthracene-based macrocycle show no signs of exciton-exciton annihilation until optical excitation densities exceeding 20 MW/cm^2, while in thin films of a typical J-aggregated cyanine dye, TDBC, annihilation appears at 10 kW/cm^2. Thin films of the macrocycle were prepared by spin-coating a 6 mg/ml solution of the dye in chlorobenzene, yielding layers that were 15 nm thick with an RMS roughness of less than 1 nm. The J-aggregation of the dye in these films was evidenced by the appearance of a narrow absorption line at 465 nm of FWHM = 15 nm, Figure 1b, and the concomitant disappearance of the monomer absorption band as the dye concentration was increased [1]. The films possess an absorption coefficient of 2.1 x 10^5 cm^{-1} at the J-aggregate absorption peak wavelength of 465 nm, show good photochemical stability, and have photoluminescence quantum yield exceeding 90%. Strong coupling was observed when thin films of the macrocycle were situated in a λ/2n planar optical microcavity consisting of a silver mirror and dielectric Bragg reflector. Devices exhibit polaritonic dispersion with a room temperature Rabi-splitting of 130 meV, Figure 2. Experiments are underway to demonstrate organic-based polariton condensation.

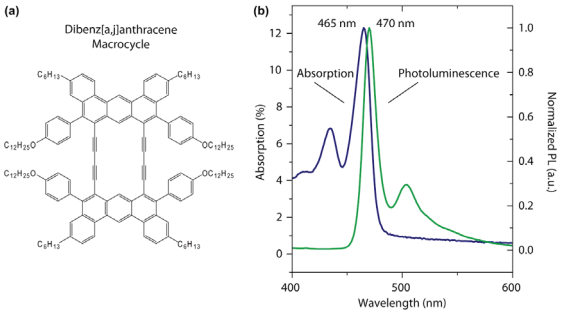


FIGURE 1: (a) Chemical structure of dibenz[a,j]anthracene-based macrocycle. (b) Optical absorption and photoluminescence spectra from a thin film prepared by spin-coating the compound onto a glass substrate. Thin film roughness of less than 1 nm was observed in AFM.

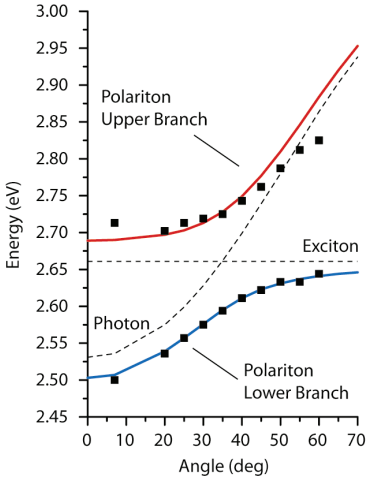


FIGURE 2: Polaritonic dispersion relation derived from angular device reflectance data. Anti-crossing of energy levels is observed at 35° from normal.

REFERENCES

[1] J. M. W. Chan, J. R. Tischler, S. E. Kooi, V. Bulović, T. M. Swager, "Synthesis of J-Aggregating dibenz[a,J]anthracene-based macrocycles", *Journal of the American Chemical Society*, vol. 131, pp. 5659-5666, April 2009.

[2] C. Weisbuch, M. Nishioka, A. Ishikawa, and Y. Arakawa, "Observation of the coupled exciton-photon mode splitting in a semiconductor quantum microcavity", *Physical Review Letters*, vol. 69, pp. 3314 – 3317, May 1992.

[3] J. Kasprzak J, M. Richard, S. Kundermann, A. Baas, P. Jeambrun, J. M. J. Keeling, F. M. Marchetti, M. H. Szymanska, R. Andre, J. K. Staehli, V. Savona, P. B. Littlewood, B. Deveaud, L. S. Dang, "Bose-Einstein condensation of exciton polaritons", *Nature*, vol. 443, pp. 409-414, September 2006.

[4] J. Moll, W. J. Harrison, D. V. Brumbaugh, A. A. Muenter, "Exciton annihilation in J-aggregates probed by femtosecond fluorescence upconversion", *Journal of Physical Chemistry A*, vol. 104, pp. 8847-8854, October 2000.

Low-threshold Coherently-coupled Organic VCSEL

J. R. Tischler, E. R. Young, D. G. Nocera, V. Bulović
Sponsorship: ISN

Here we report observation of extremely low-threshold lasing in organic VCSELs when the excitons are coherently coupled non-radiatively to each other. Non-radiative coupling between excitons can enhance the emission cross-section of a gain material and lead to laser action at considerably lower excitation densities [1]. The coupling strength associated with the excitonic interaction is proportional to the number of excited molecules at any given time; hence the effect necessitates creating the exciton population quickly relative to the excited state decay time. This phenomenon is often referred to as superradiance [1], [2]. In organic semiconductor VCSELs, this effect leads to a 95% reduction in threshold when sub-psec non-resonant excitation is utilized to create the exciton population, instead of a longer nsec duration pump pulse. The VCSELs consist of a thermally evaporated gain layer composed of the laser dye DCM doped (2.5 % v/v) into an Alq_3 host matrix, which is situated between a metal mirror and a dielectric Bragg reflector (DBR). In VCSELs where the gain layer is "λ/2n thick", i.e., 156.7 nm, an extremely low threshold of 4.9 μJ/cm² is observed. This marks the first time lasing from organics has been reported in a metal/DBR half-wavelength thick microcavity, despite the rather modest resonator quality factor of $Q < 200$. Lasing is confirmed by supra-linear input-output power dependence and by spectral and spatial line-narrowing above the threshold. Moreover, when the optical excitation is polarized, the emission above the threshold strongly follows the polarization of the pump light. All prior demonstrations of laser action in solid-state organic VCSEL structures have utilized either gain layers of at least 3 times the thickness [3] or have relied on higher finesse of all dielectric microcavities [4]. The observed laser threshold of 4.9 μJ/cm² in the half-wavelength thick microcavity corresponds to excitation of at most 3.2% of the DCM molecules.

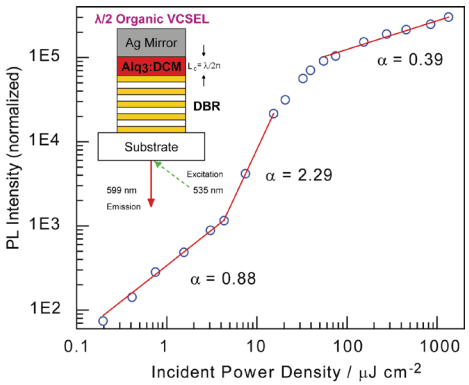


FIGURE 1: Input/Output power dependence upon direct DCM excitation (l_{ex} = 535 nm) shows the lasing threshold at 4.9 μJ/cm² incident power and superlinear slope α = 2.29 when fit to power law, $y = mx^{\alpha}$. Inset: Device design consists of a dielectric Bragg reflector (DBR), organic semiconductor gain layer, and silver mirror. The sample is excited at q = 60° from normal using TM polarized laser light focused down to a spot size of 0.001 cm² as measured on the sample plane.

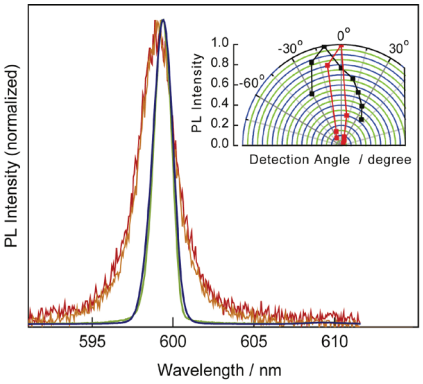


FIGURE 2: Emission spectra of OVCSEL at different power levels above and below the threshold show linewidth narrowing from 2.5 nm for excitation below threshold (, 3.25 μJ/cm²; , 8 μJ/cm2) to 1.1 nm above threshold (, 15 μJ/cm²; , 250 μJ/cm²). Inset: Emission cone spatially narrows from from Dq = ± 30° to Dq = ± 5° as measured at the emission peak.

REFERENCES

[1] L. Moi, P. Goy, M. Gross, J. M. Raimond, C. Fabre, and S. Haroche, "Rydberg-atom masers. I. A theoretical and experimental study of super-radiant systems in the millimeter-wave domain", Physical Review A, vol. 27, pp. 2043-2064, April 1983.

[2] R. H. Dicke, "Coherence in Spontaneous Radiation Processes", *Physical Review*, vol. 93, pp. 99-110, January 1954.

[3] V. Bulović, V. G. Kozlov, V. B. Khalfin, and S. R. Forrest, "Transform-limited, narrow-linewidth lasing action in organic semiconductor microcavities", *Science*, vol. 279, pp. 553-555, January 1998.

[4] M. Koschorreck, R. Gehlhaar, V. G. Lyssenko, M. Swoboda, M. Hoffmann, and K. Leo, "Dynamics of a high-Q vertical-cavity organic laser", *Applied Physics Letters*, vol. 87, pp. 181108:1-3, October 2005.

Electroluminescence from Phosphor-doped Nanocrystals

V. Wood, J. E. Halpert, M. J. Panzer, M. G. Bawendi, V. Bulović
Sponsorship: ISN, CMSE, PECASE, NDSEG

Alternating current thin-film electroluminescent (AC-TFEL) devices already occupy a segment of the large-area, high-resolution, flat-panel-display market. The AC-TFEL displays, which consist of a phosphor layer, such as manganese doped-zinc sulfide (ZnS:Mn), vertically sandwiched between two insulators that are contacted by electrodes, are robust, possess long lifetimes, and offer high luminance with relatively low power consumption [1], [2]. While fabrication of AC-TFEL devices has been the subject of considerable study over the past three decades, significant challenges remain. Development of multicolor displays with balanced red, green, and blue (RGB) emission has proven difficult as the most efficient red, green, and blue phosphors comprise different materials systems that require different deposition and annealing steps. Transparent AC-TFEL displays have recently been demonstrated by Sharp, Inc.; however, the processing of the phosphor to achieve transparency is difficult and has not yet been developed for phosphors other than ZnS:Mn [3].

We present a novel materials system for solution processing of the active phosphor layer in transparent AC-TFEL devices. We use colloidally-synthesized Mn-doped nanocrystals interspersed between RF magnetron sputtered ZnS layers to demonstrate electroluminescence (EL) from a solution-deposited active layer in an AC-TFEL device fabricated at room temperature [4]. We adapt the synthesis of Thakar *et al*. to make stable ZnSe/ZnS:Mn/ZnS nanocrystals with quantum yields of (65±5)% [5]. As Figure 1 shows, these wide band gap host nanocrystals along with sputtered wide band-gap metal oxides (Al_2O_3, HfO_2, and ITO) enable transparent AC TFEL devices without additional processing steps beyond the room-temperature layer-by-layer deposition of each material set. Our devices exhibit electroluminescence from the Mn dopants at frequencies greater than 10 kHz and with voltages as low as 110 V_{pp} (See Figures 1 and 2) [4].

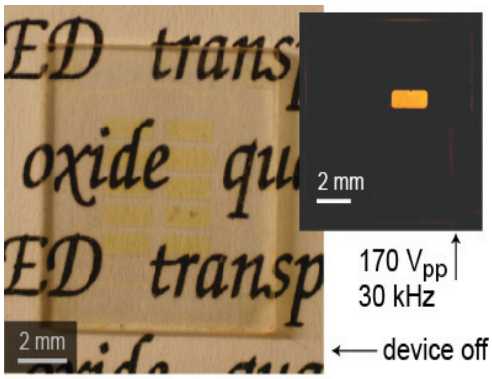


FIGURE 1: A photograph of a 0.5 in. x 0.5 in. glass substrate containing ten 1 mm x 2 mm AC-TFEL devices, with no bias applied. The substrate is pictured on top of printed text to demonstrate the transparency of our AC-TFEL device architecture. The inset shows the uniformity of pixel illumination (in the dark) with the device operating at 170 V_{pp} and 30 kHz.

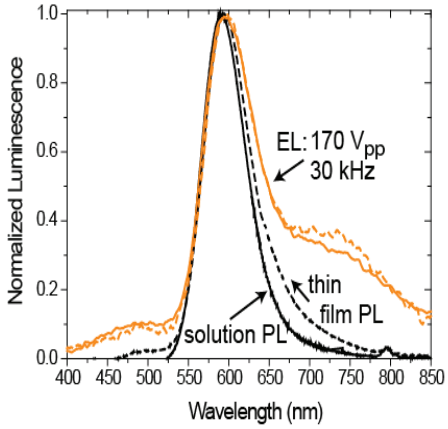


FIGURE 2: Electroluminescent (EL) spectra for devices with Al_2O_3 and HfO_2 insulating layers (solid and dashed orange curves, respectively). Photoluminescence (PL) spectra of the nanocrystal solution (solid gray curve) and a completed device (dashed black line). The overlap of the spectral peaks indicates that the emission is due to the Mn impurity dopants.

REFERENCES

[1] Y. A. Ono, *Electroluminescent Displays*. Singapore: World Scientific, 1995.

[2] J.P. Keir and J.F. Wager, "Electrical Characterization of Thin-Film Electroluminescent Devices," Annu. Rev. Mat. Sci., vol 27, 1997, pp. 223-248.

[3] A. Abileah, K. Harkonen, A. Pakkala, and G. Smid. *Transparent Electroluminescent (EL) Diplays*, Planar Systems, 2008.

[4] V. Wood, J.E. Halpert, M.J. Panzer, M.G. Bawendi and V. Bulović, "Alternating Current Driven Electroluminescence from ZnSe/ZnS:Mn/ZnS Nanocrystals," *Nano Lett.*, vol. 9, no. 6, Apr. 2009, pp. 2367–2371

[5] R. Thakar, Y. Chen, and P.T. Snee, "Efficient Emission from Core/(Doped) Shell Nanoparticles: Applications for Chemical Sensing," *Nano Lett.*, vol. 7, no. 11, Oct. 2007., pp. 3429-3432.

High-efficiency, Low-cost Photovoltaics using III-V on Silicon Tandem Cells

P. Sharma, B. Yu, M. Bulsara, E. A. Fitzgerald
Sponsorship: Chesonis Family Foundation

Photovoltaics and sustainability have received a lot of attention lately. We seek a tandem photovoltaic device using silicon as both the substrate and lower cell and GaAsP as the upper cell. The ideal band gaps for this two-cell tandem structure with silicon at 1.1eV and GaAsP at 1.75 eV allows access to the highest efficiency possible for a two-cell tandem, 36.5%. The lattice mismatch between GaP and Si is 0.37%; therefore, these two materials constitute a nearly ideal combination for the integration of Si and III–V semiconductor-based technologies. Defect-free heteroepitaxy of GaP on Si has nevertheless been a major challenge.

We are working on two approaches to building a III-V solar cell on top of a silicon solar cell. Both approaches use the same materials systems; however, in the first approach, a purely planar structure is built while in the second approach the geometry of the fabricated structure aids in creating the requisite material quality as shown in Figure 1 and Figure 2, respectively. Both the planar approach and the patterned approach are viable research paths to bring an optimal tandem cell using a 1.1eV mature silicon cell as part of the tandem. One is a layered wafer-scale approach, whereas the other is a patterned wafer-scale approach. Both promise to produce important scientific information as well as potential paths to economical high-efficiency tandem solar cells. Further, it is quite possible that a combination of the approaches will be most effective, that is, a patterned approach together with grading transition layers. Metal Organic Chemical Vapor Deposition (MOCVD) and Atomic Layer Deposition (ALD) techniques, which are central to the thin film fabrication approaches, are being currently used.

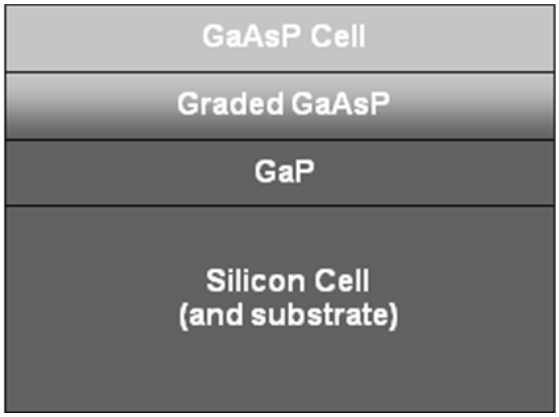


FIGURE 1: Schematic illustration of the planar approach. Note: the layers are not to scale. The Si substrate would typically be 200 μ thick and the other layers a few microns each.

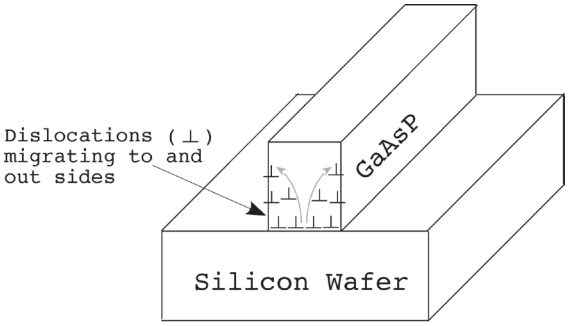


FIGURE 2: Schematic of linear GaAsP structure grown on silicon wafer showing outgrowth of dislocations.

Co-axial Integration of III-V Ridge-waveguide Gain Elements with SiO_xN_y Waveguides on Silicon

S. Famenini, J. Diaz, C. G. Fonstad, Jr.

Sponsorship: Vitesse Chair

Our ongoing research integrating 1.55-μm III-V ridge waveguide gain elements (i.e., diode lasers and semiconductor optical amplifiers) co-axially aligned with and coupled to silicon oxy-nitride waveguides on silicon substrates has made significant strides in the past year. We are working towards the goal of co-axially coupling III-V laser diodes and semiconductor optical amplifiers with waveguides on Si wafers; to do so, we use techniques consistent with fabricating waveguides on Si-CMOS wafers and integrating the III-V gain elements after all standard front- and back-end Si processing has been completed.

A novel micro-cleaving technique has been used to produce active ridge waveguide platelets on the order of 6 μm thick and 100 μm wide, with precisely controlled lengths (in the current work 300 ± 1.25 μm) and very high-quality end facets. Typical ridge guide platelet lasers have thresholds under 30 mA.

Passive micro-cleaved platelets have been integrated within dielectric recesses etched through the oxy-nitride (SiO_xN_y) waveguides on a wafer so that the ridge and SiO_xN_y waveguides are co-axially aligned. Transmission measurements indicate coupling losses are as low as 5 db with air filling the gaps between the waveguide ends, and measurements made through filled gaps indicate that the coupling losses can be reduced to below 1.5 dB with a high index (n = 2.2) dielectric fill. Simulations indicate that with further optimization of the mode profile in the III-V waveguide, the loss can be reduced to below 1 dB.

We have also performed extensive device design and optimization for co-axial recess integration and have recently completed a comparison of co-axial coupling with the evanescently coupled III-V/Si hybrid integration approach recently introduced by researchers at UCSB and Intel. The latter comparison revealed that the approach we have taken, co-axial end-fire coupling, and the UCSB/Intel approach, vertical evanescent coupling, are complementary, with each optimal for certain applications. At the same time it pointed out a number of distinct advantages for co-axial coupling of recess-integrated platelet lasers including higher operating efficiency, smaller device footprint, greater flexibility in choice of materials, lower cost, higher modularity, and easier integration of different wavelength emitters [1].

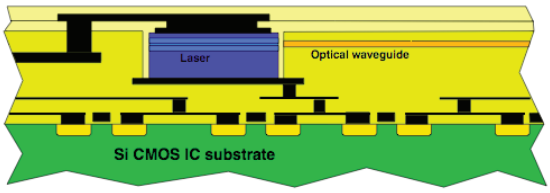


FIGURE 1: A cartoon illustrating the recess-mounting and co-axial alignment approach to integrating III-V gain elements (edge-emitting in-plane laser diodes, EELs, and semiconductor optical amplifiers, SOAs) with silicon oxy-nitride waveguides on silicon integrated-circuit chips and silicon photonic integrated-circuits platforms.

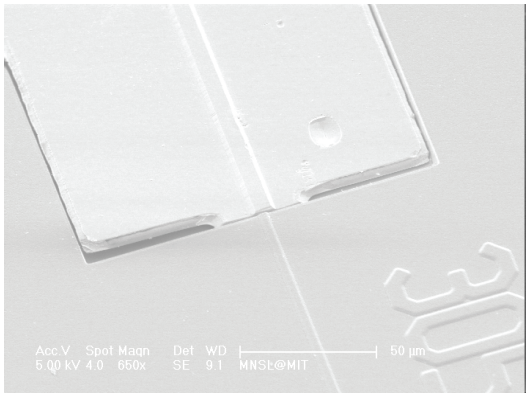


FIGURE 2: A close-up photomicrograph showing the alignment between an InGaAsP/InP ridge waveguide platelet and a buried silicon oxy-nitride waveguide. Coupling losses as low as 3 dB were measured.

REFERENCES

[1] C.G. Fonstad, J.J. Rumpler, E.R. Barkley, J.M. Perkins, and S. Famenini, "Recess Integration of Micro-cleaved Laser Diode Platelets with Dielectric Waveguides on Silicon," *Proc. of the Novel In-plane Semiconductor Lasers Conference VII*, Photonics West 2008, SPIE Conference Proc. vol. 6909, 2008, pp. 69090O-1 to 69090O-8,

Light-proof Electrodes for In-situ Monitoring of Neural Function

A. Zorzos, C. G. Fonstad, Jr. in collaboration with E. Boyden
Sponsorship: MIT Media Lab Director's Innovator Award

In recent years Professor Boyden's group has developed optogenetic reagents for neuroscience, starting with channelrhodopsin-2 (ChR2) and N. pharaonis halorhodopsin (Halo/NpHR), as well as other novel and useful reagents (Arch, spHalo, and Mac) that enable neural circuits to be activated and silenced with different colors of light [1]. Among other reasons for the importance of these technologies, they make it possible to record spiking activity concurrently with optical neuromodulation, due to the lack of the fast electrical stimulus artifact that results from electrical stimulation. However, multiple groups have observed that metal electrodes of many kinds exhibit a slow artifacts under exposure to bright light while immersed in brain tissue (or saline), with frequencies in the range of Hz to tens of Hz, thus obscuring the recording of local field potentials. This phenomenon is consistent with a classical photoelectrochemical finding, the Becquerel effect, in which illumination of an electrode placed in saline can produce a significant voltage on the electrode.

Accordingly, Boyden's group has set out to devise and test strategies for coating metal electrodes to make them insensitive to light when immersed in the brain.

The Fonstad and Boyden groups have also begun a collaboration to use standard photolithographic and micro-fabrication techniques to produce linear arrays of light-proof electrodes for high-density recording of neural spikes and field potentials (in the style of the "Michigan probe"). For both of these strategies, the transparent conductor indium tin oxide (ITO) is being used. In the collaborative effort, dense linear arrays of electrodes have been fabricated from ITO-coated substrates. The electrodes have an impedance (measured in saline, at 1 kHz) of 1 megaohm, with no detectable light artifact. Techniques are now being developed to fashion linear insertable probes with many (e.g., 40) light-proof ITO recording sites while maintaining a thin, tissue-damage-minimizing (e.g., 150 × 150 micron) cross-section.

Such novel probes will allow artifact-free recordings during optical neuro-modulation, enabling the systematic analysis of real-time neural dynamics across multiple time scales, via causal neural control tools. For translational efforts, such devices as described here may be important for assessing the effects of optical neural control on the treatment of intractable brain disorders.

REFERENCES

[1] X. Han and E.S. Boyden, "Multiple-Color Optical Activation, Silencing, and Desynchronization of Neural Activity, with Single-Spike Temporal Resolution," *PLoS ONE* vol. 2, no. 3, p. e299, March 2007.

Low-threshold Vertical Cavity Surface-emitting Lasers Recess- integrated within Silicon CMOS Integrated Circuits

J. M. Perkins, C. G. Fonstad, Jr.
Sponsorship: NSF

Optoelectronic devices intimately integrated on silicon integrated circuits have long been sought for optical intercon-nect applications in an effort to improve data transfer rates in high performance circuits. A new heterogeneous integration technique for integrating vertical-cavity surface-emitting lasers (VCSELs) on silicon CMOS integrated circuits for such applications has been developed and demonstrated for the first time in our group at MIT [1], [2].

Fully processed and tested oxide-aperture VCSELs emitting at 850 nm have been fabricated as individual "pills" 55 μm in diameter and 8 μm tall with a disk contact on the n-type backside and a ring contact on the p-type, emitting top-side. With a custom micro-pipette vacuum pick-up tool, these pills are placed on contact pads at the bottom of recesses etched though the dielectric overcoating on a Si-CMOS chip; when all the recesses on the chip are filled, the pills are batch-solder-bonded in place. Back-end processing of the chip then continues with surface planarization, contact via formation, and interconnect metal-deposition and patterning. A completely integrated pill appears in Figure 1.

The integrated VCSEL characteristics appear in Figure 2. They have threshold currents of 1 to 2.5 mA and thermal impedances as low as 1.6 °C per mW, both of which are similar to native substrate device thresholds and impedances. Thermal modeling of these devices has also been performed, investigating the impact of integration on VCSEL-device operation. The results show potential thermal impedance improvements for both single and arrayed devices due to integration on silicon. This model also investigates the impact of integration on a dielectric stack, as well as the impact of the current aperture of the VCSEL device.

The technique demonstrated in this work integrates devices as individual pills within the dielectric stack covering a Si IC, allowing for wafer-scale monolithic processing of heterogeneous circuits. The process effectively avoids thermal expansion mismatch limitations, and it is compatible with parallel assembly techniques such as fluidic self-assembly.

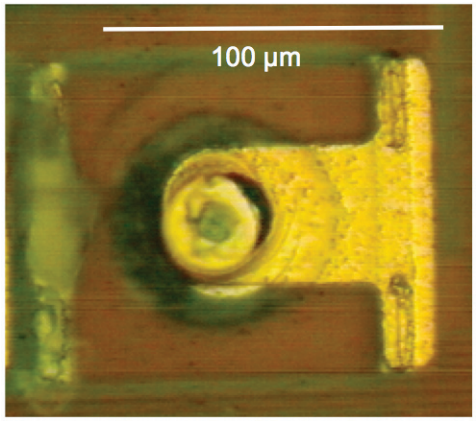


FIGURE 1: A microphotograph of a fully integrated VCSEL in its recess on a CMOS chip showing the upper contact pattern connecting the VSCEL to the underlying circuitry. The emission comes from the small aperture in the contact pattern roughly in the center of the picture. Figure 2 shows the CW drive and output characteristics of the VCSEL.

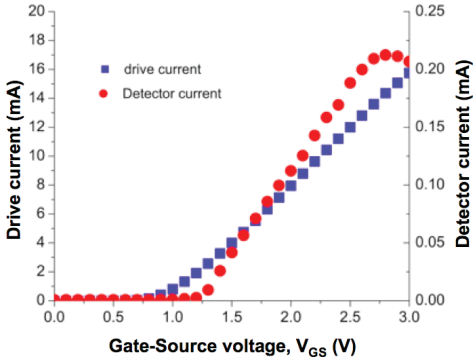


FIGURE 2: The CW drive and output characteristics of an integrated VCSEL driven by an on-chip transistor circuit. The diode current (left axis) and optical output (detector current, right axis) are plotted as a function of the gate-to-source voltage applied to the n-MOS drive transistor. The MOSFET threshold voltage is ~ 1 V, and the VCSEL threshold is ~ 2 mA.

REFERENCES

[1] J.M. Perkins, and C.G. Fonstad, "Full Recess Integration of Small Diameter Low Threshold VCSELs within Si-CMOS ICs," *Optics Express*, vol. 16, no. 18, pp. 13955-13960, 2008.

[2] J.M. Perkins, "Low threshold vertical cavity surface emitting lasers integrated onto Si-CMOS ICs using a novel hybrid assembly technique," Ph.D. thesis, Massachusetts Institute of Technology, 2007.

Micro-cleaved Laser Diode Platelets Integrated on Silicon

J. Rumpler, C. G. Fonstad, Jr.
Sponsorship: DARPA through ARL; Lincoln Laboratory IPI Program

Thin (6-μm) InP-based multiple-quantum-well (MQW) ridge laser platelets emitting at a wavelength of 1550 nm have been manufactured and integrated by metal-to-metal bonding onto silicon substrates. These laser platelets can be thought of as freestanding optoelectronic building blocks that can be integrated as desired on diverse substrates. These blocks are fully processed lasers, with both top-side and bottom-side electrical contacts. The thinness of these optoelectronic building blocks and the precision with which their dimensions are defined are conducive to assembling them in dielectric recesses on a substrate such as silicon as part of an end-fire coupled optoelectronic integration strategy [1]. They are assembled by a micro-scale pick-and-place technique that allows the blocks to be picked up individually and placed as desired on the substrate of choice. Final integration is accomplished using pressurized polymer film to hold the platelets in place as they are metal-to-metal solder-bonded to the Si substrate.

To enable the manufacture of these laser platelets, a novel micro-cleaving process technology has been developed that uses notched bars of lasers as shown in Figure 1 to accurately locate the point of cleavage. This novel micro-cleaving process is used to simultaneously obtain both smooth end facets and precisely defined cavity lengths. As a proof of concept, this process has been shown to achieve nominal cavity lengths of 300 μm +/- 1.25 μm. We believe that this micro-cleaving process can be used to make thin platelet lasers having much shorter cavity lengths and that with minor adjustments it can be used to achieve better-than-1-μm-length precision.

For the 300-μm-long, 6-μm-thin, micro-cleaved ridge platelet lasers integrated onto silicon substrates, as shown in Figure 2, continuous-wave lasing at temperatures as high as 55°C and pulsed lasing at temperatures to at least 80°C have been achieved. These lasers have output powers as high as 26.8 mW (at T = 10.3°C), differential efficiencies as high as 81% (at T = 10.3°C), and threshold currents as low as 18 mA (at T = 10.3°C). The characteristic temperatures, T_0 and T_1, of the lasers on silicon were 43 K and 85 K, respectively. The thin micro-cleaved ridge platelet lasers integrated onto silicon outperformed conventionally cleaved multiple-quantum-well (MQW) ridge lasers on their native InP substrate in terms of thermal characteristics, output power, and differential efficiency [2].

REFERENCES

[1] C.G. Fonstad, J.J. Rumpler, E.R. Barlkley, J.M. Perkins, and S. Famenini, "Recess Integration of Micro-cleaved Laser Diode Platelets with Dielectric Waveguides on Silicon," *Proc. of the Novel In-plane Semiconductor Lasers Conference VII, Photonics West 2008*, SPIE Conference Proc. vol. 6909, 2008, pp. 69090O-1 to 69090O-8,

[2] J.J. Rumpler and C.G. Fonstad, Jr., "Continuous-wave Electrically Pumped 1.55 µm Edge-emitting Platelet Ridge Laser Diodes on Silicon," *IEEE Photonics Technology Letters*, July 2009, in press.

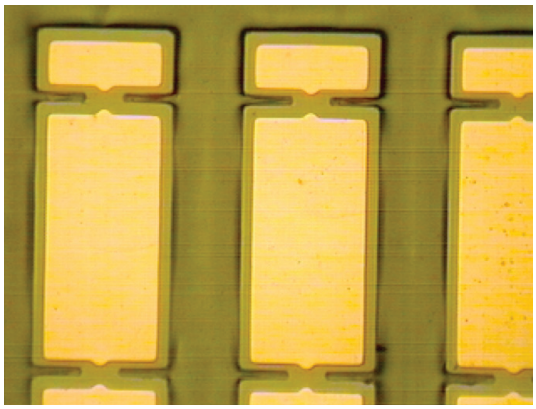


FIGURE 1: A back-side view of platelet lasers bars after front-side processing has been completed and the wafer has been mounted face-down on a carrier wafer, the substrate removed, and the back-side metal deposited and patterned. The bars will next be released and micro-cleaved to produce individual platelet lasers approximately 150-µm wide and 300-µm long.

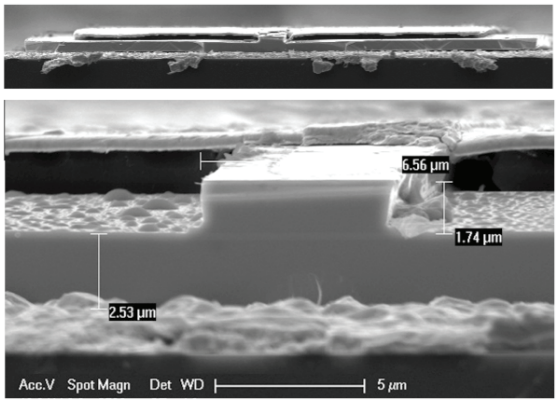


FIGURE 2: Close-up photomicrographs showing, in the top portion of the figure, a platelet bonded on a silicon wafer. A close-up view of the micro-cleaved end facet and the ridge waveguide is shown in the lower portion of the figure. Note also the stripe ohmic contact on top of the mesa and the broad-area top contact pad (insulated by a BCB support layer).

Waveguide Micro-probes for Optical Control of Excitable Cells

A. Zorzos, C. G. Fonstad, Jr. in collaboration with E. Boyden
Sponsorship: MIT Media Lab Director's Innovator Award

Professor Ed Boyden uses light to precisely control aberrant neuron activity. His lab has invented safe, effective ways to deliver light-gated membrane proteins to neurons and other excitable cells (e.g., muscle, immune cells, pancreatic cells, etc.) in an enduring fashion, thus making the cells permanently sensitive to being activated or silenced by millisecond-timescale pulses of blue and yellow light, respectively [1]. This ability to modulate neural activity with a temporal precision that approaches that of the neural code itself holds great promise for human health, and his lab has developed animal models of epilepsy and Parkinson's disease to explore the use of optical control to develop new therapies. His work has attracted international attention and appeared in numerous articles, including a recent piece in the Science Times section of *The New York Times* [2] and a profile of his lab for the Discovery Channel's "Top 5 Science Stories of the Year."

Professors Boyden and Fonstad have initiated a collaborative effort to use heterogeneous integration techniques developed in Fonstad's laboratory to construct miniature linear probes to deliver light to activate and silence neural target regions along their length as desired. The goal is to develop mass-fabricatable multiple light guide microstruc-tures produced using standard microfabrication techniques. Each probe is a 200- to 250-micron-wide insertable micro-structure comprising many miniature lightguides running in parallel and delivering light to many points along the axis of insertion. Such a design maximizes the flexibility and power of optical neural control while minimizing tissue damage. By building 2-D arrays of such probes, we can deliver multiple colors of light to 3-dimensional patterns in the brain, at the resolution of tens to hundreds of microns, thus furthering the causal analysis of complex neural circuits and dynamics. Such devices will allow the substrates that causally contribute to neurological and psychiatric disorders to be systematically analyzed via causal neural control tools. Given recent efforts on testing such reagents in nonhuman primates, these devices may also enable a new generation of optical neural control prosthetics, contributing directly to the alleviation of intractable brain disorders.

The initial light-guide structures have been fabricated from silicon nitride clad with silicon dioxide, and tests show good transmission of red light with no visible loss in the taper and bend regions of the patterns. Significantly, the novel 90° bend invented to direct light laterally out the side of the narrow probe (visible in both Figures 1 and 2) appears to function as designed, although much more work is needed to fully quantify the performance. The test mask contains a variety of guide structures and a series of measurements is underway to quantify the losses in straight sections of various widths, through different radius bends and sections with different degrees of taper and around the 90° bends. Work on the fabrication of visible-emitting platelet laser diodes to be integrated with the guides will also begin soon.

REFERENCES

[1] X. Han and E.S. Boyden, "Multiple-Color Optical Activation, Silencing, and Desynchronization of Neural Activity, with Single-Spike Temporal Resolution," PLoS ONE vol. 2, no. 3, p. e299, March 2007.

[2] I. Chen, "The Beam of Light That Flips a Switch That Turns on the Brain," New York Times, Science Section, Aug. 14, 2007, p. D1.

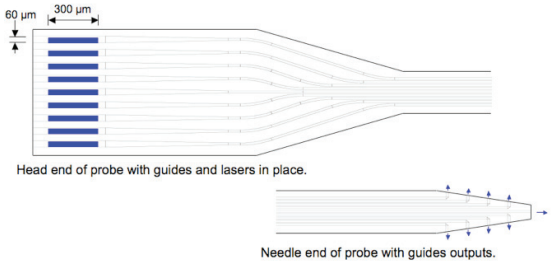


FIGURE 1: A schematic drawing of the head and needle ends of a light-guide probe with nine laser inputs (an actual probe will have many more inputs and outputs). The output of the waveguide can be seen more clearly in Figure 2; note that the drawing in Figure 2 is not to scale and an actual probe will be much longer.

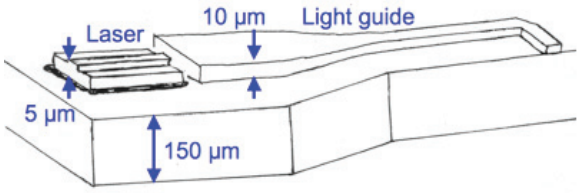


FIGURE 2: A perspective sketch of a platelet laser diode aligned with the input of a multi-mode rectangular dielectric waveguide and bonded on a contact pad. This cartoon illustrates the type of micro-scale assembly and integration proposed for the light-guide probe.

Development of Terahertz Quantum-cascade Lasers

S. Kumar, A. Lee, A. Hsu, Q. Qin, T. Kao, D. Burghoff, I. Chan, Q. Hu, in collaboration with J. Reno, Sandia National Lab.
Sponsorship: NSF, NASA, AFOSR, DOD NGSEG fellowship

The terahertz frequency range (1-10 THz) has long remained undeveloped, mainly due to the lack of compact, coherent radiation sources. Transitions between subbands in semiconductor quantum wells were suggested as a method to generate long wavelength radiation at customizable frequencies. However, because of difficulties in achieving population inversion between narrowly separated subbands and mode confinement at long wavelengths, THz lasers based on intersubband transitions were developed only very recently. Taking a completely novel approach, we have developed THz quantum-cascade lasers based on resonant-phonon-assisted depopulation and using metal-metal waveguides for mode confinement. The schematics of both features are illustrated in the top-left figure. Based on the combination of these two unique features, we have developed many THz QCLs with record performance, including a maximum pulsed-operating-temperature at 164 K (top right), a maximum cw-operating-temperature at 117 K (bottom right), and the longest wavelength (~141 μm) QCL to date without the assistance of magnetic fields (bottom left).

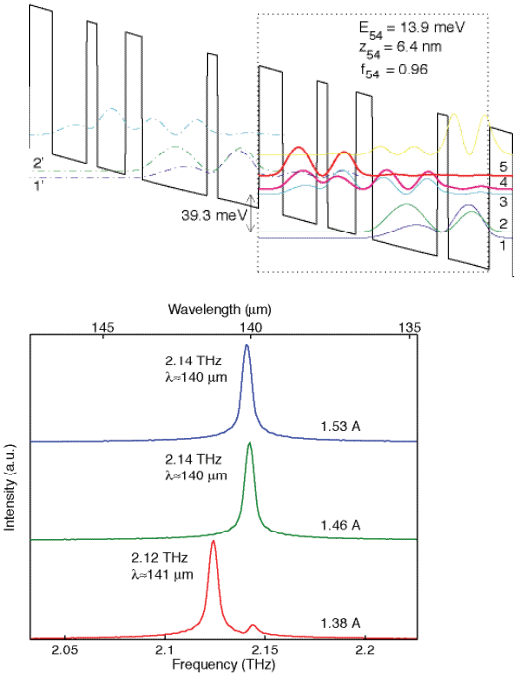


FIGURE 1: Magnetization as a function of applied field.

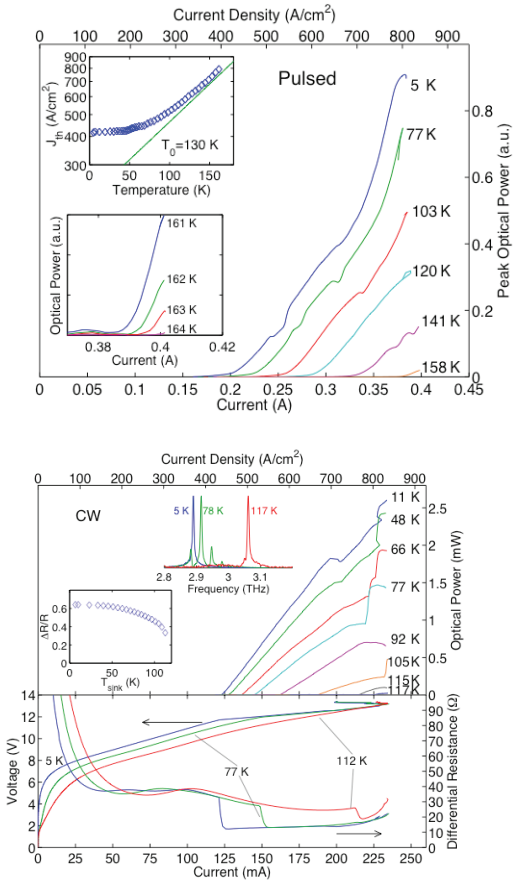


FIGURE 2: Magnetization as a function of applied field.

Ge-based Thermo-photovoltaic Cells

J. Cheng, J. Liu, L. C. Kimerling, J. Michel
Sponsorship: MIST Collaboration

A thermo-photovoltaic (TPV) cell is a narrow-band-gap semiconductor device that can absorb long wavelength photons from a hot object and convert them into electric power. The working temperature range of the hot object is 1500K to above 2000K. We have proposed the use of epitaxially grown Ge-on-Si TPV cells. The Ge has a narrow band gap (0.66eV indirect gap, 0.80ev direct gap), high hole-mobility, and CMOS process compatibility. By using hetero-epitaxial Ge on Si, we will achieve additional advantages for TPV applications in terms of cost and efficiency. This system is cost-effective because the size of the Ge epitaxial layer is determined by the Si substrate. Meanwhile, epitaxial Ge on Si is tensile-strained because of the different thermal expansion coefficients of Si and Ge. This strain effectively shrinks the band gap, which allows the collection of longer wavelengths of radiation from a hot surface.

The optimal thickness for the Ge absorption layer in a TPV cell is between 2 to 3μm for heat sources at T=2000K. The appropriate oxide thickness for selective Ge growth should be above 1.5μm. The sidewall roughness and slope will influence the Ge quality and leakage current. Two etch processes can be used to form the oxide windows: dry plasma etch and wet buffered oxide etch (BOE). A plasma oxide etch delivers the required straight sidewalls for Ge growth. During use of a plasma oxide etch for oxide thicker than 500nm, a polymer by-product of the etch process will accumulate at the bottom of the oxide window. This polymer cannot be removed easily, therefore resulting in defective Ge growth. If a BOE etch is used, the sidewalls of the window will be sloped, preventing a complete fill of Ge during epitaxial growth. Therefore we combined a 500-nm dry etch with a short BOE etch. The BOE etch can remove the polymer that was formed during the dry-etch process. We limited the dry-etch process to 500nm and used several etch cycles to etch 1.8μm oxide. This way we were able to arrive at a clean Si surface for good Ge growth and straight sidewalls. Figure 1 shows an SEM image of the etched oxide mesa. The image shows smooth sidewalls and a clean Si surface. Figure 2 shows a thin Ge film grown inside the mesa. Ge clearly grows along the oxide sidewall.

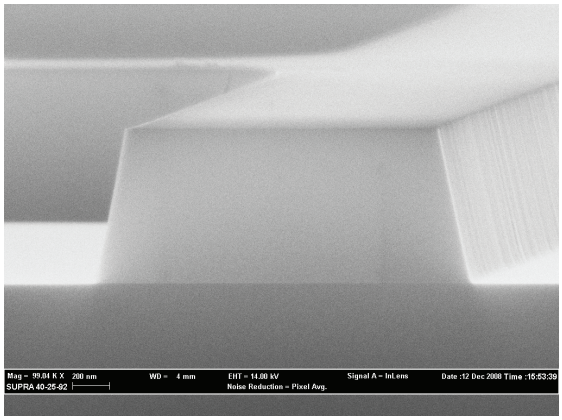


FIGURE 1: An SEM image of 2 cycles of dry and wet etched oxide walls.

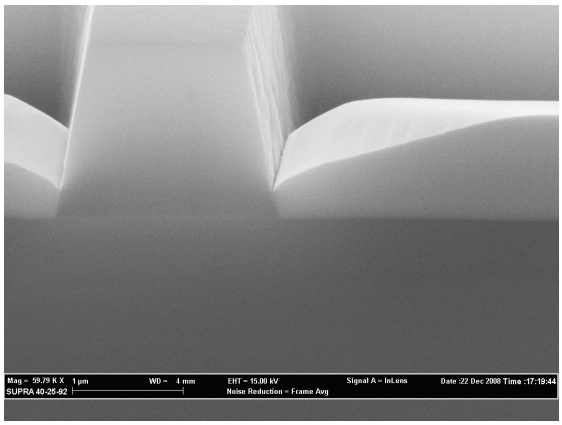


FIGURE 2: An SEM image of Ge grown in a 1.8-µm-deep oxide mesa.

Cavity-enhanced Photosensitivity in Chalcogenide Glass

J. Hu, M. Torregiani, F. Morichetti, N. Carlie, L. Petit, A. Agarwal, A. Melloni, K. Richardson, L. C. Kimerling
Sponsorship: DOE

Chalcogenide glasses, namely the amorphous compounds of sulfur, selenium and/or tellurium, have emerged as a promising material candidate for nonlinear optics in recent years due to their high Kerr nonlinearity and low two-photon absorption (TPA), giving rise to a superior nonlinear figure of merit (FOM) compared to conventional semiconductor materials such as silicon.

Here nonlinear absorption, infrared photosensitivity, and thermal stability characteristics of the glass material are tested in a cavity-enhanced setting. The chalcogenide glass resonators are patterned by lift-off entirely using a 500-nm CMOS line [1], [2]. In the nonlinear optical measurements, TM polarization light from a tunable laser is first amplified using an erbium-doped fiber amplifier (EDFA) and then end-coupled into the bus-waveguide through a silica optical fiber. Figure 1 plots the TM transmission spectra near a resonant peak of a 30-μm radius micro-disk at different input power levels. Corresponding nonlinear absorption in the optical resonator can be calculated using the generalized coupling matrix method based on the resonant peak extinction ratio change. The absorption value does not exhibit measurable increase within the accuracy of our testing setup, suggesting a TPA coefficient $\alpha_2 < 1.5 \times 10^{-13}$ m/W, almost two orders of magnitude smaller than that of silicon. Further, the resonant peak shape is significantly altered at input power levels higher than 17 dBm, a combined consequence of the index-trimming effect and thermo-optic instability. To further investigate the index-trimming effect due to 1550-nm light illumination, we perform pump-probe measurements to evaluate the refractive index change in As_2S_3 under non-resonant and resonant pumping conditions,. The resonant peak shift is negligible when the pump beam is not aligned with the resonant wavelength. However, significant resonant wavelength red shift is observed as the pump beam with an input power > 14 dBm is tuned to the resonant wavelength, which unequivocally confirms the cavity-enhancement due to infrared photosensitivity.

To summarize, we have performed systematic cavity-enhanced optical characterizations of As_2S_3 chalcogenide glass films using planar micro-disk resonators. No TPA is observed in the nonlinear measurements and the TPA coefficient is calculated to be $< 1.5 \times 10^{-13}$ m/W. We also characterize refractive index-trimming induced by resonant illumination of light at 1550 nm. A power-density threshold of < 0.1 GW/cm^2 is measured in the unannealed As_2S_3 films. At high input power ($\sim$ 10 mW coupled power in the bus waveguide), the thermo-optic effect and the cavity-enhanced photosensitivity lead to resonant peak shape distortion and cavity instability.

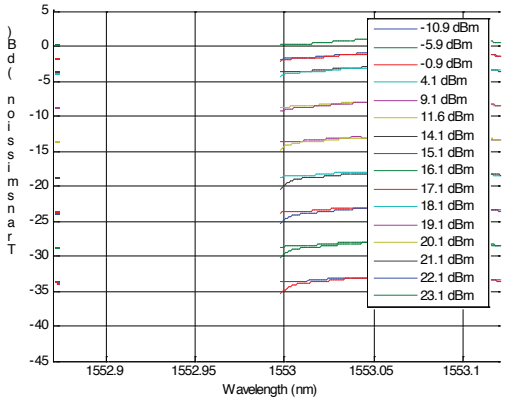


FIGURE 1: (a) Transmission spectra of a micro-disk resonator near a resonant peak measured at different input power levels; the arrows indicate the temporal sequence of measurements. [3]

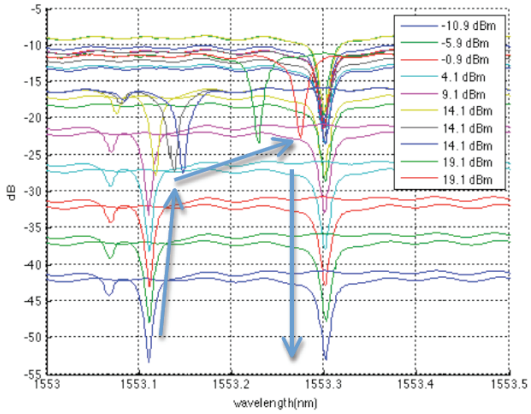


FIGURE 2: Transmission spectra recorded in the pump-probe measurements showing significant resonant peak shift when the pump beam is tuned to the resonant wavelength, indicating refractive index trimming due to 1550-nm infrared light illumination; the arrows indicate the temporal sequence of measurements.

REFERENCES

[1] J. Hu, V. Tarasov, N. Carlie, N. Feng, L. Petit, A. Agarwal, K. Richardson, and L. C. Kimerling, "Si-CMOS-compatible lift-off fabrication of low-loss planar chalcogenide waveguides," *Opt. Express* vol. 15, pp. 11798-11807, 2007.

[2] J. Hu, N. Carlie, N. Feng, L. Petit, A. Agarwal, K. Richardson, and L. C. Kimerling, "Planar waveguide-coupled, high-index-contrast, high-Q resonators in chalcogenide glass for sensing," *Opt. Lett.* vol. 33, pp. 2500-2502, 2008.

[3] J. Hu, M. Torregiani, F. Morichetti, N. Carlie, L. Petit, A. Agarwal, A. Melloni, K. Richardson, and L.C. Kimerling, "Cavity-enhanced photosensitivity in chalcogenide glass," *OSA Integrated Photonics and Nanophotonics Research and Applications Topical Meeting,* 2009.

Polycrystalline Germanium for Use in CMOS-compatible Photodetectors

K. McComber, J. Liu, J. Michel, L. C. Kimerling
Sponsorship: NSF

The fabrication of germanium photodetectors at microprocessor interconnect levels could enable dense CMOS electronic-photonic integration, in which electronic components exist at the substrate level and photonic devices exist at higher levels. This degree of integration would help continue Moore's Law even further into the future. However, such a task faces daunting complexities. For one, the lack of a single-crystal Si substrate removes the possibility of traditional Ge-on-Si epitaxial growth. Additionally, as fabrication moves to higher chip levels, the thermal budget decreases, and devices at these higher levels must be processed at temperatures lower than those of substrate-level device processing. This constrains, for example, the amount of electronic defect annealing that may be performed on such devices.

This work investigates the fabrication of interconnect-level CMOS-compatible polycrystalline Ge (poly-Ge) photodetectors by ultra-high vacuum chemical vapor deposition (UHVCVD), with the goal of fabricating functioning devices using processing steps that do not exceed 450° C. Previous researchers have grown poly-Ge photodetectors at such temperatures [1], but these devices showed poor responsivities compared with epitaxial devices and were not suitable for production-grade microprocessors. To improve the poly-Ge performance, a major concentration of this work is on the control of both the grain sizes and textures of the poly-Ge, as large-grained devices with consistent textures should yield the least grain boundary (bulk) leakage current and the most reproducible characteristics.

We have successfully grown poly-Ge selectively on Si in submicron features using UHVCVD at temperatures less than 450° C. Figure 1 shows the process steps and temperatures used for each step. Figure 2 shows a cross-sectional image of a trench filled with poly-Ge on a-Si. The poly-Ge exhibits near-planar surface morphology (roughness ~20 nm) and completely fills the Si features, a feat that has eluded researchers of epitaxially-grown Ge. Current work focuses on methods to increase the grain sizes and control the properties of the grain boundaries.

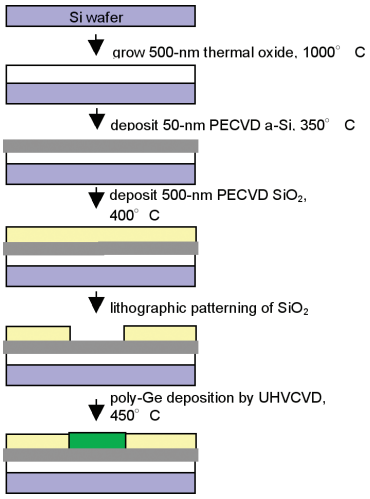


FIGURE 1: The selective poly-Ge deposition process (not to scale). The initial thermal oxide growth is merely to provide an amorphous substrate for the a-Si and is thus not considered part of the novel process.

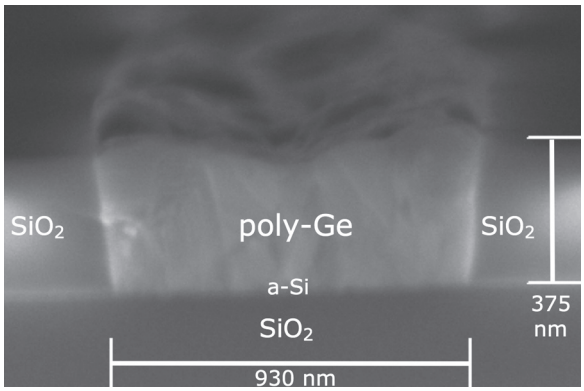


FIGURE 2: Cross-sectional SEM image of poly-Ge selectively grown on a-Si in an oxide trench.

REFERENCES

[1] L. Colace, V. Sorianello, M. Balbi, and G. Assanto, "Germanium near infrared detector in silicon on insulator," *Applied Physics Letters*, vol. 91, pp. 021107-1-021107-3, July 2007.

Room-temperature Direct-band-gap Electroluminescence from Ge-on-Si Light-emitting Diodes

X. Sun, J. Liu, L. C. Kimerling, J. Michel
Sponsorship: AFOSR MURI

Recently, there has been a surge in research on Si-based light-emitters for Si optoelectronic applications owing to the potential for monolithically integrating optical components with electronic devices on Si. Electronic-photonic integration on Si meets the needs for high-bandwidth and low-power-density on-chip interconnects. Germanium as the active material is a promising candidate for monolithically integrated Si-based light emitters because of its high compatibility with silicon-complementary metal oxide semiconductor (CMOS) processes and its 1550-nm (0.8 eV) light emission from direct band-to-band transition. To increase the injected electron population in the Γ valley so as to increase the overall light-emission efficiency, in-plane tensile stress is introduced into epitaxial (100) Ge thin films on Si.

The thermally induced tensile strain shrinks the direct band gap relative to the indirect band gap, resulting in more injected electrons in the direct Γ valley following Fermi statistics. To verify this idea, we have fabricated tensile strained Ge/Si p-i-n diodes to investigate the direct gap electroluminescence (EL) of Ge. The cross-section of the p-i-n heterojunction diode is schematically shown in Figure 1(a). A hot-wall ultra-high vacuum chemical vapor deposition (UHVCVD) reactor was used to selectively grow epitaxial Ge. The I-V characteristic shown in Figure 1(c) is measured from a 20-μm-by-100-μm rectangle-shaped diode and exhibits a good rectifying behavior. We observed the onset of EL from the 20-μm-by -00-μm diode at a forward bias of 0.5 V, corresponding to an injection current of 1.3 mA. Figure 2(a) shows the EL spectrum at room temperature from the diode at 50 mA forward electrical current.

The spectrum is consistent with the room-temperature PL measured from a 0.2% tensile-strained epitaxial Ge film. The multiple sharp peaks in the EL spectrum are reproducible and not due to noise. The linear relationship between the energy positions of these peaks and the peak number shown in the Figure 2(a) inset indicates the occurrence of Fabry-Perot resonances corresponding to an air gap of ~120 μm between the end of the optical fiber and the device surface.

REFERENCES

[1] J. Liu, X. Sun, D. Pan, X. Wang, L. C. Kimerling, T. L. Koch and J. Michel, "Tensile-strained, n-type Ge as a gain medium for monolithic laser integration on Si," *Opt. Express*, vol. 15, no. 18, pp.11272-11277, 2007.

[2] X. Sun, J. Liu, L. C. Kimerling, and J. Michel, "Room Temperature Direct Band Gap Electroluminescence from Ge-on-Si Light Emitting Diodes," *Opt. Lett.*, vol. 34, no. 18, pp. 1198-1200, 2009

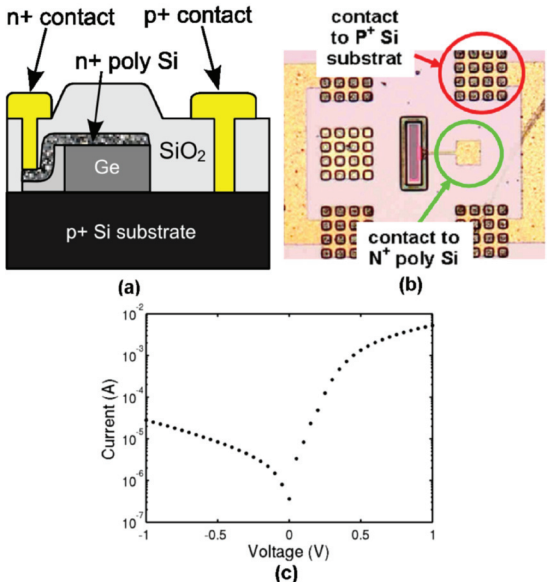


FIGURE 1: (a) Schematic cross-section of a tensile-strained Ge/Si heterojection p-i-n light emitting diode. (b) The microscopic image of the top view of a 20-µm-by-100-µm Ge/Si p-i-n diode. (c) The I-V characteristics of the Ge diode [2].

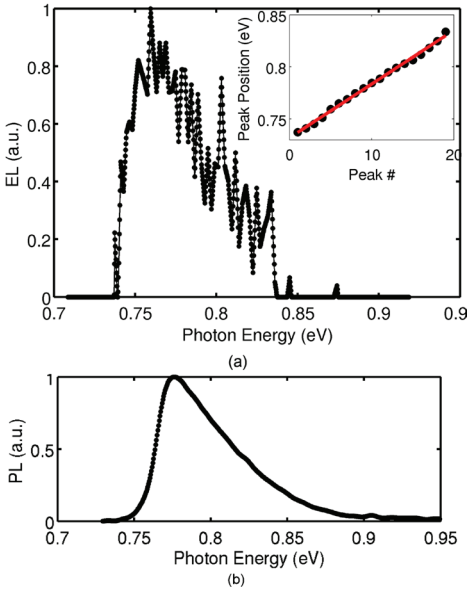


FIGURE 2: (a) Direct gap EL spectrum of a 20-µm-by-100-µm 0.2% tensile-strained Ge/Si p-i-n light-emitting diode measured at room temperature. The multiple sharp peaks in the spectrum are highly periodic as a result of Fabry-Perot resonances as shown in the inset. (b) Room temperature direct gap PL of a 0.2% tensile-strained Ge film epitaxially grown on silicon [2].

Mid-IR Light Sources

P. Chu, H. AlBrithen, A. AlSahli, G. S. Petrich, R. J. Ram, L. A. Kolodziejski
Sponsorship: King Abdul Aziz City for Science and Technology

Numerous medical and military applications require high-performance mid-IR semiconductor laser sources. Quantum cascade lasers, which do not utilize material properties but rather utilize intraband energy level engineering, are used as sources in the mid-IR spectrum (l=4~9μm). In the shorter mid-IR spectrum (l=2~4μm), optical sources use interband transitions. In this region of the spectrum, the energy-gap separation and band alignment determine the emission wavelength of laser diodes.

GaSb-based, type I lasers have been successfully used at wavelengths up to 2.6μm with high power, high characteristic temperature, and low threshold current density. The rest of the shorter mid-IR spectra rely on lasers employing a type II "W" active region, which limits the laser's performance due to the lack of spatial overlap of the carrier wave functions in the conduction and valence bands. The use of a small amount of incorporated nitrogen within the active region of GaSb-based, type I lasers has the potential to increase the emission wavelength to over 2.6 μm while preserving the use of interband transitions. Shallow nitrogen defect states interact with the conduction band edge and causes splitting of the energy levels, which narrows the band gap to allow the emission spectrum to shift to longer wavelengths.

Currently we have designed a nitrogen-free GaSb-based laser structure, which emits at 2.6 μm (Figure 1). Various nitrogen-free test structures have been grown by MBE. Future work will focus on the growth of III-(SbN) epitaxial thin films followed by material and optical characterization. High resolution x-ray diffraction, Auger electron spectroscopy, and photoluminescence will be used to characterize the epilayers. The long-term goal is to fabricate a mid-IR diode laser that emits between 2.6 μm and 3 μm.

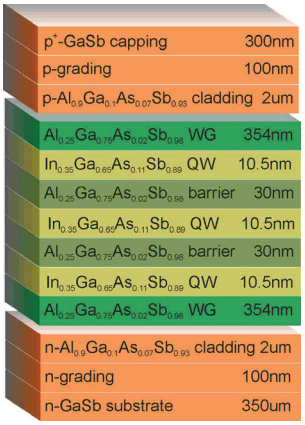


FIGURE 1: Nitrogen-free triple-quantum-well laser design that is designed to emit at 2.3 µm.

Modulators for Arbitrary Optical Waveform Generation

O. Shamir, G. S. Petrich, F. X. Kaertner, E. P. Ippen, L. A. Kolodziejski
Sponsorship: DARPA

Optical signal modulation is a cornerstone of communication systems, allowing the transfer of information by electrically encoding the data onto an optical carrier. By transforming an incoming pulsed optical source into an optical frequency comb using arrayed waveguide gratings and employing both phase and amplitude modulation using Mach Zehnder interferometers, an arbitrary optical waveform is constructed following the recombination of the frequency comb.

Electro-optic modulation of frequency combs that are centered at a wavelength of 800nm requires the use of GaAs-based materials that are transparent to light of that wavelength. A structure (shown schematically in Figure 1) is composed of alternating high- and low-index AlGaAs materials, low-index AlGaAs cladding layers, and oxidizable AlAs layers. The structure has been grown by molecular beam epitaxy and has been processed into Mach Zehnder interferometers that consist of 2-μm-wide waveguides and active modulators. To create the largest mode possible and to minimize the coupling loss, the index contrast between the waveguiding layers and the cladding layers is minimized through the use of a dilute waveguide structure in which thin layers of high-index material are embedded in a low-index material. The resulting layered structure has an effective index slightly higher than the low-index material and is determined by the layer thicknesses as well as the refractive index of the two materials that comprise the dilute waveguide. The oxidized AlAs layers strongly confine the optical mode to the middle of the structure and are expected to allow the device to withstand higher operating voltages without concern about breakdown or carrier loss.

Fabrication of the electro-optic modulator employs self-aligned photolithography and etching processes to ensure successful optical transfer between the passive and active waveguide regions, which are defined in separate steps. The work includes an exploration of the use of bicyclobutane as a planarizing agent and etching techniques on a SAMCO ICP-RIE system. Optical testing of some of the initial modulators are underway.

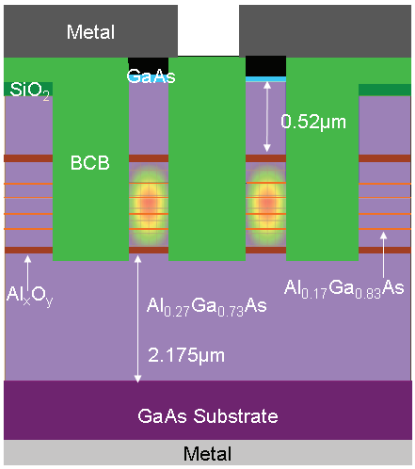


FIGURE 1: Cross-section illustration of a complete waveguide modulator structure.

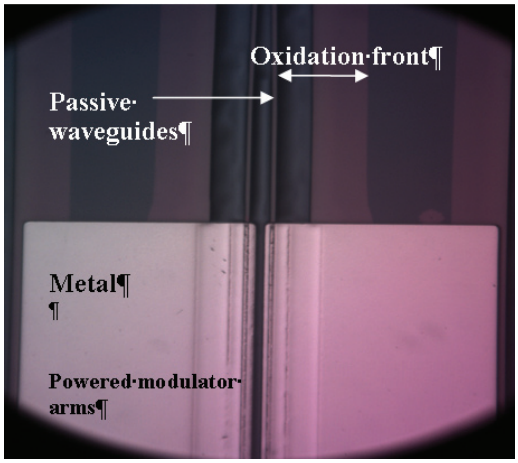


FIGURE 2: Top view of modulator device, including active (metallized) and passive waveguides. The oxidation front of the AlAs is also visible.

Nanoelectromechanically Actuated Optical Switches

R. E. Bryant, G. S. Petrich, L. A. Kolodziejski
Sponsorship: NSF MRSEC

As an alternative to free-space MEM optical switches, a set of planar MEM optical switches were designed to reconfigure light paths on the micro- to submicro-second timescales within a smaller device footprint and at a lower anticipated manufacturing (packaging) cost. Moreover, these optical switches were specifically designed to be compatible with a variety of microphotonic substrate platforms, enabling them to be monolithically integrated alongside a diverse suite of optical devices.

Two well-established technologies were used in the design of these substrate platform-independent optical switches: high-index contrast planar optics and microelectromechanical (MEM) actuation. All of the MEM optical switches were based on evanescent-coupled structures that were modulated mechanically. A flexible fabrication process sequence was devised in order for the MEM optical switches to be digitally actuated without requiring complex and expensive feedback circuitry. Moreover, the MEM optical switches were designed with mechanical latches that effectively made the MEM optical switches bistable--not requiring a constant external power supply to maintain a switch state. Figure 1 shows an optical switch that uses adiabatic directional coupling to transfer the optical signal from one waveguide to the other, tethers along with gap closers to push the waveguides together to allow the waveguides to interact, and latches along with gap closers to hold the optical switch in the desired optical state.

Unlike free-space MEM optical switches, each of the MEM optical switches is able to perform polarization-independent broadband switching, coarse-wavelength-division multiplexing, polarization-splitting, or a combination thereof.

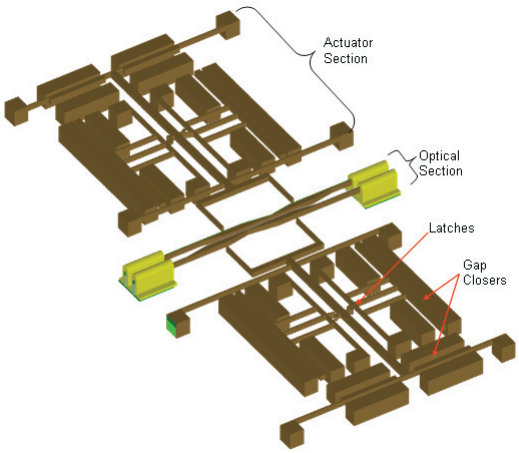


FIGURE 1: Schematic of the optical switch.

Novel Active Materials for Optical Sources

S. Nabanja, G. S. Petrich, L. A. Kolodziejski
Sponsorship: NSF

Quantum-dot (QD) heterostructure lasers are a type of semiconductor laser that utilize quantum dots as their active medium within the light-emitting region. Quantum dots are semiconductor nanocrystals of narrow band-gap material that are embedded in a wider band-gap material. The use of molecular beam epitaxy for the growth of highly lattice-mismatched III-V semiconductor materials has made the self-assembly of these structures possible. Due to the strong three-dimensional carrier confinement, devices that employ quantum dots have unique capabilities that are otherwise practically unachievable with bulk semi-conductors or even two-dimensional-confined quantum wells.

One of the significant benefits of exploiting quantum effects in QD semiconductor lasers is the decrease of the laser's threshold current density, which is a direct result of the reduction in the translational degrees of freedom of charge-carriers (electrons and holes). This reduction in translational degrees of freedom leads to an increase in the density of states of charge-carriers near the band edges. Another important benefit is that the threshold current density in QD lasers is unaffected by temperatures up to about 300K since the charge-carriers can only be thermally excited to a very limited number of the well-spaced energy levels.

The goal of this work is to design, fabricate, and characterize semiconductor lasers with quantum dots within their active region on both n-GaAs substrates and n-InP substrates. The use of a separate confinement heterostructure will allow for electrical and vertical optical confinement while horizontal optical confinement will be achieved by means of ridge waveguides. The front-end fabrication processes include photolithography to define the etch masks, a reactive ion and a wet etch of the arsenide-based or phosphide-based material to create the waveguide ridges, a planarization step, and then finally ohmic contact patterning. The back-end processes include lapping, metal evaporation, and cleaving. Characterization of GaAs-based quantum dot layers is underway while the etching of the phosphide layers within the InP-based quantum dot lasers is being optimized on the SAMCO inductively-coupled-plasma reactive ion etcher.

Photonic Crystal Applications

M. Araghchini, T. Shih, A. Kurs, M. Dahlem, I. Čelanović, J. Kassakian, K. Hall, M. Kesler, G. S. Petrich, M. Soljacic, J. D. Joannopoulos, E. P. Ippen, L. A. Kolodziejski
Sponsorship: NSF MRSEC, SRC/FCRP IFC, STTR

Photonic crystals (PhCs) are engineered structures that modify the propagation of light through the material. Two-dimensional photonic crystals are used in super collimators and in thermo-photo-voltaic systems.

Super-collimation (SC) is the propagation of light without diffraction using the properties of the photonic crystal. As opposed to reducing the distribution of the beam's constituent eigenmodes to be sufficiently narrow in k-space (or equivalently approaching a infinitely wide plane wave) to achieve nearly divergent-less propagation, a super-collimator allows for nearly divergent-less propagation for beam widths only a few times the lattice constant of the PhC. Successful fabrication and measurement of SC have been achieved for planar PhCs that are composed of silicon rods surrounded by air and for PhCs that are composed of air holes that are etched into silicon. The super-collimating PhC is fabricated on a silicon-on-insulator (SOI) wafer (Figure 1). The low-index SiO_2 layer is used to minimize radiation loss into the high-index silicon substrate. The rods are defined using interference lithography and pattern transfer is achieved with reactive ion etching. Figure 2 shows a plan view IR image of a rod-based photonic crystal super-collimator as a function of wavelength. Super collimation is observed at a wavelength of 1550nm.

Thermo-photo-voltaic (TPV) systems convert heat into electricity. A basic thermo-photo-voltaic system consists of a thermal emitter and a photovoltaic (PV) diode. These systems have been of scientific interest for over 50 years; however, most interesting TPV developments have occurred in the last 15 years, with the development of the semiconductor industry. The TPV conversion systems have the advantages of no moving parts, long lifetime, quiet operation, low exhaust emissions, and low maintenance. However, their low efficiency has been their main disadvantage. In order to achieve higher TPV efficiencies, it is necessary to better match the emitted spectrum to the sensitivity spectrum of the PV diode. In this work, spectral control is done via selective emission by using periodic structures, i.e., a PhC. In this project, the design, fabrication, and demonstration of optimized efficient TPV systems using tungsten-based photonic crystals for spectrum modification are being investigated [1].

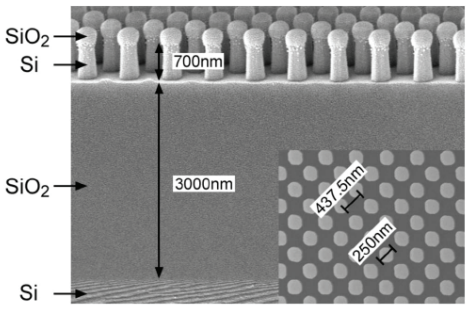


FIGURE 1: Scanning electron microscope image of the super-collimator. The silicon posts are 700nm tall and rest on 3-µm-thick layer of silicon dioxide on a silicon wafer.

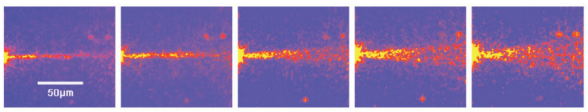


FIGURE 2: An IR image of the super collimation effect within the photonic crystal. The measurement wavelengths are (left to right): 1530nm, 1550nm, 1570nm, 1590nm, and 1610nm.

REFERENCES

[1] N. Jovanovic, "Microstructured Tungsten Thermophotovoltaic Selective Emitters," PhD thesis, Massachusetts Institute of Technology, Cambridge, 2008.

Photonic Integrated Circuits for Ultrafast Optical Logic

T.-M. Shih, J. Wang, G. S. Petrich, E. P. Ippen, L. A. Kolodziejski
Sponsorship: DARPA

Today, long-distance internet traffic is transmitted optically — "3R"-regenerated (reamplified, reshaped, retimed) — and routed by optical repeaters. However, the transmitted information is processed in the electronics domain; hence expensive optical-to-electronic-to-optical (OEO) conversions are required. This OEO bottleneck can be alleviated by all-optical processing, which has the potential to increase data bit rates to over 100Gb/s [1]. Nonlinear semiconductor optical amplifiers (SOAs) are good candidates for all-optical logic. Among other functions, add-drop-multiplexing, "3R"-regeneration, wavelength conversion, and packet header processing have been demonstrated with SOA-based interferometers [2], [3].

Two generations of integrated all-optical logic chips operating at a wavelength of 1550nm [4-6] have been modeled, designed, fabricated, and tested. Indium phosphide-based SOAs are vertically integrated with passive waveguides using the asymmetric twin waveguide technique [7]. The SOAs are placed in a Mach-Zehnder interferometer configuration as depicted in Figure 1. A passive waveguide loss of 0.89 cm^{-1} has been measured, and MMI operation has been verified using an IR camera. The diode characteristics of the SOAs indicate a contact resistance on the order of 10^{-4} Ω cm^2 needs to be improved upon. Optical gain as high as 27dB has been measured. Future work also includes utilizing quantum well and quantum dot active materials to increase optical data bit rates.

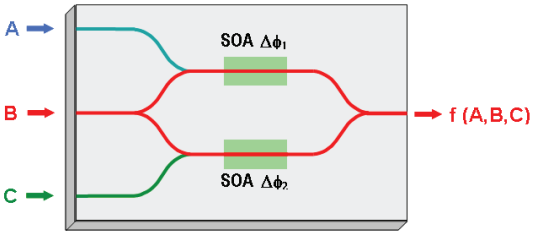


FIGURE 1: General schematic of an all-optical logic gate. Control signals A and C set the relative phase shifts of the two arms of the Mach-Zehnder interferometer, which signal B experiences. The output is filtered to obtain the desired wavelength (generally that of B).

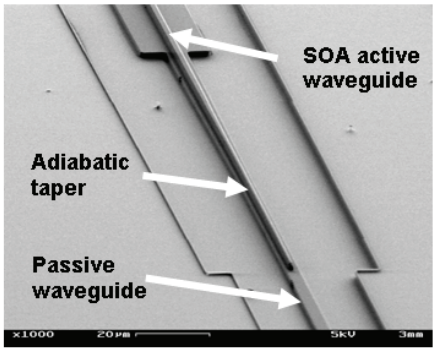


FIGURE 2: Scanning electron microscope image of the asymmetric twin waveguide taper for coupling between the active SOA waveguide and the passive waveguide lying below (courtesy R.D. Williams [5]).

REFERENCES

[1] K.L Hall and K.A. Rauschenbach, "100-Gbit/s bitwise logic," *Optics Letters*, 23(16):1271-1273, 1998.

[2] K.E. Stubkjaer, "Semiconductor optical amplifier-based all-optical gates for high-speed optical processing," *IEEE Journal of Selected Topics in Quantum Electronics*, 6(6):1428-1435, 2000.

[3] J.P. Wang, B.S. Robinson, S.A. Hamilton, and E.P. Ippen, "Demonstration of 40-Gb/s Packet Routing Using All-Optical Header Processing," *IEEE Photonics Technology Letters*, 18(21):2275-2277, 2006.

[4] A. Markina, "Design and Simulation for the Fabrication of Integrated Semiconductor Optical Logic Gates," PhD thesis, Massachusetts Institute of Technology, Cambridge, 2005.

[5] R.D. Williams, "Photonic Integrated Circuits for Optical Logic Applications," PhD thesis, Massachusetts Institute of Technology, Cambridge, 2007.

[6] J. Wang, "Demonstrating Effective All-Optical Processing in Ultrafast Data Networks Using Semiconductor Optical Amplifiers," PhD thesis, Massachusetts Institute of Technology, Cambridge, 2008.

[7] V.M. Menon, F. Xia, and S.R. Forrest, "Photonic integration using asymmetric twin-waveguide (ATG) technology: part II-devices," *IEEE Journal of Selected Topics in Quantum Electronics*, 11(1):30-42, 2005.

Tunable Diode-laser Photoacoustic Spectroscopy

H. Lee, A. Masurkar, A. Hamidalddin, R. J. Ram
Sponsorship: KACST

.Photoacoustic spectroscopy [1] is an optical absorption spectroscopy whereby the absorbed optical power is detected indirectly by sensing the thermal excitation and expansion of the sample using microphones or other mechanical displacement sensors. For trace-gas-sensing, specificity is achieved by tuning the optical excitation source to the narrow band absorption lines of the gas of interest. The accessibility of photoacoustic spectroscopy has improved due to the availability of inexpensive tunable diode-laser sources developed for telecommunications applications and continued innovation in semiconductor active materials [2], [3] is opening new spectral windows for detecting a wider variety of gasses. Photoacoustic detection of optical absorption has favorable scaling properties for miniaturization [4] and miniature photoacoustic cells have been investigated [5] along with compact resonant quartz tuning fork detectors [6]. We are working to develop a compact and robust photoacoustic spectroscopy system with the aim of performing gas analysis in harsh environments. Initial experiments have focused on evaluating photoacoustic sensor architectures and laser diode characterization.

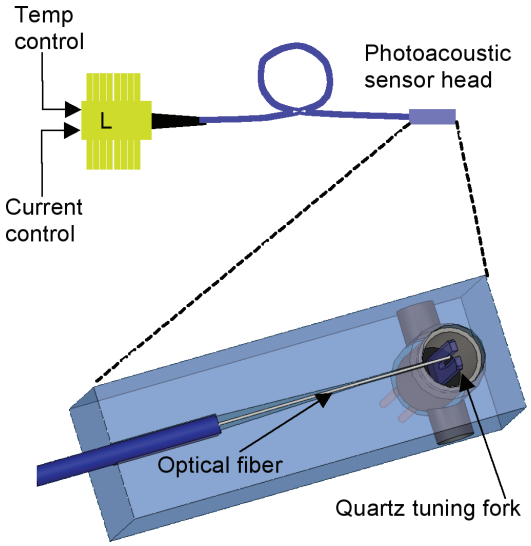


FIGURE 1: Schematic representation of a photoacoustic sensor using a quartz tuning fork. Wavelength modulation of the laser diode at 1/2 the resonant frequency of the tuning fork results in optical absorption and thermal excitation at the tuning fork's resonant frequency.

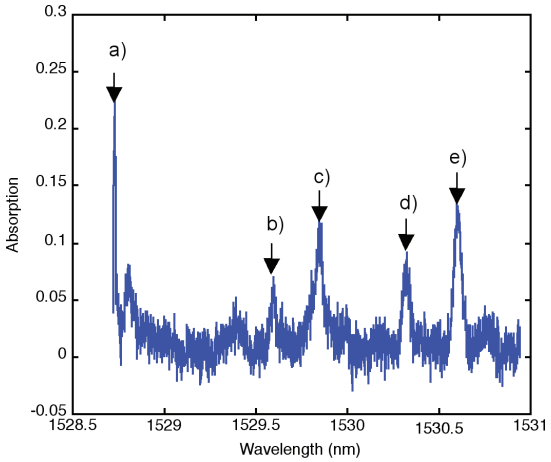


FIGURE 2: Optically measured absorption spectrum of ammonia gas (100Torr, 10-cm path length). Absorption peaks correspond to known lines at a) 1528.727 nm, b) 1529.596 nm, c) 1529.850 nm, d) 1530.328 nm, and e) 1530.601 nm.

REFERENCES

[1] G.A. West, J.J. Barrett, D.R. Siebert, and K.V. Reddy, "Photoacoustic spectroscopy," *Review of Scientific Instruments* vol. 54, no. 7, pp 797-817, 1983.

[2] S. Schilt, A. Vicet, R. Werner, M. Mattiello, L. Thevenaz, A. Salhi, Y. Rouillard, and J. Koeth, "Application of antimonide diode lasers in photoacoustic spectroscopy," *Spectrochimica Acta Part A*, vol. 60, pp 3431-3436, 2004.

[3] B.A. Paldus, T.G. Spence, R.N. Zare, J. oomens, F.J.M. Harren, D.H. Parker, C. Gmachl, F. Cappasso, D.L. Sivco, J.N. Baillargeon, A.L. Hutchinson, and A.Y. Chao, "Photoacoustic spectroscopy using quantum-cascade lasers," *Optics Letters*, vol. 24, no. 3, pp. 178-180, Feb. 1999.

[4] S.L. Firebaugh, K.F. Jensen, and M.A. Schmidt, "Miniaturization and integration of photoacoustic detection," *Journal of Applied Physics*, vol. 92, no. 3, pp. 1555-1563, Aug. 2002.

[5] P.M. Pellegrino and R.G. Polcawich, "Advancement of a MEMS photoacoustic chemical sensor," in *Proceedings of the SPIE*, vol. 5085, 2003, pp. 52-63.

[6] S.G. So, O. Al Rifai, G. Wysocki, A.A. Kosterev, F.K. Tittel, "Advanced embedded control and data acquisition systems for laser-based quartz-enhanced photoacoustic spectroscopy," in *Proceedings of IEEE Sensors 2007*, pp. 1279-1282.

Deep Submicron CMOS Photonics

J. S. Orcutt, A. Khilo, M. A. Popović, C. W. Holzwarth, E. Zgraggen, B. Moss, H. Li, M. S. Dahlem, H. I. Smith, F. X. Kärtner, E. P. Ippen, J. L. Hoyt, V. Stojanović, R. J. Ram
Sponsorship: DARPA

In the past decade, silicon has moved from a workbench for low-index contrast photonics to a strong-confinement (SC) photonics workhorse. The SC silicon-core waveguides have been shown to maintain low-loss while enabling micron-scale photonic structures [1] and suitability for next-generation telecom components [2]. The possibility of inter- and intrachip photonic interconnect integrated with traditional CMOS electronics has opened silicon-core SC photonics to the VLSI community. Photonic components required for integration include SC waveguides, resonant add-drop filters for wavelength-division multiplexing (WDM), energy-efficient modulators, and integrated photodiodes.

Traditional silicon-on-insulator (SOI) waveguides that use the active electronic silicon layer of SOI wafers as the waveguide core require a thick buried-oxide layer (2 to 3 μm) to enable low optical-substrate leakage loss. The photonic chip presented here, shown in Figure 1, is produced within an existing commercial bulk CMOS flow, adding zero in-house production changes. In bulk CMOS processes, unlike SOI CMOS, there is no single-crystal silicon layer. There is, however, a polysilicon layer in the process front end that is used to form the transistor gates over a thin oxide as well as local interconnects and resistors over a thicker oxide, referred to as shallow trench isolation (STI). This poly-Si layer must first be deposited undoped since opposite polarity implant steps are used to form the n-channel and p-channel transistor gates. Additionally, the need to create accurate resistors requires a way to block the standard silicidation step of the polysilicon. These two facts allow for the processing masks to be designed to create an undoped, unsilicided polysilicon layer for SC waveguide fabrication.

Using this platform, we designed the first bulk photonic chip in a commercial process on a 4-mm2 die. Primary goals for this chip are to demonstrate integrability, characterize waveguide loss, and evaluate photonic device performance. Preliminary device demonstrations include ring resonator filter banks, shown in Figure 2.

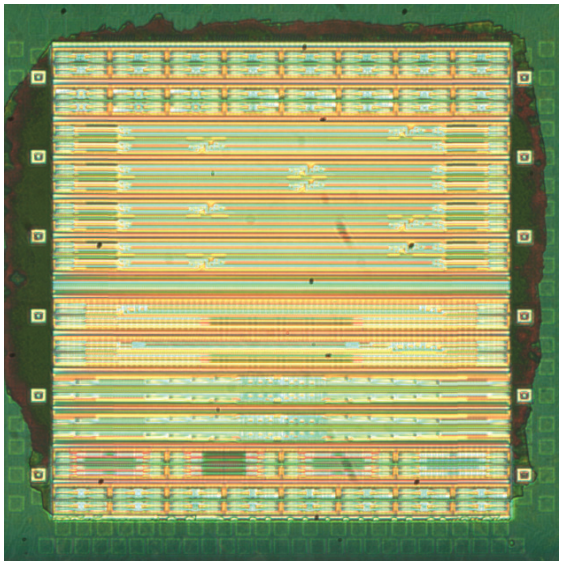


FIGURE 1: Bulk 65-nm photonic test chip die photo. A 2x2 mm^2 die contains 116 devices and over 21 cm of waveguide.

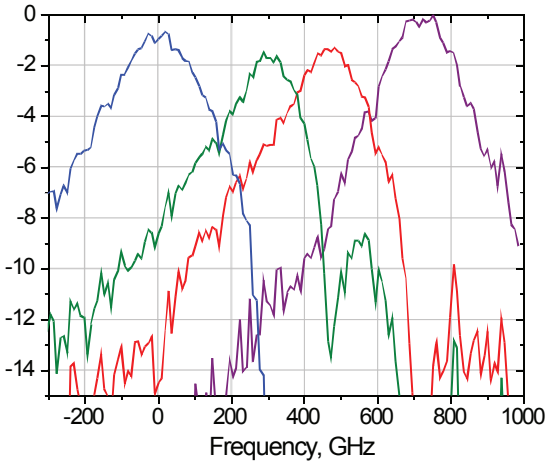


FIGURE 2: Measured drop-port transmission functions for a 4-channel ring resonator add-drop filter bank with 240 GHz channel spacing. Low process variation is observed in the center frequency and peak transmission uniformity.

REFERENCES

[1] F. Xia, et al., "Ultracompact optical buffers of a silicon chip," in Nat. Phot. 1, pp. 65-71, (2007).

[2] M.A. Popović, T. Barwicz, et al., "Strong-confinement microring resonator photonic circuits," in Proc. 20th An. Meet. IEEE Lasers and Electro-Optics Soc. (LEOS), Lake Buena Vista, Florida, Oct 2007, paper TuCC3.

Ensuring Precision of Overlay in Photonic-crystal Lithography

C. P. Fucetola, A. A. Patel, E. E. Moon, H. I. Smith
Sponsorship: AFOSR

This project aims to develop a new approach to constructing 3-dimensional systems. In brief, the 3-D structure is formed by the stacking of membranes. This stacking approach enables one to pattern the membranes prior to assembly, thereby achieving a highly complex 3-D system using only well-developed 2-D patterning technology. Our initial objective is the fabrication of 3-D photonic crystals, in Si and SiNx, with devices located in the photonic-crystal interior. The 3-D photonic crystal consists primarily of periodic structures. The particular 3-D photonic crystal of interest, a passive reflector, can be made from stacked membranes, each consisting of a 4-fold symmetric array of holes and a 4-fold array of posts, shifted slightly from the holes, as depicted in Fig. 1. The placement of the array of posts with respect to the holes is such that any post falls between only two holes. Then, upon stacking the membranes, the final periodicity in the third dimension is formed between the overlaid post-hole-post-hole positions.

Interference Lithography (IL) can make a 4-fold symmetric pattern but conventional IL cannot easily overlay two 4-fold symmetric patterns. Generating the second 4-fold pattern of posts and overlaying it onto the patterned (pre-released) membrane is necessary to create the structure shown in Figure 1. However, generation of a second periodic pattern using conventional IL tools is problematic because of variations in the pitch, duty-cycle and symmetry. These considerations require another approach; we call it Coherent-diffraction Lithography (CDL) [2]. Figure 2 shows the Coherent-diffraction Lithography tool and schematic. CDL incorporates Interferometric Spatial-phase Imaging (ISPI) for multilayer alignment and uses the Talbot effect to replicate the periodic pattern on a mask. ISPI [1] allows precise 6-axis closed-loop positioning between the mask and substrate by imaging back-diffracted and reflected light to determine the relative position between the mask and substrate. Combined, the Talbot effect and ISPI is ideal for photonic-crystal lithography.

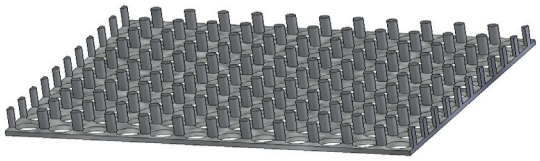
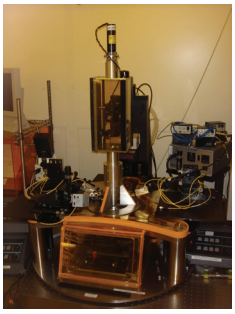
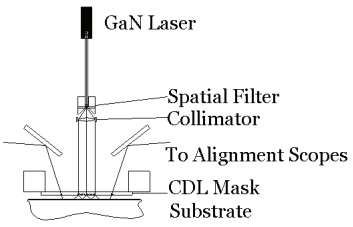


FIGURE 1: Two-dimensional square geometry photonic crystal membrane design consisting of two feature layers. The bottom layer is a layer of holes 145nm thick and the top layer of posts is 585nm thick. The periodicity in the x and y directions is 660nm for both layers. Any given post is between two holes. This structure is designed to reflect in-plane 1.55μm light regardless of polarization.





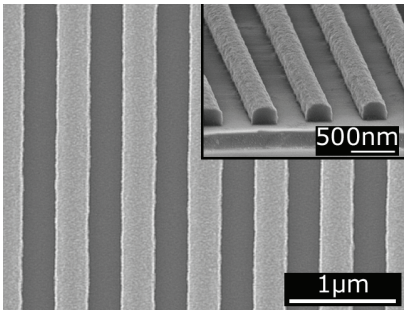


FIGURE 2: ISPI & CDL: Apparatus, System Schematic and printed grating. Light from the GaN laser is spatially filtered prior to irradiating the CDL Mask. Combined with the ISPI alignment scheme, the filtered light passes through the mask and interferes on the substrate to produce a grating pattern.

REFERENCES

[1] E. E. Moon, L. Chen, P. N. Everett, M. K. Mondol, and H. I. Smith, "Interferometric-spatial-phase imaging for six-axis mask control", *J. Vac. Sci. Technol. B*, vol. 21, no. 6, pp. 3112-3115, Dec. 2003.

[2] C. Zanke, M. Qi, and H. I. Smith, "Large-area patterning for photonic crystals via coherent diffraction lithography", *J. Vac. Sci. Technol. B*, vol. 22, no. 6, pp. 3352-3355, Nov. 2004.

Nanofabrication of Optical-microring Filter Banks for Integrated Photonic Systems

C. W. Holzwarth, T. Barwicz, M. A. Popović, A. Khilo, M. Dahlem, E. P. Ippen, F. X. Kärtner, H. I. Smith
Sponsorship: DARPA

Achieving accurate resonant-frequency spacing of microring-filters is critical for integrated-photonic systems. In the NanoStructures Laboratory we have developed a technique using scanning-electron-beam lithography (SEBL) that is capable of accurately controlling the resonant frequency spacing in microring-resonator filter banks. The resonant wavelength of a microring-resonator filter is dependant on the ring radius and effective index of refraction of the ring waveguide. The effective index is controlled lithographically by controlling the width of the ring waveguide. Although it is simple to change the width and the radius of the ring in the SEBL layout, this is limited to discrete jumps corresponding to the step size of the SEBL address grid. To achieve 1 GHz control of the resonant frequency the SEBL systems needs a step size of <30 pm. In our process this limitation of discrete step size is overcome by modulating the electron-beam dose to precisely control the average ring waveguide width [1]. However, stochastic variations during processing typically limit dimensional precision, resulting in small frequency errors (~20 GHz), resulting in the need for postfabrication trimming. Methods for dynamic and static trimming are being developed.

In our experiment second-order microring-resonator filters, fabricated in silicon-rich silicon nitride and overclad with HSQ, were used in microring filter banks (Fig. 1(a), (b)). Using dose modulation, twenty-channel dual-filter banks with a target channel spacing of 80 GHz were fabricated and tested, demonstrating control of changes in the average ring-waveguide width of 0.10 nm, despite the 6 nm SEBL step size (Fig. 1(c)). Variations between filter responses were due to slight frequency mismatches between rings of the same filter, we demonstrated that this can be corrected by trimming with integrated microheaters. Current efforts focus on improving filter bank performance, by using lower loss Si-core microrings and electron-beam curing the HSQ overcladding to statically trim frequency errors.

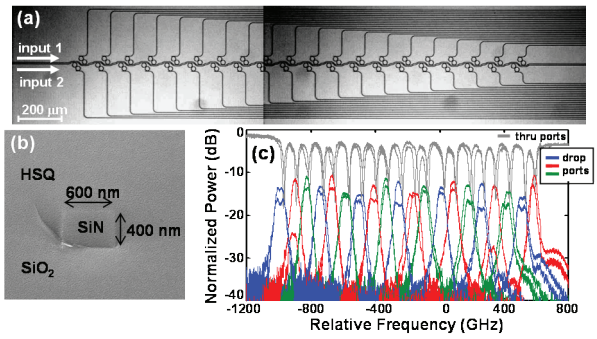


FIGURE 1: a) Scanning-electron micrograph of fabricated second-order twenty-channel dual-filter bank and b) cross-section of overclad waveguide. c) Filter response of second-order twenty-channel dual-filter bank with an average channel spacing of 83 GHz.

REFERENCES

[1] C. W. Holzwarth, T. Barwicz, M. A. Popović, P. T. Rakich, F. X. Kaertner, E. P. Ippen, and H. I. Smith, "Accurate resonant frequency spacing of microring filters without postfabrication trimming," *J. Vac. Sci. Technol. B*, vol. 24, no.6, pp. 3244-3247, Nov. 2006.

Localized-Substrate-Removal Technique Enabling Strong-confinement Microphotonics in Bulk-Silicon CMOS

C. W. Holzwarth, J. S. Orcutt, J. Sun, H. Li, M. A. Popović, V. Stojanović, J. L. Hoyt, R. J. Ram, H. I. Smith
Sponsorship: DARPA

Efforts elsewhere to integrate photonics with CMOS electronics require customization of the fabrication process to provide low-loss photonic components [1]. This compromises electronic performance, throughput, and cost. Customizations included thick low-index cladding layers, silicon-on-insulator material and electron-beam lithography. While tolerable for some applications, such customization is considered unacceptable for microprocessors and DRAM, circuits that would benefit the most from optical intrachip communication. To integrate photonics with circuits produced in high volume, one must be able to work within the constraints of commercial bulk CMOS process flows by utilizing industry-standard material layers, thicknesses, processing steps and tools. The CMOS process flow allows waveguides to be fabricated out of the polysilicon layer used for transistor gates and poly-resistors deposited above the shallow-trench isolation (STI) layer. However, such waveguides have a propagation loss of ~1000 dB/cm since the STI layer (<400 nm) is not thick enough to prevent the guided optical mode from "leaking" into the high-index Si substrate.

To overcome this problem, we have developed a post-processing technique using XeF_2 to locally remove the silicon underneath the STI layer (Fig. 1). The creation of air tunnels under the polysilicon waveguides eliminates propagation loss due to leakage into the substrate, with minimal impact on electrical, thermal, and mechanical performance of the electronics. XeF_2 gas is used because it etches Si isotropically, undercuts large areas without stiction problems, and has a high silicon-to-oxide etch-rate selectivity (>1000:1).

We have used this method to fabricate waveguides in polysilicon-on-oxide films, where the oxide undercladding was 50 nm (Fig. 2). Propagation loss was measured to be ~10 dB/cm at 1550 nm [2]. This process can be viable for CMOS chips, using CF_4 based reactive-ion etching to open vias through the backend dielectric, exposing the substrate. XeF_2 is then used to locally remove the substrate, undercutting proximate photonic structures.

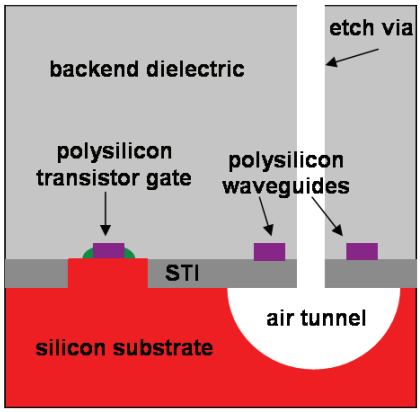


FIGURE 1: Sketch of the cross-section of a bulk CMOS chip showing how electronics and photonic devices can be fabricated on the same chip with only the addition of a post-processing step to locally remove the silicon substrate beneath the polysilicon waveguides.

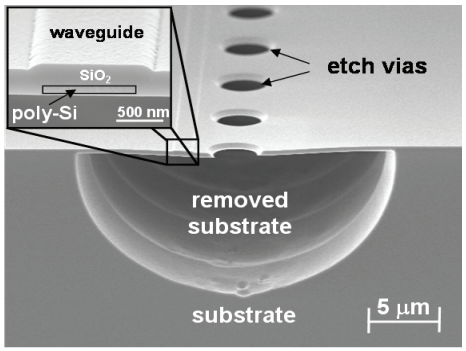


FIGURE 2: Scanning-electron micrograph of fabricated poly-silicon waveguide using the XeF_2 based substrate removal technique. The inset shows a close-up of the waveguide. The SiO_2 cladding beneath the poly-silicon is only 50 nm thick resulting in loss >1000 dB/cm before the localized substrate removal step. After removal, the loss is reduced to approximately 10 dB/cm.

REFERENCES

[1] J. S. Orcutt et al., "Demonstration of the first electronic photonic integrated circuit in a commercial scale bulk CMOS Process," Submitted to the Conference of Lasers and Electro-Optics (CLEO), San Jose, California, May 5-9, 2008.

[2] C. W. Holzwarth et al., "Localized Substrate Removal Technique Enabling Strong-Confinement Microphotonics in Bulk-Si CMOS Processes," Submitted to the Conference of Lasers and Electro-Optics (CLEO), San Jose, California, May 5-9, 2008.

Three-dimensional Photonic Crystals In Si_3N_4 and Si by Assembly of Prepatterned Membranes

A. A. Patel, C. Fucetola, E. E. Moon, H. I. Smith
Sponsorship: AFOSR

The diffraction of light within periodic structures (so called "photonic crystals") offers a wide variety of opportunities for controlling and manipulating light. Most research to date has focused on 2-dimensional (2D) photonic crystals, because highly developed planar-fabrication techniques are directly applicable. However, the full potential of photonic crystals in futuristic sensing, communication and computation systems is best achieved with 3-dimensional (3D) structures. The problem is that new methods of 3D fabrication need to be developed to achieve desired complex structures over large areas with low cost and high yield

Interference lithography can produce periodic 3D structures in photosensitive polymers, but the introduction of deviations from perfect periodicity (i.e., waveguides and structures that constitute "devices" within the periodic matrix, so-called "defects") is highly problematic. Moreover, it's not clear that backfilling 3D polymeric structures is applicable to a suitable range of materials. Layer-by-layer methods using scanning-electron-beam lithography enable the controlled introduction of defects, but to date fabrication is tedious, slow, low yield, and covers impractically small areas (e.g., <0.1mm on edge).

We describe a novel approach in which the 3D structure is fabricated by assembling membranes that are patterned in advance using conventional planar methods (Figure 1a). This approach minimizes the yield problem because membranes can be inspected and selected before assembly, and the desired waveguides and devices, can be introduced at any level. When brought into contact, membranes that are free of particles will directly bond at room temperature via van der Waals interatomic forces.

Figure 2 shows the concept of membrane stacking. We have developed a novel stacking apparatus in a cleanroom environment to study bonding mechanisms (Figure1b). This apparatus uses actuators to bring membranes together in a controlled and repeatable manner. A mix and match lithography process is used to pattern a large area photonic crystals alongside nonperiodic alignment marks. Surface flatness is characterized using interferometric techniques.

REFERENCES

[1] A. A. Patel and H. I. Smith, "Membrane stacking: a new approach to 3D nanostructure fabrication," *J. Vac. Sci. Technol. B*, vol. 25, no. 6, pp. 2662-2664, Nov. 2007.

[2] E. E. Moon, L. Chen, P. Everett, H. I. Smith, "Interferometric-spatial-phase imaging for Si x-axis control," *J. Vac. Sci. Technol. B*, vol. 21, no.6, pp. 3112-3115, Nov. 2003.

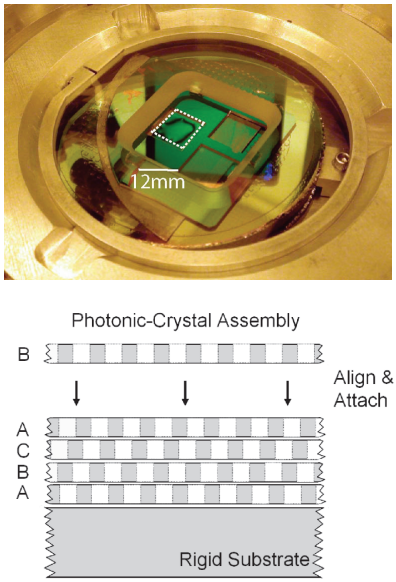


FIGURE 1: (a) Depiction of the layer-by-layer stacking approach. All the layers in the photonic crystal are fabricated in parallel reducing processing cycles, which will improve yield and reduce lead times. (b) Stacking apparatus with frame holding three membranes. Interference fringes between the left membrane and the mesa are observed.

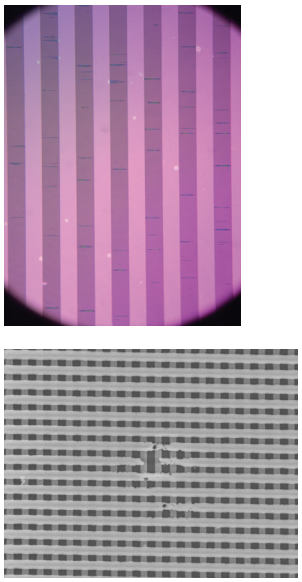


FIGURE 2: Stacking experiment in which free-standing gratings are stacked orthogonally to a raised substrate with gratings. The optical micrograph examines the quality of contact. Zooming on the square (40 micron per side) the freestanding grating has a pitch of 600nm.

Correction of Intrafield Distortion in Scanning-electron-beam Lithography and Confirmation via Optical Ring-resonator Filters

J. Sun, C. W. Holzwarth, J. T. Hastings (U. Kentucky), H. I. Smith
Sponsorship: DARPA

In scanning-electron-beam lithography (SEBL), distortion in the electron-beam deflection field (i.e., intrafield distortion) leads to systematic pattern-placement errors. These are particularly detrimental to photonic devices, which depend on coherent interference. Intrafield-distortion arises from imperfections in the electron optics, and errors in the digital-to-analog conversion and field-calibration electronics. The intrafield-distortion of our Raith 150 SEBL system was measured by comparing a written grid to a precision reference grid, generated by interference lithography. Figure 1(a) and 1(b) illustrate maps of the Raith's intrafield-distortion for a 100□m field in x and y direction, respectively.

Optical microring-resonator filters in high-index-contrast materials, such as Si or Si3N4, require 1-nm-level pattern placement precision. In fabricating such devices with SEBL, intrafield-distortion is manifested in the deviation of resonant frequency from design values. Based on the distortion maps, we corrected the intrafield-distortion in second-order microring-resonator filters by pre-distorting the beam positions in the layout. Figure 2(a) and 2(b) show the statistical results of resonant-frequency mismatch without and with intrafield-distortion correction, respectively. By applying distortion correction, the average resonant-frequency mismatch is reduced from -8.6GHz to 0.28GHz.

REFERENCES

[1] J. Sun, C. W. Holzwarth, M. Dahlem, J. T. Hastings, and H. I. Smith, "Accurate frequency alignment in fabrication of high-order microring-resonator filters," *Optics Express*, vol. 16, no. 20, pp. 15958-15963, Sept. 2008.

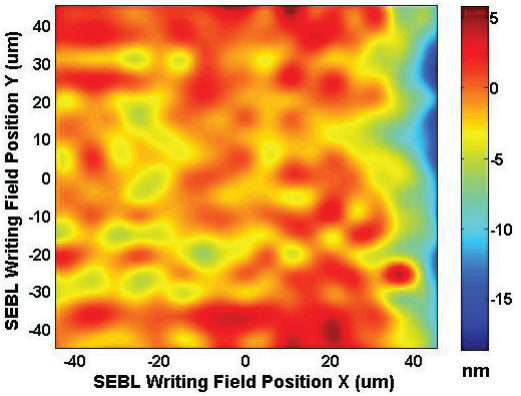


FIGURE 1(A): Raith's Intrafield Distortion in x-direction in 100mm field

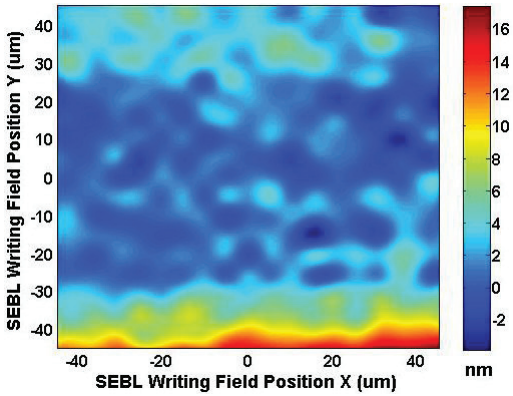


FIGURE 1(B). Raith's Intrafield Distortion in y-direction in 100mm field

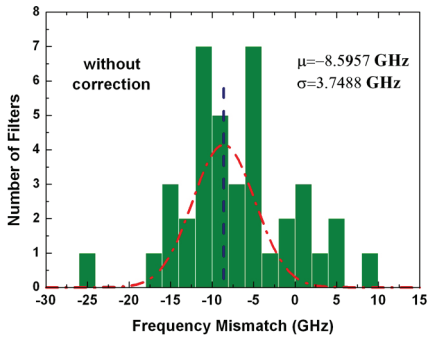


FIGURE 2(A): Statistics of the frequency mismatch of a number of 2nd-order ring resonators without intrafield distortion correction

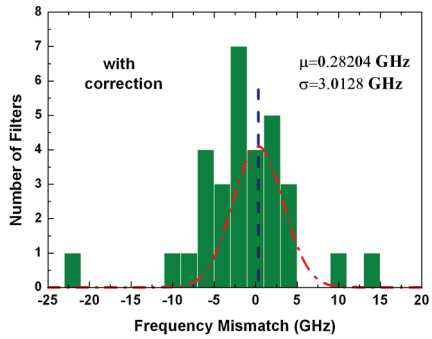


FIGURE 2(B): Statistics of the frequency mismatch of a number of 2nd-order ring resonators with intrafield distortion correction

Microscopy Beyond the Diffraction Limit Using Absorbance Modulation

H.-Y. Tsai, R. Menon, H. I. Smith

Sponsorship: Deshpande Center for Technological Innovation

Absorbance Modulation Imaging (AMI) is an approach to overcome the optical diffraction limit in the far–field in able to achieve macro-molecular resolution with photons.

AMI relies on an absorbance-modulation layer (AML), composed of photochromic molecules. Illumination at one wavelength, l_2, renders the AML opaque, while illumination at a shorter wavelength, l_1, renders it transparent. When illuminated with a ring-shaped spot at l_2 co-incident with a focused spot at l_1, the dynamic competition results in a nanoscale aperture, through which l_1 can penetrate to the substrate beneath, as illustrated in Figure 1. The size of the aperture is limited only by the photo-kinetic parameters of the AML and the intensity ratio of the two illuminating wavelengths, not the absolute intensities [1]. By scanning this dynamic nanoscale aperture over the sample, resolution beyond the far-field diffraction limit is achieved. A related technique was demonstrated in stimulated-emission-depletion (STED) fluorescence microscopy [2], but AMI can operate at much lower illumination intensity and does not require fluorescent markers.

In an AMI microscope, collimated beams at l_1 and l_2 illuminate the dichromat, a binary phase element that creates a ring-shaped spot at l_2 and a round spot at l_1. Dichromats are composed of concentric circular zones whose radii and phase shift are selected based on a nonlinear-optimization algorithm [3] The dichromats can readily be fabricated using electron beam lithography in dielectric materials, such as poly-methylmethacrylate (PMMA) or hydrogen silsesquioxane (HSQ), enabling the fabrication of large arrays of dichromats with high optical uniformity [4]. The point-spread functions (PSF) of the dichromats were verified through photoresist exposures, and PSF compression via absorbance modulation was demonstrated in lithography with NA=0.55 dichromats. As indicated in Figure 2, l_1 illumination is focused more tightly as the intensity at l_2 is increased relative to that at l_1. The full-width at half-maximum (FWHM) of the l_1 PSF decreased from 300 nm to 250 nm when the ratio of the intensity at l_2 to that at l_1 is 20, illustrating the tighter focusing enabled by absorbance modulation [5].

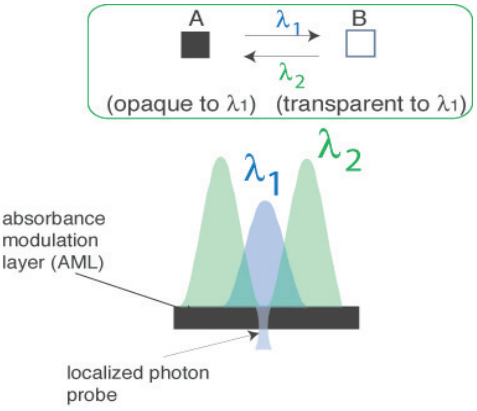


FIGURE 1: Concept and illumination configuration for absorbance modulation. Through dynamic competition of the reversible transitions in the AML, the ring illumination at l_2 creates a sub-wavelength aperture for l_1 in the AML through which the underlying object is illuminated.

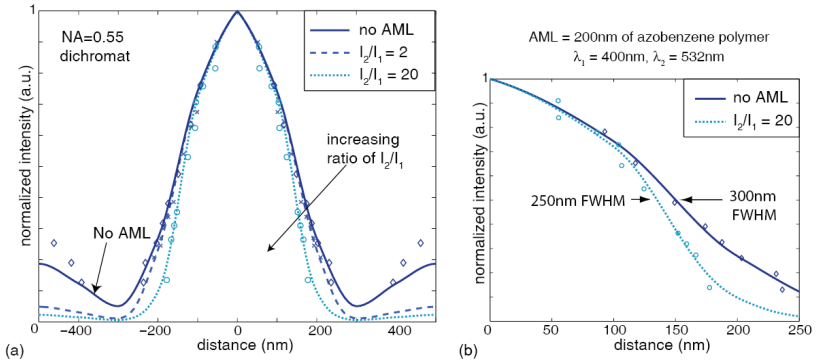


FIGURE 2: PSF compression via absorbance modulation in lithography. As I_2/I_1 increases, the I_1 illumination beyond the film is focused more tightly. (I_1 and I_2 are the incident intensities at I_1 and I_2, respectively.) (a) Solid lines show simulated PSF at I_1 without AML. Dashed and dotted lines shows simulated PSF at I_1 for I_2/I_1=2 and 20, respectively. The crosses show the corresponding experimental data. Diamonds, crosses, and circles represent experimental data correspondingly. (b) FWHM compression from 300nm to 250nm.

REFERENCES

[1] R. Menon and H. I. Smith, "Absorbance modulation optical lithography," *J. Opt. Soc. Am. A*, vol. 23, no. 9, pp. 2290-2294, Sept. 2006.

[2] S.W. Hell and J. Wichmann, "Breaking the diffraction resolution limit by stimulated emission: stimulated-emission-depletion fluorescence microscopy," *Optics Lett.*, vol. 19, no. 11, pp. 780-782, June, 1994.

[3] R. Menon, P. Rogge, and H.-Y. Tsai, "Design of diffractive lenses that generate optical nulls without phase singularities," *J. Opt. Soc. Am. A*, vol. 26, no. 2, pp. 297-304, Jan. 2009.

[4] D. Gil, R. Menon, and H. I. Smith, "Fabrication of high-numerical-aperture phase zone plates with a single lithography exposure and no etching," *J. Vac. Sci. Technol. B*, vol. 21, pp. 2956-2960, Dec. 2003.

[5] H.-Y. Tsai, H. I. Smith, and R. Menon, "Reduction of focal-spot size using dichromats in absorbance modulation," *Optics Letters*, vol. 33, no. 24, pp. 2916-2918, Dec. 2008.

Research Centers

Center for Integrated Circuits and Systems

Professor Hae-Seung Lee, Director

The Center for Integrated Circuits and Systems (CICS) at MIT, established in early 1998, is an industrial consortium created to promote new research initiatives in circuits and systems design, as well as to promote a tighter technical relationship between MIT's research and relevant industry. Seven faculty members participate in the CICS: Hae-Seung Lee (director), Duane Boning, Anantha Chandrakasan, Joel Dawson, David Perreault, Charles Sodini, and Vladimir Stojanovic. CICS investigates a wide range of circuits and systems, including wireless and wireline communication, high-speed and RF circuits, microsensor/actuator systems, imagers, digital and analog signal processing circuits, and power conversion circuits, among others.

We strongly believe in the synergistic relationship between industry and academia, especially in practical research areas of integrated circuits and systems. CICS is designed to be the conduit for such synergy. At present, participating companies include Analog Devices, Bosch, Intel, IBM, Linear Technology, Marvell Technology Group, Maxim Integrated Products, Media Tek, National Semiconductor, Qualcomm, and Texas Instruments.

CICS's research portfolio includes all research projects that the seven participating faculty members conduct, regardless of source(s) of funding, with a few exceptions.

(A very small number of projects have restrictions on information dissemination placed on them due to the nature of funding.)

Technical interaction between industry and MIT researchers occurs on both a broad and individual level. Since its inception, CICS recognized the importance of holding technical meetings to facilitate communication among MIT faculty, students, and industry. We hold two informal technical meetings per year open to participating companies. Throughout each full-day meeting, faculty and students present their research, often presenting early concepts, designs, and results that have not been published yet, giving early access to meeting attendees. Participating companies then offer valuable technical feedback, as well as suggestions for future research. We have held bi-annual meetings each year, and the response from industry has been overwhelmingly positive.

More intimate interaction between MIT researchers and industry takes place during work on projects of particular interest to participating companies. Companies may invite students to give on-site presentations, or they may offer students summer employment. Additionally, companies may send visiting scholars to MIT. The result is truly synergistic, and it will have a lasting impact on the field of integrated circuits and systems.

Intelligent Transporation Research Center

Dr. Ichiro Masaki, Director

Transportation is an important infrastructure for our society. It is time to propose a new transportation scheme for resolving the increasing transportation problems. In responding to social needs, MIT's Microsystems Technology Laboratories established the Intelligent Transportation Research Center (ITRC) in September 1998 as a contact point of industry, government, and academia for ITS research and development.

ITRC focuses on the key Intelligent Transportation Systems (ITS) technologies, including an integrated network of transportation information, automatic crash and incident detection, notification and response, advanced crash avoidance technology, advanced transportation monitoring and management, etc., in order to improve safety, security, efficiency, mobile access, and environment. There are two emphases for research conduced in the center:

- The integration of component technology research and system design research.
- The integration of technical possibilities and social needs.

ITRC proposes the incremental conversion and development process from current to near- and far-future systems and develops enabling key components in collaboration with the government, industries, and other institutions. Other necessary steps are the integration of technical, social, economical, and political aspects. The integration of the Intelligent Transportation Systems in different countries is also essential. The integration of vehicles, roads, and other modes of transportation, such as railways and public buses, is all imperative.

These integrations are fulfilled with the cooperation of researchers in various fields, including the Microsystems Technology Laboratory (MTL), the Research Laboratory of Electronics (RLE), the Artificial Intelligence Laboratory (AI), the Center for Transportation Studies (CTS), the Age Laboratory, the Department of Electrical Engineering and Computer Science, the Department of Civil and Environmental Engineering, the Department of Aeronautics and Astronautics, and the Sloan School of Management. The research center has 8 MIT faculty and several visiting professors and scientists. The director of the center is Dr. Ichiro Masaki.

MIT Center for Integrated Photonic Systems

Professor Rajeev J. Ram, Director

The goals of the Center for Integrated Photonic Systems are:

1. To provide leadership and direction for research and development in photonics.

The core activity of CIPS is the development of a long-range vision for research and the development of integrated photonic devices and systems. CIPS will host forums and facilitate working groups with industrial consortium members to identify and discuss technology and road-mapping issues:

- technology directions
- potential disruptive technologies
- technical barriers (gaps)
- actions needed to enable future-generation systems, and
- manufacturing and market issues that drive timing of technology deployment.

As an academic institution we can work openly with a variety of different organizations in developing and gathering input for our models. Whether it is performance data for new devices "in the lab," yield data for existing manufacturing processes, planning documents, or first-hand observations of the corporate decision making process, CIPS researchers benefit greatly from the unique relationship between MIT and industry. The level of detail and intellectual rigor of the models being developed here is complemented by the high quality of data available to us. CIPS researchers are developing models of optical and electronic devices, the packages they are wrapped inside, the manufacturing processes that assemble them, the standards that define them, the market that buys them, and the policy processes that influence their deployment.

2. To foster an Institute wide community of researchers in the field of integrated photonics & systems.

The Departments of Electrical Engineering and Computer Science, Materials Science and Engineering, Mechanical Engineering and Economics are consistently ranked as the top graduate programs in the country. Likewise, the Sloan School of Management has consistently ranked first in the nation in the areas of information technology, operations research, and supply chain management. CIPS leverages MIT's strengths, by unifying the photonics researchers in these departments and laboratories to focus on technological developments in photonics. The combined volume of research funds in the photonics area at MIT exceeds $20 million dollars annually. The faculty and staff at MIT in photonics-related areas have included Claude Shannon (founder of information theory), Charles Townes (inventor of the laser), Robert Rediker (inventor of the semiconductor lasers), and Hermann Haus (inventor of the single-frequency semiconductor laser & ultrafast optical switch). CIPS-affiliated faculty and staff continue this tradition of excellence in areas ranging from optical network architectures, to novel optical devices, to novel photonic materials.

3. To integrate member companies into the MIT photonics community.

CIPS will host annual meetings and seminars in photonics. For CIPS member companies, focused visits to the Institute for individual companies will be organized with faculty and graduate students. In addition, CIPS will hold forums geared towards the creation of campus-industry teams to pursue large-scale research programs. CIPS will host poster sessions at the annual meeting so as to introduce graduate students and their research to industry. CIPS publications will include a resume book of recent graduate students in the area of photonics. Graduates of the Massachusetts Institute of Technology have founded 4,000 firms which, in 1994 alone, employed at least 1.1 million people and generated $232 billion of world sales. Photonics related companies founded by alumni include Sycamore Networks, Analog Devices, Texas Instruments, Hewlett-Packard, and 3Com as well as recent start-ups such as OmniGuide.

Member companies have the opportunity to guide the research of CIPS faculty and students through the Working Groups (WGs) and individual graduate student awards.

MEMS@MIT

Professor Martin A. Schmidt, Director

The MEMS@MIT Center serves to unite the wide-ranging campus activities in micro/nano systems and MEMS with forward-looking industrial organizations. Currently, MEMS@MIT is composed of more than 150 faculty, students, and staff working on a broad research agenda and supported by more than $15 million/year in research sponsorship. The MEMS research efforts on campus focus on four overarching themes:

1) Materials, Processes, and Devices for MEMS - including work on piezoelectrics, magnetics, materials/package reliability, DRIE, wafer bonding, plastic fabrication, and printed MEMS

2) Biological and Chemical MEMS - includes cell manipulation, DNA and protein processing, biomolecule detection, medical sensors, microreactors, micro gas analyzers, and microfluidics

3) Actuators and Power MEMS - includeing switches, mirrors, pumps, turbines, fuel cells, thermophotovoltaics, chemical lasers, and energy harvesting

4) Sensors, Systems, and Modeling - includes wireless sensors, pressure sensing systems, and CAD for MEMS

Membership benefits include:

- Insight into newest ideas in MEMS
- Early access to research results
- Early awareness of IP generated for licensing
- Access to high-quality continuing education materials
- Partnering for federal or other funding opportunities
- Recruitment of leading MIT graduates

Faculty Research Staff & Publications

Akintunde I. (Tayo) Akinwande
Professor
Department of Electrical Engineering and Computer Science

COLLABORATORS
C. G. Sodini, MIT
V. Bulović, MIT
H. I. Smith, MIT
M. A. Schmidt, MIT
B. E. Gnade, UT Dallas
A. A. Seshia, University of Cambridge

RESEARCH STAFF
L.F. Velasquez-Garcia, Res. Scientist, MTL
Xiaochi Wang, Post-Doc. Assc., MTL

GRADUATE STUDENTS
K. Cheung, Res. Asst., EECS
M. A. Smith, GEM Fellow, DMSE
A. I. Wang, Res. Asst., EECS
M. E. Swanwick, Gates Cambridge Trust Fellow, EECS
S. A. Guerrera, Res. Asst., EECS
Ying Niu, Res. Asst., EECS

SUPPORT STAFF
C. Collins, Admin. Asst. II

L. F. Velásquez-García and A. I. Akinwande, "A MEMS CNT-based Neutralizer for Micro-propulsion Applications," IEPC-2007-253, Presented at the *30th International Electric Propulsion Conference*, Florence, Italy, September 17-20, 2007.

B. Gassend, L. F. Velasquez-Garcıa, A. I. Akinwande, and M. Martınez-Sanchez, "A Fully-Integrated Microfabricated Externally-Wetted Electrospray Thruster," IEPC-2007-233, Presented at the *30th International Electric Propulsion Conference*, Florence, Italy, September 17-20, 2007.

L. F. Velásquez–García1, and A.I. Akinwande, "A PECVD CNT-Based Open Architecture Field Ionizer For Portable Mass Spectrometry," *2008 21st IEEE International Conference on Micro Electro Mechanical Systems - MEMS 2008*, pp. 742-745

B. Gassend, L. F. Velasquez-Garcıa, A. I. Akinwande, and M. Martınez-Sanchez, "Fabrication of a Fully Integrated Electrospray Array With Applications To Space Propulsion," 2008 21st IEEE International Conference on Micro Electro Mechanical Systems - MEMS 2008, pp. 976-979.

I. Nausieda, K. Ryu, I. Kymissis, A. I. Akinwande, V. Bulović, C. G. Sodini, "An Organic Active-Matrix Imager," IEEE Transactions on Electron Devices, vol. 55, No. 2, Feb. 2008, pp. 527-532

L. F. Velásquez-García, L. Chen and A. I. Akinwande, "Recent MEMS/NEMS Activities at the Microsystems Technology Laboratories of MIT," the International Display Workshop, The 14th International Display Workshops, IDW '07, Saporo Convention Center, Saporo, Japan, December 3-5, 2007.

A. Wang, K. Ryu, J. Perkins, I. Nausieda, B. Yaglioglu, V. Bulović, C. Sodini, A. Akinwande, "Near-Room-Temperature Processed Integrated Metal Oxide Field Effect Transistor for Large Area Electronics," MRS 2007 Fall Meeting, Symposium, Large-Area Processing and Patterning for Active Optical and Electronic Devices, Boston MA, USA, November 26-30, 2007.

L. F. Velasquez-Garcia and A. I. Akinwande, "Fabrication of large arrays of high-aspect-ratio single-crystal silicon columns with isolated vertically aligned multi-walled carbon nanotube tips," Nanotechnology, v 19, n 40, 8 Oct. 2008, (Cover Page Photo and Featured Article)

A. K. Sood, R. A. Redwine, Y. R. Puri, O. O. Olubuyide, N. DiLello, J. L. Hoyt, A. T. Akinwande, R. S. Balcerak, S. Horn, T. G. Bramhall, D. J. Raddack, "Design considerations for SiGe-based near infrared imaging sensor," Proc. SPIE - The International Society for Optical Engineering, v 6940, 3 April 2008, 69400M-1-9.

Kerry Cheung, L.F. Velásquez-García, and A.I. Akinwande, "Fully Batch-fabricated Linear Quadrupole Mass Filters, Hilton Head 2008, Solid State Sensors, Actuators and Microsystems Workshop, June 2008.

A. I. Akinwande, "CNT-based Sensors and Applications," Invited Paper at The International Society for Optical Engineering (SPIE) Conference, 3 April 2008.

L. F. Velasquez-Garcia, K Cheung and A. I. Akinwande, An Application of 3-D MEMS Packaging: Out-of-Plane Quadrupole Mass Filters," Journal of Microelectromechanical Systems, vol. 15, no. 5, Oct 2006 Page(s):1272 – 1280.

B. Gassend, L. F. Velasquez-Garcia and A. I. Akinwande, "Precision In-Plane Hand Assembly of Bulk-Microfabricated Components for High Voltage MEMS Arrays Applications," Journal of Microelectromechanical Systems, vol. 16, 2009.

Dimitri A. Antoniadis
Ray and Maria Stata Professor of Electrical Engineering
Department of Electrical Engineering and Computer Science

COLLABORATORS
T. Equi, FCRP Materials, Structures, and Devices Focus Center, Executive Director
Chang-Hyun Lee, Visiting Scientists, Samsung Semiconductor

GRADUATE STUDENTS
J. Hennessy, Res. Asst., EECS
J-K. Lee, Res. Asst., EECS
O. Nayfeh, Res. Asst., EECS
J. Teherani, Res. Asst., EECS

SUPPORT STAFF
W. Rokui, Admin. Asst. II

A. Khakifirooz and D.A. Antoniadis, "MOSFET performance scaling — part I: historical trends," to be published in IEEE Trans. Electron Devices, vol. 55, no. 6, June 2008.

A. Khakifirooz and D.A. Antoniadis, "MOSFET performance scaling — part II: future directions," to be published in IEEE Trans. Electron Devices, vol. 55, no. 6, June 2008.

A. Khakifirooz and, D. A. Antoniadis, "The Future of High-Performance CMOS: Trends and Requirements," Proc. of 38th European Solid-State Device Research Conference, ESSDERC, pp. 30-37, Sept. 2008 (Invited Plenary Paper).

A. Khakifirooz and, D. A. Antoniadis, "MOSFET Performance Scaling: Limitations and Future Options," IEDM 2008 Tech. Digest, pp 253-256. , December 2008(Invited Paper).

A. Khakifirooz and, D. A. Antoniadis, "Trends and requirements of future high-performance CMOS," Physical and Failure Analysis of Integrated Circuits, 2008. Proc. of IPFA 2008. 15th International Symposium, July 2008, pp. 1 – 6. (Invited Plenary Paper).

Nayfeh, O.M.; Chleirigh, C.N.; Hoyt, J.L.; Antoniadis, D.A.,"Measurement of Enhanced Gate-Controlled Band-to-Band Tunneling in Highly Strained Silicon-Germanium Diodes," Electron Device Letters, IEEE vol. 29, no. 5, May 2008 Page(s):468 – 470.

Nayfeh, O.M.; Chleirigh, C.N.; Hennessy, J.; Gomez, L.; Hoyt, J.L.; Antoniadis, D.A., "Design of Tunneling Field-Effect Transistors Using Strained-Silicon/Strained-Germanium Type-II Staggered Heterojunctions," *Electron Device Letters, IEEE*, vol. 29, no. 9, Sept. 2008 Page(s):1074 – 1077.

X. Wang, K. L. Pey, W. K. Choi, C. K. F. Ho, E. Fitzgerald, and D. Antoniadis, "Arrayed Si/SiGe Nanowire and Heterostructure Formations via Au-Assisted Wet Chemical Etching Method," Electrochem. Solid-State Lett., Vo. 12, 5, pp. K37-K40, 2009.

Marc Baldo
Associate Professor
Department of Electrical Engineering and Computer Science

COLLABORATORS
T. Van Voorhis, MIT Dept of Chemistry
T. Swager, MIT Dept of Chemistry

GRADUATE STUDENTS
K. Milaninia, Res. Asst., DMSE
T. Heidel, Res. Asst., EECS
P. Reusswig, Res. Asst., EECS
P. Jadhav, Res. Asst., EECS
J. Lee, Res. Asst., EECS
C.L. Mulder, Res. Asst., EECS

POSTDOCTORAL ASSOCIATE
C. Rotschild

SUPPORT STAFF
E. Moran, Admin. Asst. I

Currie, M.J., J.K. Mapel, T.D. Heidel, S.G. Goffri, and M. A. Baldo, "High efficiency organic solar concentrators for photovoltaics," Science, 321, 226 2008.

Celebi, K., P. Jadhav, K.M. Milaninia, M. Bora, and M. A. Baldo, "The density of states in thin film copper phthalocyanine measured by Kelvin probe force microscopy," Applied Physics Letters, 93, 083308 2008.

Bora, M., K. Celebi, J. Zuniga, C. Watson, K.M. Milaninia, and M. A. Baldo, "Near field detector for integrated surface plasmon resonance biosensor applications," Optics Express, 17, 329-336. 2009.

Mulder, C.L., L. Theogarajan, M. Currie, J.K. Mapel, M. A. Baldo, M. Vaughn, Paul Willard, B. D. Bruce, M.W. Moss, C.E. McLain, and J.P. Morseman, "Luminescent solar concentrators employing phycobilisomes," Advanced Materials, 21, 1-5. 2009.

Jadhav, P., B.N. Limketkai, and M. A. Baldo, "Effective temperature models for the electric field dependence of charge carrier mobility in tris(8-hydroxyquinoline) aluminum," invited submission to *Organic Electronics* (Book), edited by Gregor Mellor, Springer Verlag. 29 pages 2009.

Karl K. Berggren
Associate Professor
Department of Electrical Engineering and Computer Science

COLLABORATORS
M. Baldo, MIT
M. Bawendi, MIT
V. Bulović, MIT
S. Hamilton, Lincoln Labs
A.J. Kerman, Lincoln Labs
C. Ross, MIT
E. Thomas, MIT

POSTDOCTORAL ASSOCIATES
M. Csete, EECS
F. Marsili, EECS
D. Morecroft, EECS
S. Strobel, EECS

GRADUATE STUDENTS
J-B. Chang, Res, Asst., Mat. Sci
B. Cord, Res. Asst., EECS
E. Dauler, Res. Asst., EECS
X. Hu, Res. Asst., EECS
J. Leu, Res. Asst., EECS
D. Winston, Res. Asst., EECS
J. Yang, Res. Asst., EECS

UNDERGRADUATE STUDENTS
D. Aude, UROP
M. Batista, UROP
A. Chao, UROP
C. Herder, UROP
H. Korre, Harvard University
V. Ramasesh, UROP
James White, UROP

VISITING STUDENTS
L. Battistella, Politecnico di Torino
H. Duan, Lanzhou University
F. Najafi, TUM
Simon Schuster, TUM

SUPPORT STAFF
T. Kuhn, Admin. Asst.
A. Akins, Admin. Asst.
J. Daley, Project Technician, NSL
M. Mondol, Facility Manager,SEBL
L. LaForce, Shop Helper, NSL

Anant, V., A.J. Kerman, E.A. Dauler, J.K.W. Yang, K.M. Rosfjord, and K.K. Berggren, "Optical Properties of Superconducting Nanowire Single-Photon Detectors," Optics Express, vol. 16, pp. 10750-10761, 3 July 2008.

Bita, I., J.K.W. Yang, Y.-S. Jung, C.A. Ross, E.L. Thomas, and Karl K. Berggren, "Graphoepitaxy of Self-Assembled Block Copolymers on Two-Dimensional Periodic Patterned Templates," Science, vol. 321, pp. 939-943, 15 August 2008.

Berns, D.M., M.S. Rudner, S.O. Valenzuela, K.K. Berggren, W.D. Oliver, L.S. Levitov, and T.P. Orlando, "Amplitude Spectroscopy of a Solid-State Artificial Atom," Nature, vol. 455, pp. 51-57, 4 September 2008.

Hashemi, P., M. Canonico, J.K.W. Yang, L. Gomez, K.K. Berggren, and J. L. Hoyt, "Fabrication and Characterization of Suspended Uniaxial Tensile Strained-Si Nanowires for Gate-All-Around n-MOSFETs," ECS (Electrochemical Society) Transactions, vol. 16, pp. 57-68, October 2008.

Wu, W., W.M. Tong, J. Bartman, Y. Chen, R. Walmsley, Z. Yu, Q. Xia, I. Park, C. Picciotto, J. Gao, S.-Y. Wang, D. Morecroft, J.K.W. Yang, K.K. Berggren, and R.S. Williams, "Sub-10 nm Nanoimprint Lithography by Wafer Bowing," Nano Letters, vol. 8, No. 11, pp. 3865-3869, 12 November 2008.

Dauler, E.A., M.J. Stevens, B. Baek, R. Molnar, S.A. Hamilton, R.P. Mirin, S.-W. Nam, and K.K. Berggren, "Measuring intensity correlations with a two-element superconducting nanowire single photon detector," Physical Review A, vol. 78, 053826 (2008).

Ross, C.A., Y.S. Jung, V.P.Chuang, F. Ilievski, J.K.W. Yang, I. Bita, E.L. Thomas, H.I. Smith, K.K. Berggren, J.G.Vansco, and J.Y. Cheng, "Si-Containing Block Copolymers for Self-Assembled Nanolithography (invited)," Journal of Vacuum Science and Technology B, vol. 26 No. 6., pp. 2489-2494 (Nov/Dec 2008).

Dauler, E.A., A.J. Kerman, B.S. Robinson, J.K.W. Yang, B. Voronov, G. Gol'tsman, S.A. Hamilton, and K.K. Berggren, "Photon-Number-Resolution with Sub-30-ps Timing using Multi-Element Superconducting Nanowire Single Photon Detectors," Journal of Modern Optics, vol. 56, No. 2 & 3, pp. 364-373 (January 2009).

Sangeeta N. Bhatia
Professor
Harvard-MIT Division of Health Sciences & Technology
Department of Electrical Engineering and Computer Science

COLLABORATORS
C. Chen, UPenn
B. Engelward, MIT Biological Eng.
T. Golub, Broad Institute
C. Marcus, Harvard
L. Mahadevan, Harvard University
D. Melton, Harvard University
E. Ruoslahti, Burnham Institute
M. Sailor, UCSD
R. Sasisekharan, MIT
P. Sharp, MIT
J. Shah, Harvard
S. Suresh, MIT
K. Van Vliet, MIT
R. Weissleder, HMS

POSTDOCTORAL ASSOCIATES
N. Singh
D. Wood
S. March
K. Stevens
R. Shwartz

GRADUATE STUDENTS
A. Chen, Res. Asst., HST
G. von Maltzahn, Res. Asst., HST
J. Shan, Res. Asst., HST
Y. Ren, MD/PhD, HST
N. Reticker-Flynn, Res. Asst., MechE
K. Trehan, Res. Asst., HST
K. Lin, Res. Asst., ChemE
C. Li, Res. Asst., ChemE

SUPPORT STAFF
S. Kangiser, Admin. Asst. II
S. Katz, Laboratory Manager
C. Powell, Technical Asst.
G. Underhill, Senior Research Scientist

Simberg, D., Park, J.-H., Karmali, P. P., Zhang, W.-M., Merkulov, S., McCrae, K., Bhatia, S. N., Sailor, M. and Ruoslahti, E. (2009 in press): Differential proteomics analysis of the surface heterogeneity of dextran iron oxide nanoparticles and the implications for their in vivo clearance. *Biomaterials*, 30: 3926-3933.

March, S., Hui, E. E., Underhill, G. H., Khetani, S., and Bhatia, S. N. (2009 in press). Microenvironmental regulation of the sinusoidal endothelial cell phenotype in vitro. *Hepatology.*

von Maltzahn, G., Centrone, A., Park, J.-H., Ramanathan, R., Sailor, M. J., Hatton, T. A., and Bhatia, S. N. (2009 in press): SERS-Coded gold nanorods as a multifunctional platform for densely multiplexed near-infrared imaging and photothermal heating. *Advanced Materials.*

von Maltzahn, G., Park, J.-H., Agrawal, A, Bandaru, N. K., Das, S. K., Sailor, M. J., and Bhatia, S. N. (2009 in press): Computationally-guided photothermal tumor therapy using long-circulating gold nanorod antennas. *Cancer Research.*

Park, J.-H., von Maltzahn, G., Zhang, L., Derfus, A. M., Simberg, D., Harris, T. J., Ruoslahti, E., Bhatia, S. N., and Sailor, M. J. (2009): Systematic surface engineering of magnetic nanoworms for in vivo tumor targeting. *Small.* 5(6):694-700.

Park, J.-H., Gu, L., von Maltzahn, G., Ruoslahti, E, Bhatia, S. N., and Sailor, M. J. (2009): Biodegradable luminescent porous silicon nanoparticles for in vivo applications. *Nature Materials,* 8: 331-336.

Higgins, J., Eddington, D., Bhatia, S. N., Mahadevan, L. (2009): Statistical dynamics of flowing red blood cells by morphological image processing. *PLoS Computational Biology.* 5 (2), e1000288.

Chen, A. A.[†], Khetani, S. R.[†], Lee, S., Bhatia, S. N., Van Vliet, K. J. (2009, in press): Modulation of hepatocyte phenotype in vitro via chemomechanical tuning of polyelectrolyte multilayers. *Biomaterials* 30: 1113-1120. [†] These authors contributed equally.

Alvarez, S. D., Derfus, A. M., Schwartz, M. P., Bhatia, S. N., Sailor, M. J. (2008): The compatibility of hepatocytes with chemically modified porous silicon with reference to in vitro biosensors. *Biomaterials*, 30: 26-34.

Khetani, S. R., Chen, A. A., Ranscht, B., and Bhatia, S. N. (2008): T-cadherin modulates hepatocyte functions in vitro. *FASEB Journal*, 22:3678-3775.

J. H. Park, G. von Maltzahn, M. P. Schwartz, E. Ruoslahti, S. N. Bhatia, M. J. Sailor, "Magnetic iron oxide nanoworms for tumor targeting and imaging," *Advanced Materials,* vol. 20, no. 9, pp. 1630-1635, May 2008.

Flaim, C. J., Teng D, Chien, S, and Bhatia, S. N. (2008). Combinatorial signaling microenvironments for studying stem cell fate. *Stem Cells and Development,* 17: 1–11.

S. R. Khetani and S. N. Bhatia, "Microscale human liver tissue for drug development," *Nature Biotechnology,* vol. 26, no. 1, pp. 120-126, Jan. 2008.

Albrecht, D. R., Underhill, G. H., Mendelson, A., Bhatia, S. N. (2007). Multiphase electropatterning of cells and biomaterials. *Lab on a Chip,* 7: 702 – 709.

von Maltzahn, G. [†], Min, D.-H. [†], Zhang, Y., Park, J.-H., Harris, T. J., Sailor, M., Bhatia, S. N. (2007): Nanoparticle self-assembly directed by antagonistic kinase and phosphatase activities. *Advanced Materials*, 19(21): 3579-3583. [†] These authors contributed equally.

Underhill, G. H. and Bhatia, S. N. (2007): High-throughput analysis of signals regulating stem cell fate and function. *Current Opinion in Chemical Biology,* 11: 357-366.

Evans, A. R., Euteneuer, S., Chavez, E., Mullen, L. M., Hui, E. E., Bhatia, S. N., and Ryan, A. F. (2007): Laminin and fibronectin modulate inner ear spiral ganglion neurite outgrowth in an in vitro alternate choice assay. *Developmental Neurobiology,* 67(13): 1721-1730.

A. M. Derfus, A. A. Chen, D. H. Min, E. Ruoslahti, and S. N. Bhatia, "Targeted quantum dot conjugates for siRNA delivery," *Bioconjugate Chemistry,* vol. 18, no. 5, pp. 1391-1396, Sept. 2007.

J. M. Higgins, D. T. Eddington, S. N. Bhatia, and L. Mahadevan, "Sickle-cell vasoocclusion and rescue in a microfluidic device," *Proc. National Academy of Sciences,* vol. 104, no. 51, pp. 20496-20500, Dec. 2007.

A. M. Derfus, G. von Maltzahn, T. J. Harris, T. Duza, K. S. Vecchio, E. Ruoslahti, and S. N. Bhatia, "Remotely triggered release from magnetic nanoparticles," *Advanced Materials,* vol. 19, pp. 3932-3936, 2007.

G. von Maltzahn, T. J. Harris, J. H. Park, A. J. Schmidt, M. J. Sailor, and S. N. Bhatia, "Nanoparticle self-assembly gated by logical proteolytic triggers," *Journal of the American Chemical Society,* vol. 129, pp. 6064-6065, 2007.

E. E. Hui and S. N. Bhatia, "Micromechanical control of cell-cell interactions," *Proc. National Academy of Sciences,* vol. 104, pp. 5722-5726, 2007.

V. Liu Tsang, A. A. Chen, L. M. Cho, K. D. Jadin, R. L. Sah, S. DeLong, J. L. West, and S. N. Bhatia, "Fabrication of 3D hepatic tissues by additive photopatterning of cellular hydrogels," *FASEB Journal*, vol. 21, pp. 790-801, 2007.

Duane S. Boning
Professor
Department of Electrical Engineering and Computer Science

COLLABORATORS
S.F. Yoon, NTU, Singapore
A. Philipossian, Univ. of Arizona

GRADUATE STUDENTS
K. Balakrishnan, Res. Asst., EECS
A. Chang, Res. Asst., EECS
J. Diaz, Res. Asst., EECS
N. Drego, Res. Asst., EECS
W. Fan, Res. Asst., EECS
D. Lim, Res. Asst., EECS
J. Johnson, Res. Asst., EECS
H. Taylor, Res. Asst., EECS
B. Wu, UROP, EECS

VISITING SCIENTISTS
J. Lee, Samsung Electronics

SUPPORT STAFF
M. Whiting, Admin. Asst. II

D. Boning, K. Balakrishnan, H. Cai, N. Drego, A. Farahanchi, K. Gettings, D. Lim, A. Somani, H. Taylor, D. Truque, and X. Xie, "Variation," *IEEE Trans. on Semicond. Manuf.*, vol. 21, no. 1, pp. 63-71, Feb. 2008.

H. Taylor, D. Boning, C. Iliescu, and B. Chen, "Computationally efficient modeling of pattern dependencies in the micro-embossing of thermoplastic polymers," *Microelectronic Engineering*, vol. 85, no. 5-6, pp. 1453-1456, May-June, 2008.

K. Gettings and D. Boning, "Study of CMOS Process Variation by Multiplexing Analog Characteristics," *IEEE Trans. on Semicond. Manuf.*, vol. 21, no. 4, pp. 513-525, Nov. 2008.

N. Drego, A. Chandrakasasan, D. Boning, "Lack of Spatial Correlation in MOSFET Threshold Voltage Variation and Implications for Voltage Scaling," *IEEE Trans. on Semicond. Manuf.*, vol. 22, no. 2, pp. 245-255, May 2009.

Y. Sampurno, L. Borucki, Y. Zhuang, S. Misra, K. Holland, D. Boning, and A. Philipossian, "Characterization of Thermoset and Thermoplastic Polyurethane Pads, and Molded and Non-optimized Machined Grooving Methods for Oxide Chemical Mechanical Planarization Applications," *Thin Solid Films*, vol. 517, pp. 1719-1726, Jan. 2009.

Z. Xu, S. Li, D. J. Burns, V. Shilpiekandula, H. K. Taylor, S. F. Yoon, K. Youcef-Toumi, I. Reading, Z. Fang, J. Zhao, and D. S. Boning, "Three-Dimensional Profile Stitching Based on the Fiducial Markers for Microfluidic Devices," *Optics Communications*, vol. 282, No. 4, pp. 493-499, Feb. 2009.

H. K. Taylor and D. S. Boning, "Diffraction-based Approaches to the In-situ Measurement of Dimensional Variations in Components Produced by Thermoplastic Micro- and Nano-embossing," presented at the *5th International Symposium on Nanomanufacturing*, Singapore, Jan. 2008.

Z. G. Xu, S. G. Li, S. F. Yoon, Z. P. Fang, K. Youcef-Toumi, D. J. Burns, V. Shilpiekandula, H. K. Taylor and D. S. Boning, "Complete Surface Distinguishing and Overlapping Technology for Three-dimensional Image Processing of Micro Devices," presented at the *5th International Symposium on Nanomanufacturing*, Singapore, Jan. 2008.

H. K. Taylor, Z. Xu, L. Shiguang, K. Youcef-Toumi, S. F. Yoon, and D. S. Boning, "Moire fringe method for the measurement of distortions of hot-embossed polymeric substrates," presented at the *9th International Symposium on Laser Metrology*, Singapore, June-July 2008.

H. Taylor and D. Boning, "An Integrated Crack-Opening Method for Determining the Work of Fracture of Bonded Polymer Interfaces," presented at the *12th International Conference on Miniaturized Systems for Chemistry and Life Sciences (μTAS 2008)*, San Diego, CA, Oct. 2008.

N. Drego, A. Chandrakasan, and D. Boning, "An All-Digital, Highly Scalable Architecture for Measurement of Spatial Variation in Digital Circuits," presented at the *IEEE Asian Solid-State Circuit Conf.*, Fukuoka, Japan, Nov. 2008.

H. Taylor, D. S. Boning, C. I. Iliescu, B. Chen, Y.-C. Lam, and X. Chen, "Modeling Pattern Dependencies in the Micro-scale Embossing of Polymeric Layers," presented at the *Micro- and Nanotechnology: Materials, Processes, Packaging, and Systems IV*, Proc. of SPIE, vol. 7269, Melbourne, Australia, Dec. 2008.

A. Philipossian, Y. Sampurno, L. Borucki, Y. Zhuang, S. Misra, K. Holland, and D. Boning, "Characterization of Thermoset and Thermoplastic Polyurethane Pads, and Molded and Non-optimized Machined Grooving Methods for Oxide CMP Applications," presented at the *Clarkson Workshop on Chemical-Mechanical Polishing*, Lake Placid, NY, Aug. 2008.

D. Boning, K. Balakrishnan, A. Chang, N. Drego, W. Fan, J. Johnson, and H. Taylor, "Measuring and Modeling IC Variability at the Process, Device, and Circuit Levels," presented at the *ICCAD Workshop on Test Structure Design for Variability Characterization (TSD)*, San Jose, CA, Nov. 2008.

D. Boning, J. Johnson, H. McCulloh, and N. Patel, "The Evolution of Pattern-Density in CMP Modeling," presented at the *Symposium on Chemical-Mechancial Planarization, Materials Research Society Spring Meeting*, San Francisco, CA, April 2009.

V. Michael Bove, Jr.
Principal Research Scientist
Media Arts and Sciences Program/Media Laboratory

COLLABORATORS
W. J. Plesniak, Brigham & Women's Hospital

POSTDOCTORAL ASSOCIATES
Q. Smithwick, MIT Media Lab
Graduate Students
S. Alfaro, Res. Asst., MAS
J. Barabas, Res. Asst., MAS
D. Smalley, Res. Asst., MAS
A. L. Santos, Res. Asst., MAS

SUPPORT STAFF
K. Hall, Admin. Asst. II

Q. Y. J. Smithwick, J. Barabas, D. E. Smalley, and V. M. Bove, Jr., "Real-time shader rendering of holographic stereograms," *Proc. SPIE Practical Holography XXIII,* v. 7233, p. 723302, 2009.

B.T. Taylor and V.M. Bove, Jr., "Graspables: grasp-recognition as a user interface," *Proc. ACM CHI 2009*, 2009.

S. A. Benton and V. M. Bove. Jr., *Holographic Imaging*, Wiley, New York, 2008.

Q. Y. J. Smithwick, D. E. Smalley, V. M. Bove, Jr., and J. Barabas, "Progress in Holographic Video Displays Based on Guided-Wave Acousto-Optic Devices," *Proc. SPIE Practical Holography XXII*, 6912, 69120H, 2008.

D. E. Smalley, Q. Y. J. Smithwick, and V. M. Bove, Jr., "Holographic Video Display Based on Guided-Wave Acousto-Optic Devices," *Proc. SPIE Practical Holography XXI*, 6488, 64880L, 2007.

W. Plesniak, M. Halle, V. M. Bove, Jr., J. Barabas, and R. Pappu, "Reconfigurable Image Projection (RIP) Holograms," *Optical Engineering*, 45, 115801, Nov. 2006.

V. M. Bove, Jr., W. J. Plesniak, T. Quentmeyer, and J. Barabas, "Real-Time Holographic Video Images with Commodity PC Hardware," *Proc. SPIE Stereoscopic Displays and Applications,* 5664A, 2005.

Vladimir Bulović
Associate Professor
Department of Electrical Engineering and Computer Science

COLLABORATORS
A. I. Akinwande, MIT
M. A. Baldo, MIT
M. Bawendi, MIT
T. Bloomstein, Lincoln Lab.
T. Etheridge, HP
F. Jaworski, Raytheon
L. Rolly, HP
M. A. Schmidt, MIT
C. G. Sodini, MIT
T. Swager, MIT

POSTDOCTORAL ASSOCIATES
C. Packard
M. Panzer
J.) Tischler
B. Yaglioglu
N. Zhao

GRADUATE STUDENTS
P. Anikeeva, Res. Asst., DMSE
A. Arango, Res. Asst., EECS
M. S. Bradley, Res. Asst., EECS
D. Friend, Res. Asst., EECS
J. Ho, Res. Asst., EECS
Q. Hu, Res. Asst., Harvard Univ.
T. Osedach, Res. Asst., Harvard Univ.
S. Paydavosi, Res. Asst., EECS
J. Rowehl, Res. Asst., DMSE
Y. Shirasaki , Res. Asst., EECS
H. Tang , Res. Asst., EECS
V. Wood , Res. Asst., EECS
J. Yu , Res. Asst., EECS

SUPPORT STAFF
M. Pegis, Admin. Asst.

C. Madigan , E. Howe, V. Bulović, P. Mardilović, P. Kornilovitch, "Planarization in electrochemically fabricated nanodimensional films," *Journal of Physical Chemistry C* 112, 7318 (2008).

I. Nausieda, K. Ryu, I. Kymissis, A. Akinwande, V. Bulović, C.G. Sodini, "An Organic Active-Matrix Imager," *IEEE Transactions on Electron Devices* 55, 527 (2008).

J.M. Caruge, J.E. Halpert, V. Wood, V. Bulović, and M.G. Bawendi, "Colloidal Quantum-Dot Light-Emitting Diodes with Metal-Oxide Charge Transport Layers," *Nature Photonics* 2, 247 (2008).

J. Yu and V. Bulović, "Using Integrated Optical Feedback to Counter Pixel Aging and Stabilize Light Output of Organic LED Display Technology," *IEEE Journal of Display Technology* 4, 308 (2008).

J. Ho, A. Arango, and V. Bulović, "Lateral Organic Bi-layer Heterojunction Photoconductors," *Applied Physics Letters* 93, 063305 (2008).

P. O. Anikeeva, C.F. Madigan, J.E. Halpert, M.G. Bawendi, V. Bulović, "Electronic and Excitonic Processes in Light-Emitting Devices Based on Organic Materials Colloidal Quantum Dots," *Physical Review B* 78, 085434, (2008).

M. S. Bradley, J. R. Tischler, Y. Shirasaki, and V. Bulović, "Predicting the Linear Optical Response of J-aggregate Microcavity Exciton-Polariton Devices," *Physical Review B* 78, 193305 (2008).

L. Kim, P. O. Anikeeva, S. A. Coe-Sullivan, J. S. Steckel, M. G. Bawendi, and V. Bulović, "Contact Printing of Quantum Dot Light-Emitting Devices," *Nano Letters* 8, 4513 (2008).

A. C. Arango, D. C. Oertel, Y. Xu, M. G. Bawendi, and V. Bulović, "Heterojunction Photovoltaics Using Printed Colloidal Quantum Dots as a Photosensitive Layer," *Nano Letters* 9, 860 (2009).

T. P. Osedach, S. M. Geyer, J. C. Ho, A. C. Arango, M. G. Bawendi, and V. Bulović, "Lateral Heterojunction Photodetector Consisting of Molecular Organic and Colloidal Quantum Dot Thin Films," *Applied Physics Letters* 94, 043307 (2009).

A. Reina, X. Jia, J. Ho, D. Nezich, H. Son, V. Bulović, M. S. Dresselhaus, and J. Kong, "Large Area, Few-Layer Graphene Films on Arbitrary Substrates by Chemical Vapor Deposition," *Nano Letters* 9, 30 (2009).

J. E. Halpert, J. R. Tischler, G. Nair, B. J. Walker, W. Liu, V. Bulović, M. G. Bawendi, "Electrostatic Formation of Quantum Dot/J-aggregate FRET Pairs in Solution," *Journal of Physical Chemistry C* 113, 9986 (2009).

V. Wood, M. J. Panzer, J. Chen, M. S. Bradley, J. E. Halpert, M. G. Bawendi, and V. Bulović, "Inkjet-Printed Quantum Dot–Polymer Composites for Full-Color AC-Driven Displays," *Advanced Materials* 21, 2151 (2009).

V. Wood, J. E. Halpert, M. J. Panzer, M. G. Bawendi, V. Bulović, "Alternating Current Driven Electroluminescence from ZnSe/ZnS:Mn/ZnS Nanocrystals," *Nano Letters* 9, 2367 (2009).

J. Mei, M. S. Bradley, V. Bulović, "Photoluminescence quenching of tris-(8-hydroxyquinoline) aluminum thin films at interfaces with metal oxide films of different conductivities," *Physical Review B* 79, 235205 (2009).

J. M. W. Chan, J. R. Tischler, S. E. Kooi, V. Bulović, T. M. Swager "Synthesis of J-Aggregating Dibenz[a,J] anthracene-Based Macrocycles," *Journal of American Chemical Society* 131, 5659 (2009).

Anantha P. Chandrakasan

Joseph F. & Nancy P. Keithley Professor of Electrical Engineering
Department of Electrical Engineering and Computer Science

GRADUATE STUDENTS
S. Bandyopadhyay, Res. Asst., EECS
M. Bhardwaj, Res. Asst., EECS
J. Bohorquez, Res. Asst., EECS (co-supervised with Prof. J. Dawson)
F. Chen, Res. Asst., EECS (co-supervised with Prof. V. Stojanović)
H.W. Chung, Res. Asst., EECS
D. Daly, Res. Asst., EECS
N. Drego, Res. Asst., EECS (co-supervised with Prof. D. Boning)
D. Finchelstein, Res. Asst., EECS
Y. Koken, Res. Asst., EECS
J. Kwong, Res. Asst., EECS
P. Lajevardi, Res. Asst., (co-supervised with Prof. H. Lee)
B. Lam, Res. Asst., EECS
K-J. Lee, Res. Asst., EECS (co-supervised with Prof. J. Kong)
S. Lee, Res. Asst., EECS (co-supervised with Prof. H. Lee)
H. Liang, Res. Asst., EECS
P. Mercier, Res. Asst., EECS
M. Qazi, Res. Asst., EECS
Y. Ramadass, Res. Asst., EECS
R. Rithe, Res. Asst., EECS
C. Schmitt, Res. Asst., EECS
M. Sinangil, Res. Asst., EECS
V. Sze, Res. Asst., EECS
N. Verma, Res. Asst., EECS
M. Yip, Res. Asst., EECS

POSTDOCTORAL ASSOCIATE
C-C. Cheng
N. Ickes

VISITING SCIENTIST
F. Pappalardo

VISITING STUDENTS
J. Rajendrakumar
P. Sethi

SUPPORT STAFF
M. Flaherty, Senior Admin. Asst.

J. L. Bohorquez, A. P. Chandrakasan, J. L. Dawson "A 350uW CMOS MSK Transmitter and 400uW OOK Super-Regenerative Receiver for Medical Implant Communications," *IEEE Journal of Solid-State Circuits (JSSC)*, vol. 44, no. 4, pp. 1248-1259, April 2009.

A. P. Chandrakasan, F. S. Lee, D. D. Wentzloff, V. Sze, B. P. Ginsburg, P. P. Mercier, D. C. Daly, R. Blazquez, "Low-Power Impulse UWB Architectures and Circuits," *Proc. IEEE*, vol. 97, no. 2, pp. 332-352, February 2009.

T. S. Cho, K.-J. Lee, J. Kong, and A. P. Chandrakasan, "A 32-uW 1.83-kS/s Carbon Nanotube Chemical Sensor System," *IEEE JSSC*, vol. 44, no. 2, pp. 659-669, February 2009.

Y. K. Ramadass, A. P. Chandrakasan, "An Efficient Piezoelectric Energy-Harvesting Interface Circuit Using a Bias-Flip Rectifier and Shared Inductor," *IEEE International Solid-State Circuits Conference (ISSCC)*, pp. 296-297, February 2009.

P. P. Mercier, M. Bhardwaj, D. C. Daly, A. P. Chandrakasan, "A 0.55V 16Mb/s 1.6mW Non-Coherent IR-UWB Digital Baseband with +-1ns Synchronization Accuracy," *IEEE ISSCC*, pp. 252-253, February 2009.

D. C. Daly, P. P. Mercier, M. Bhardwaj, A. L. Stone, J. Voldman, R. B. Levine, J. G. Hildebrand, A. P. Chandrakasan, "A Pulsed UWB Receiver SoC for Insect Motion Control," *IEEE ISSCC*, pp. 200-201, February 2009.

N. Verma, and A. Chandrakasan, "A High-Density 45nm SRAM Using Small-Signal Non-Strobed Regenerative Sensing," *IEEE JSSC*, vol. 44, no. 1, pp. 163-173, January 2009.

J. Kwong, Y. K. Ramadass, N. Verma, and A. Chandrakasan, "A 65nm Sub-Vt Microcontroller with Integrated SRAM and Switched Capacitor DC-DC Converter," *IEEE JSSC*, vol. 44, no. 1, pp. 115-126, January 2009.

B.P. Ginsburg, and A. Chandrakasan, "Highly Interleaved 5-bit, 250-MSample/s, 1.2mW ADC with Redundant Channels in 65nm CMOS," *IEEE JSSC*, vol. 43, no. 12, pp. 2641-2650, December 2008.

L. Dolecek, M. Qazi, D. Shah, and A.P. Chandrakasan, "Breaking the Simulation Barrier: SRAM Evaluation Through Norm Minimization," *IEEE/ACM International Conference on Computer-Aided Design*, pp. 322-329, November 2008.

D. F. Finchelstein, V. Sze, M. E. Sinangil, Y. Koken, and A.P. Chandrakasan, "A Low-Power 0.7-V H.264 720p Video Decoder," *IEEE Asian Solid-State Circuits Conference*, pp. 173-176, November 2008.

N. Ickes, D. Finchelstein, and A. P. Chandrakasan, "A 10-pJ/instruction, 4-MIPS Micropower DSP for Sensor Applications," *IEEE Asian Solid-State Circuits Conference*, pp. 289-292, November 2008.

N. Drego, A. P. Chandrakasan, and D. Boning, "An All-Digital, Highly-Scalable Architecture for Measurement of Spatial Variation in Digital Circuits," *IEEE Asian Solid-State Circuits Conference*, pp. 393-396, November 2008.

V. Sze, M. Budagavi, A. P. Chandrakasan, and M. Zhou, "Parallel CABAC for Low Power Video Coding," *IEEE International Conference on Image Processing*, October 2008.

M. E. Sinangil, N. Verma, and A. P. Chandrakasan, "A reconfigurable 65nm SRAM achieving voltage scalability from 0.25-1.2V and performance scalability from 20kHz-200MHz," *European Solid-State Circuits Conference*, pp. 282-285, September 2008.

Luca Daniel
Emanuel E. Landsman Associate Professor
Department of Electrical Engineering and Computer Science

COLLABORATORS
A. Elfadel, IBM T.J.Watson,
A. Megretski, MIT
V. Stojanović, MIT
K. Sou, LTH Lund
R. Suaya, Mentor Graphics
J. White, MIT

GRADUATE STUDENTS
B. Bond, Res. Asst., EECS
Y. Hsiao, Res. Asst., EECS
Z. Mahmood, Res. Asst., EECS
E. Natarajan, Res. Asst., EECS
T. El Moselhy, Res. Asst., EECS

SUPPORT STAFF
C. Collins, Admin. Asst.

B. Bond, Z. Mahmood, R. Sredojevic, Y. Li, A. Megretski, V. Stojanović, L. Daniel, "Compact Modeling of Nonlinear Circuits using Quasi-Convex Based Stable System Identification," submitted to IEEE Transaction on Computer Aided Design of Integrated Circuits and Systems, May 2009.

T. Moselhy and L. Daniel, "Stochastic Integral Equation Solver for Efficient Variation Aware Interconnect Extraction," submitted to IEEE Transaction on Computer Aided Design of Integrated Circuits and Systems, May 2009.

B. Bond and L. Daniel, "Guaranteed Stable Projection-Based Model Reduction for Indefinite and Unstable Linear Systems," submitted to IEEE Transaction on Computer Aided Design of Integrated Circuits and Systems, May 2009.

T. Moselhy, I. M. Elfadel, and L. Daniel, "A Generalized Floating Random Walk Algorithm for Variation-Aware Electrical Extraction," submitted to IEEE Transaction on Computer Aided Design of Integrated Circuits and Systems, April 2009.

K. C. Sou, A. Megretski, L. Daniel, "Convex Relaxation Approach to the Identification of the Wiener-Hammerstein Model," submitted to IEEE Transaction on Computer Aided Design of Integrated Circuits and Systems, March 2009.

B. Bond and L. Daniel, "Stable Macromodeling for Nonlinear Descriptor Systems via Piecewise-Linear Approximation and Projection," submitted to IEEE Trans. on Computer Aided Design of Integrated Circuits and Systems, January 2009.

K. C. Sou, A. Megretski, L. Daniel, "Convex Relaxation Approach to the Identification of the Wiener-Hammerstein Model," in Proc. 47th IEEE Conference on Decision and Control, Cancun Mexico, December 2008.

T. Moselhy, I. M. Elfadel, and L. Daniel, "A Capacitance Solver for Incremental Variation-Aware Extraction," Proc. IEEE Conference on Computer-Aided Design, San Jose, November 2008.

B. Bond and L. Daniel, "Guaranteed Stable Projection-Based Model Reduction for Indefinite and Unstable Linear Systems" Proc. IEEE Conference on Computer-Aided Design, San Jose, November 2008, ***(IEEE/ACM William J. McCalla ICCAD Best Paper Award).***

T. Moselhy and L. Daniel, "Stochastic Integral Equation Solver for Efficient Variation Aware Interconnect Extraction," IEEE/ACM Design Automation Conference, Anaheim, CA, June 2008.

K. C. Sou, A. Megretski, L. Daniel, "A Quasi-Convex Optimization Approach to Parameterized Model Order Reduction. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems," Vol 27, No 3, March 2008.

B. N. Bond, L. Daniel, "A Piecewise-Linear Moment-Matching Approach to Parameterized Model-Order Reduction for Highly Nonlinear Systems," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 26 , no.: 12, page(s): 2116 - 2129, Dec. 2007.

K. C. Sou, A. Megretski, L. Daniel, "Bounding L2 Gain System Error Due to Approximations of the Nonlinear Vector Field," Proc. IEEE Conference on Computer-Aided Design, San Jose, November 2007.

B. Bond and L. Daniel, "Stabilizing Schemes for Piecewise-Linear Reduced Order Models via Projection and Weighting Functions," Proc. IEEE Conference on Computer-Aided Design, San Jose, November 2007, ***(Best Paper Award Nomination).***

T. Moselhy, L. Daniel, "Stochastic High Order Basis Functions for Volume Integral Equation with Surface Roughness," IEEE Conference on Electrical Performance of Electronic Packaging (EPEP), Oct. 2007, ***(Best Student Paper Award Nomination).***

T. Moselhy , X. Hu, L. Daniel, "pFFT in FastMaxwell: A Fast Impedance Extraction Solver for 3D Conductor Structures over Substrate," IEEE Conference on Design Automation and Test in Europe (DATE), April 2007, ***(Best Paper Award Nomination).***

Joel L. Dawson
Assistant Professor
Department of Electrical Engineering & Computer Science

GRADUATE STUDENTS
T. Barton, Res. Asst., EECS
J. Bohorquez, Res. Asst., EECS
S. Chung Res. Asst., EECS
P. Godoy, Res. Asst., EECS
T. Khanna, Res. Asst., EECS
H. Khurana, Res.Asst., EECS
Z. Lee, Res Asst., EECS
O. Ogunnika, Res. Asst., EECS
W. Sanchez, Res. Asst., EECS

SUPPORT STAFF
C. Kinsella, Admin. Asst. II

Chung, S., P.A. Godoy, T.W. Barton, E.W. Huang, D.J. Perrault, and J.L. Dawson, "Asymetric Multilevel Outphasing Architecture for Multi-Standard Transmitters," accepted for publication at the *2009 IEEE RFIC Symposium*.

Chung, S. and J.L. Dawson, "A 73.1dB SNDR Digitally Assisted Subsampler for RF Power Amplifier Linearization Systems," accepted for publication at the *2009 Symposium on VLSI Technology and Circuits*.

J.L. Bohorquez, A.P. Chandrakasan, and J. L. Dawson, "A 350μW CMOS MSK Transmitter and 400μW OOK Super-Regenerative Receiver for Medical Implant Communications," *IEEE Journal of Solid-State Circuits (VLSI Symposium Special Issue)*, pp. 1248-1259, Apr. 2009.

S. Chung, J.W. Holloway, and J.L. Dawson, "Energy-Efficient Digital Predistortion with Lookup Table Training Using Analog Cartesian Feedback," *IEEE Transactions on Microwave Theory and Techniques*, pp. 2248-2258, Oct. 2008.

P. Godoy and J.L. Dawson, "Chopper Stabilization of Analog Multipliers, Variable Gain Amplifiers, and Mixers," *IEEE Journal of Solid-State Circuits*, pp. 2311-2321, Oct. 2008.

Jesús A. del Alamo
Donner Professor, MacVicar Faculty Fellow
Department of Electrical Engineering and Computer Science

COLLABORATORS
P. C. Chao, BAE Systems
D. Greenberg, IBM
K. Hayashi, Mitsubishi Electric
J. Jimenez, Triquint Semic
A. Valdes, IBM
E. Piner, Nitronex

VISITING SCIENTISTS
Y. Ikura, Fuji Electric

POSTDOCTORAL ASSOCIATE
T. W. Kim

GRADUATE STUDENTS
U. Gogineni, Res. Asst., EECS
J. Joh, Res. Asst., EECS
D. H. Jin, Res. Asst., EECS
L. Xia, Res. Asst., EECS
S. Demirtas, Res. Asst., EECS

UNDERGRADUATE STUDENTS
A. Ojeda, EECS

SUPPORT STAFF
E. Kubicki, Admin. Asst. II

Hisaka, T., Y. Nogami, H. Sasaki, N. Yoshida, K. Hayashi, A. Villanueva, and J. A. del Alamo, "Degradation Mechanism of AlGaAs/InGaAs Power Pseudomorphic High-Electron-Mobility Transistors under Large-Signal Operation." Japanese Journal of Applied Physics, vol. 47, No. 2, pp. 833-838, 2008.

Joh, J. and J. A. del Alamo, "Critical Voltage for Electrical Degradation of GaN High Electron Mobility Transistors." IEEE Electron Device Letters vol. 29, No. 4, pp. 287-289, April 2008.

Villanueva, A. A., J. A. del Alamo, T. Hisaka, K. Hayashi, and M. Somerville, "Degradation Uniformity of RF Power GaAs PHEMTs under Electrical Stress." Invited Paper, IEEE Transactions on Device and Materials Reliability, vol. 8, No. 2, pp. 283-288, June 2008.

Joh, J., J. A. del Alamo and J. Jimenez, "A Simple Current Collapse Measurement Technique for GaN High Electron Mobility Transistors." IEEE Electron Device Letters vol. 29, No. 7, pp. 665-667, July 2008.

Kim, D-H. and J. A. del Alamo, "30 nm InAs Pseudomorphic HEMTs on InP Substrate with Current-Gain Cut-off Frequency of 628 GHz." IEEE Electron Device Letters vol. 29, No. 8, pp. 830-833, August 2008.

Chowdhury, U., J. L. Jimenez, C. Lee, E. Beam, P. Saunier, T. Balistreri, S.-Y. Park, T. Lee, J. Wang, M. J. Kim, J. Joh, and J. A. del Alamo, "TEM Observation of Crack- and Pit-Shaped Defects in Electrically Degraded GaN HEMTs." IEEE Electron Device Letters vol. 29, No. 10, pp. 1098-1100, October 2008.

Kim, D.-H. and J. A. del Alamo, "Lateral and Vertical Scaling of $In_{0.7}Ga_{0.3}As$ HEMTs for Post-Si-CMOS Logic Applications." IEEE Transactions on Electron Devices 55 (10), 2546-2553, October 2008.

Saunier, P., C. Lee, J. Jimenez, A. Balistreri, H. Dumka, H. Q. Tserng, M. Y. Kao, U. Chowdhury, P. C. Chao, K. Chu, A. Souzis, I. Eliashevich, S. Guo, J. del Alamo, J. Joh, and M. Shur, "Progress in GaN Devices, Performance and Reliability." SPIE Photonics West Conference, San Jose, CA, Jan. 20-24, 2008.

del Alamo, J. A., "CMOS Extension via III-V Compound Semiconductors." Tutorial at Spring Meeting of the Materials Research Society. San Francisco, CA, March, 2008.

del Alamo, J. A., D.-H. Kim, and N. Waldron, "III-V CMOS: Challenges and Opportunities." Invited paper at International Conference on Solid State Devices and Materials, Tsukuba, Japan, September, 2008, pp. 28-29.

Fukuda, S., T. Suemitsu, T. Otsuji, C.-H. Kim, and J. A. del Alamo, "Analysis of Gate Delay Scaling in $In_{0.7}Ga_{0.3}As$-Channel HEMTs." International Conference on Solid State Devices and Materials, Tsukuba, Japan, September, 2008, pp. 166-167.

Joh, J., J. A. del Alamo, U. Chowdhury and J. L. Jimenez, "Correlation Between RF and DC Reliability in GaN High Electron Mobility Transistors." 2008 Reliability of Compound Semiconductors Workshop, Monterey, CA, October 12, 2008, pp. 185-188.

Hisaka, T., H. Sasaki, Y. Nogami, K. Hosogi, N. Yoshida, A. A. Villanueva, J. A. del Alamo, S. Hasegawa and H. Asahi, "Degradation Mechanisms of GaAs PHEMTs under Operation in High Humidity Conditions." 2008 Reliability of Compound Semiconductors Workshop, Monterey, CA, October 12, 2008, pp. 109-113.

Joh, J., S. Demirtas, and J. A. del Alamo, "Impact of electrical degradation on trapping characteristics of GaN high electron mobility transistors." 2008 IEEE International Electron Devices Meeting, San Francisco, CA, December 15-17, 2008, pp. 461-464.

Kim, D.-H. and J. A. del Alamo, "30 nm E-mode InAs PHEMTs for THz and Future Logic Applications." 2008 IEEE International Electron Devices Meeting, San Francisco, CA, December 15-17, 2008, pp. 719-722.

Clifton G. Fonstad, Jr.
Professor
Department of Electrical Engineering and Computer Science

COLLABORATORS
E. Boyden, MIT
Yoon Soon Fatt, Nanyang Technological University, Singapore
F. J Cadieu, Queens College of CUNY
A. Postigo, Instituto de Microelectronica, Madrid, Spain
S. Prasad, Northeastern U.
M. Zahn, MIT

GRADUATE STUDENTS
S. Faminini, Res. Asst., EECS
J. Rumpler, Res. Asst., EECS
A. Zorzos, Graduate Fellow, Media Lab

UNDERGRADUATE STUDENTS
J. Diaz, EECS

SUPPORT STAFF
M. Pegis, Admin. Asst. II

Postigo, P. A, F. Suarez, A. Sanz-Heras, J. Sangrador, and C. G. Fonstad, "Growth of InP on GaAs(001) by Hydrogen-assisted Low-temperature Solid-source Molecular Beam Epitaxy," *Journal of Applied Physics*, vol. 103 (2008) 013508-1 to -5.

Perkins, J. M., and C. G. Fonstad, "Full Recess Integration of Small Diameter Low Threshold VCSELs within Si-CMOS ICs," *Optics Express*, vol. 16 (2008) 13955-193960.

Cheng, D. I., J. J. Rumpler II, J. M. Perkins, M. Zahn, C. G. Fonstad, Jr., E. S. Cramer, R. W. Zuneska, and F. J. Cadieu. "Use of Patterned Magnetic Films to Retain and Orient Micro-Components During Fluidic Assembly," presented at the *Magnetism and Magnetic Materials Annual Conference*, Austin, TX, November 2008.

F. M. Morales, R. García, S. I. Molina, A. Aouni , P. A. Postigo, and C. G. Fonstad, "Micro-structural Improvements of InP on GaAs (001) grown by Molecular Beam Epitaxy by In-situ Hydrogenation and Post-growth Annealing," *Appl. Phys. Lett.*, in press.

Cheng, D. I., J. J. Rumpler II, J. M. Perkins, M. Zahn, C. G. Fonstad, Jr., E. S. Cramer, R. W. Zuneska, and F. J. Cadieu. "Use of Patterned Magnetic Films to Retain and Orient Micro-Components During Fluidic Assembly," *Journal of Applied Physics*, vol. 105, 07C123 (2009)

Rumpler, J. J., and C. G. Fonstad, "Continuous-Wave Electrically Pumped Ridge Laser on Silicon," *IEEE Photon Tech. Lett.*, in press.

Jongyoon Han
Associate Professor
Department of Electrical Engineering and Computer Science / Biological Engineering

COLLABORATORS
S. Tannenbaum, BE
S. Manalis, BE
M. Rubner, DMSE
R. Cohen, ChemE,
Tae-Song Kim, KIST, Korea
N. Hadjiconstantinou, MechE
Y. Chen, NUS, Singapore
N.-T. Nguyen, NTU, Singapore
C. T. Lim, NUS, Singapore
K. Van Vliet, MSE
S. Suresh, MSE

GRADUATE STUDENTS
P. Mao, Res. Asst., MechE
H. Bow, Res. Asst., EECS
P. Dextras, Res. Asst., BE
L. Li, Res. Asst., EECS / HST
L. F. Cheow, Res. Asst., EECS
A. Sarkar, Res. Asst., EECS

RESEARCH STAFF
Y. Song, Ph.D.
S. Kim, Ph.D.

SUPPORT STAFF
S. Davco, Admin. Asst.

Schoch, R.B., J. Han, and P. Renaud, Transport phenomena in nanofluidics. *Reviews of Modern Physics*, 80, 839-883, 2008.

Z. R. Li, G. R. Liu, Y. Z. Chen, J.-S. Wang, H. Bow, Y. Cheng, J. Han, "Continuum Transport Model of Ogston Sieving in Patterned Nanofilter Arrays for Rod-like Biomolecule Separation," *Electrophoresis*, 29, 329–339. 2008.

Y.-C. Wang and J. Han, "Pre-binding dynamic range and sensitivity enhancement for immuno-sensors using nanofluidic preconcentrator," *Lab on a Chip*, **8**, 392-394, 2008.

J. Lee, Y.-A. Song, J. Han, "Multiplexed Proteomic Sample Preconcentration Device Using Surface-Patterned Ion-Selective Membrane," *Lab on a Chip*, 8, 596-601, 2008.

S. J. Kim and J. Han, "Self-Sealed Vertical Polymeric Nanoporous-Junctions for High-Throughput Nanofluidic Applications," *Analytical Chemistry*, 80, 3507-3511, 2008.

S. Chung, J. H. Lee, M.-W. Moon, J. Han, R. D. Kamm, "Non-lithographic wrinkle nanochannels for protein preconcentration," *Advanced Materials*, 20, 3011-3016, 2008.

J. Hoon Lee, Y.-A. Song, S. R. Tannenbaum, J. Han, "Enhanced Reaction Kinetics and Sensitivity of Low-Abundance Enzyme Assay using Micro/Nanofluidic Preconcentration Chip," *Analytical Chemistry*, 80, 3198-3204, 2008.

Y.-A. Song, C. Batista, R. Sarpeshkar and J. Han, "In-plane integration of ion-selective membrane in microfluidic PEM fuel cell by micro flow surface patterning," *Journal of Power Sources*, 183, 674-677, 2008.

J. Fu, P. Mao, and J. Han, "Artificial molecular sieves and filters: a new paradigm for biomolecule separation," *Trends in Biotechnology* 26, 311-320, 2008

Duong-Hong, D., J. Han, J.-S. Wang, N. G. Hadjiconstantinou, Y. Z. Chen, and G.-R. Liu, "Realistic Simulations of Combined DNA Electrophoretic and Electroosmotic Flows in Nano-Fluidic Devices," *Electrophoresis*, 29, 4880-4886, 2008.

H. Bow, J. Fu, and J. Han, "Decreasing effective nanofilter size by modulating electrical double layers: Separation enhancement in microfabricated nanofilters," *Electrophoresis*, 29, 1-6, 2008.

P. Mao and J. Han, "Massively-Parallel Ultra-High-Aspect-Ratio Nanochannels as Mesoporous Membranes," *Lab on a Chip*, 9, 586-591, 2009.

Zi Rui Li, Gui Rong Liu, J. Han, Yu Zong Chen, Jian-Sheng Wang, N. Hadjiconstantinou, "Transport of biomolecules in asymmetric nanofilter arrays," *Analytical and Bioanalytical Chemistry*, accepted for publication (DOI: 10.1007/s00216-008-2558-y) (2009).

Y.-Ak Song and J. Han, "High-throughput Sample Preparation for Mass Spectrometry by Continuous-Flow pI-based Fractionation of Peptides and Proteins," (oral) *Proc. μTAS 2008 Symposium*, San Diego, CA, vol. 2, pp. 1323-1325, October 2008.

S. J. Kim and J. Han, "Self-Sealed Vertical Nanoporous Junctions for Integrating Various Nanomaterials in PDMS Microfluidic System," *Proc. μTAS 2008 Symposium*, San Diego, CA, vol. 2, pp. 1042-1044, October 2008.

S. J. Kim and J. Han, "Amplified Electrokinetic Fluid Pumping and Switching by Concentration Polarization Near Nanofluidic Channel," *Proc. μTAS 2008 Symposium*, San Diego, CA, vol. 1, pp. 197-199, October 2008.

H. Bow, P. Abgrall, and J. Han, "Microfabricated Slits in Series: A Simple Platform to Probe Differences in Cell Deformability," (poster), *Proc. μTAS 2008 Symposium*, San Diego, CA, vol. 2, pp.1199-120, October 2008.

Y.-A. Song, A. Sarkar, and J. Han, "Encapsulation of Biomolecules with Programmable Concentrations in Microdroplets using Electrokinetic Concentrator," *Proc. μTAS 2008 Symposium*, San Diego, CA, vol. 2, pp. 1420-1422, October 2008.

P. Mao and J. Han, "Fabrication of Massively-Parallel Regular Nanofluidic Filters for High-Throughput Biomolecule Separation," (poster), *Proc. μTAS 2008 Symposium*, San Diego, CA, vol. 1, pp. 853-855, October 2008.

Judy L. Hoyt
Professor
Department of Electrical Engineering and Computer Science

COLLABORATORS
D. Antoniadis, EECS
K. Berggren, EECS
F. Kartner, EECS
R. Ram, EECS
V. Stojanović, EECS
M. Canonico, ASU
T. Lyszczarz, Lincoln Labs
J. Yoon, Lincoln Labs

POSTDOCTORAL ASSOCIATE
H. S. Lee

GRADUATE STUDENTS
N. DiLello, EECS
L. Gomez, EECS
P. Hashemi, EECS
M. Kim, DMSE
J. Teherani, EECS

RESEARCH STAFF
G. Riggott, Research Specialist

SUPPORT STAFF
W. Rokui, Admin. Asst. II

P. Hashemi, L. Gomez, M. Canonico, and J.L. Hoyt, "Electron Transport in Gate-All-Around Uniaxial Tensile Strained-Si Nanowire n-MOSFETs," *IEEE IEDM*, Dec., 2008, pp.865-868.

C. Ni Chleirigh, N.D. Theodore, H. Fukuyama, S. Mure, H.-U. Ehrke, A. Domenicucci, and J. L. Hoyt, "Thickness Dependence of Hole Mobility in Ultrathin SiGe-Channel p-MOSFETs," IEEE Trans. Electron Devices, vol. 55, no. 10, Oct. 2008, pp. 2687 – 2694.

L. Gomez, P. Hashemi, and J.L. Hoyt, "Hole Velocity Enhancement in Sub-100nm Gate Length Strained-SiGe Channel p-MOSFETs on Insulator," IEEE SOI Conference, New Paltz, NY, USA, October 2008.

P. Hashemi, M. Canonico, J.K.W. Yang, L. Gomez, K.K. Berggren, and J. L. Hoyt, "Fabrication and Characterization of Suspended Uniaxial Tensile Strained-Si Nanowires for Gate-All-Around n-MOSFETs," ECS (Electrochemical Society) Transactions, vol. 16, No. 10, p.p. 57-68, October 2008.

Meekyung Kim, Oluwamuyiwa Olubuyide, Jung Yoon, and Judy Hoyt, "Selective Epitaxial Growth of Ge-on-Si for Photodiode Applications," ECS (Electrochemical Society) Transactions, vol. 16, No. 10, pp. 837-847, October 2008.

J.L. Hoyt, P. Hashemi, and L. Gomez, "Prospects for Top-Down Fabricated Uniaxial Strained Nanowire MOSFETs, " in ECS Transactions , vol. 16, No. 10, p.p. 731-734, October 2008.

O.M. Nayfeh, C. Ni Chleirigh, J. Hennessy, L. Gomez, J.L. Hoyt and D.A. Antoniadis, "Design of tunneling field-effect transistors using strained-silicon/strained-germanium type-II staggered heterojunctions," IEEE Electron Device Letters, v 29, n 9, Sept. 2008, p 1074-7.

O.M. Nayfeh, C. Ni Chleirigh, J.L. Hoyt and D.A. Antoniadis, "Measurement of enhanced gate-controlled band-to-band tunneling in highly strained silicon-germanium diodes," IEEE Electron Device Letters, v 29, n 5, May 2008, p 468-70.

C. Ni Chleirigh, XiaoRu Wang, G. Rimple, Yun Wang, N.D. Theodore, M. Canonico, and J.L. Hoyt, "Super critical thickness SiGe-channel heterostructure p-type metal-oxide-semiconductor field-effect transistors using laser spike annealing," Journal of Applied Physics, v 103, n 10, 15 May 2008, p 104501-1-4.

P. Hashemi, L. Gomez, M. Canonico, and J.L. Hoyt "Performance Enhancement in Uniaxially Tensile Strained-Si Gate-All-Around Nanowire n-MOSFETs," presented at IEEE Device Research Conference (DRC 2008), Santa Barbara, CA, USA, p. 185, June 2008.

L. Gomez, M. Canonico, M.K. Kim, P. Hashemi , and J.L. Hoyt, "Fabrication of Strained-Si/Strained-Ge Heterostructures on Insulator," Journal of Electronic Materials, vol. 37, No. 3, pp. 240-244, March 2008.L. Gomez, M. Canonico, M. Kim, P. Hashsmi, and J.L. Hoyt, Fabrication of Strained-Si/Strained-Ge Heterostructures on Insulator, J. Electronic Matl., 38 (3), p. 240, Feb. 2008.

P. Hashemi, L. Gomez, J.L. Hoyt, M.D. Robertson, M. Canonico, "Asymmetric strain in nano-scale patterned strained-Si/strained-Ge/strained-Si heterostructures on insulator," Applied Physics Letters, vol. 91, 083109, Aug. 2007.

L. Gomez, I. Aberg, and J.L. Hoyt, "Electron Transport in Strained-Silicon Directly onInsulator Ultrathin-Body n-MOSFETs With Body Thickness Ranging From 2 to 25 nm," IEEE EDL 28 (4), p. 285, April, 2007.

Guangrui (Maggie) Xia, Judy L. Hoyt and Michael Canonico, "Si-Ge interdiffusion in strained Si/strained SiGe heterostructures and implications for enhanced mobility metal-oxide-semiconductor field-effect transistors," Journal of Applied Physics, vol. 101, p. 044901 (2007)

T. Barwicz, H. Byun, F. Gan, C.W. Holzwarth, M.A. Popovic, P.T. Rakich, M.R. Watts, E.P. Ippen, F.X. Kartner, H.I. Smith, J.S. Orcutt, R.J. Ram, V. Stojanović, O.O. Olubuyide, J.L. Hoyt, S. Spector, M. Geis, M. Grein, T. Lyszczarz, J.U. Yoon, "Silicon photonics for compact, energy-efficient interconnects," Journal of Optical Networking, v 6, n 1, p. 63-73 (Jan. 2007).

Guangrui (Maggie) Xia, Michael Canonico, and Judy L. Hoyt, "Interdiffusion in strained Si/strained SiGe epitaxial heterostructures," Semicond. Sci. Technol. 22, pp. S55-S58, Nov. 2006.

Qing Hu
Professor
Department of Electrical Engineering and Computer Science

COLLABORATORS
J. L. Reno, Sandia National Lab.
D. Ban, University of Waterloo

POSTDOCTORAL ASSOCIATE
S. Kumar, RLE

GRADUATE STUDENTS
D. Burghoff, Res. Asst., EECS
I. Chan, Res. Asst., EECS
T.g-Y. Kao, Res. Asst., EECS
A. Lee, Res. Asst., EECS
Q. Qin, Res. Asst., EECS
A. Hsu, Res. Asst., EECS

SUPPORT STAFF
C. Bourgeois, Admin. Asst.

B. S. Williams, S. Kumar, Q. Hu, and J. L. Reno, "High-power terahertz quantum-cascade lasers," Elect. Lett. 42, 89 (2006). Also reported in Compound Semiconductor, page 32, March (2006).

S. Kumar, B. S. Williams, Q. Hu, and J. L. Reno, "1.9-THz quantum-cascade lasers with one-well injector," Appl. Phys. Lett. 88, 121123 (2006).

E. E. Orlova, J. N. Hovenier, T. O. Klaassen, I. Kasalynas, A. J. L. Adam, A. Baryshev, J. R. Gao, T. M. Klapwijk, B. S. Williams, S. Kumar, Q. Hu, and J. L. Reno, "Antenna Model for Wire Lasers," Phys. Rev. Lett. 96, 173904 (2006). Also published in the May 29, 2006 issue of Virtual Journal of Nanoscale Science & Technology.

A. J.L. Adam, I. Kašalynas, J.N. Hovenier, T.O. Klaassen, J.R. Gao, E.E. Orlova, B.S. Williams, S. Kumar, Q. Hu, and J. L. Reno, "Beam pattern of Terahertz quantum cascade lasers with sub-wavelength cavity dimensions," Appl. Phys. Lett. 88, 151105 (2006). Also published in Virtual Journal of Nanoscale Science & Technology, 13(16), April 26 (2006).

S. Kumar, B. S. Williams, Q. Hu, and J. L. Reno, "1.9-THz quantum-cascade lasers with one-well injector," Appl. Phys. Lett. 88, 121123 (2006).H. C. Liu, H. Luo, D. Ban, M. Wächter, C. Y. Song, Z. R. Wasilewski, M. Buchanan, G. C. Aers, A. J. Spring Thorpe, J. C. Cao, S. L. Feng, B. S. Williams, and Q. Hu, "Terahertz Semiconductor Quantum Well Devices," Proc. of SPIE, 6029, 602901 (2005).

Alan W.M. Lee, Benjamin S. Williams, Sushil Kumar, Qing Hu, and John L. Reno, "Real-Time Imaging using a 4.3-THz Quantum Cascade Laser and a 320´240 Microbolometer Focal-Plane Array," IEEE Photonics Technology Letters 18, 1415 (2006).

A. Baryshev, J. N. Hovenier, A. J. L. Adam, I. Kasalynas, J. R. Gao, T. O. Klaassen, B. S. Williams, S. Kumar, Q. Hu, and J. L. Reno, "Phase locking and spectral linewidth of a two-mode terahertz quantum cascade laser," Appl. Phys. Lett. 89, 031115 (2006).

B. S. Williams, S. Kumar, Q. Qin, Q. Hu, and J. L. Reno, "Terahertz quantum cascade lasers with double resonant-phonon depopulation," Appl. Phys. Lett. 88, 261101 (2006).

Alan W.M. Lee, Qi Qin, Sushil Kumar, Benjamin S. Williams, Qing Hu, and John L. Reno, 'Real-Time Terahertz Imaging over a Standoff Distance (>25 meters)," Appl. Phys. Lett. 89, 141125 (2006).

Sushil Kumar, B. S. Williams, Q. Qin, A. W. M. Lee, Q. Hu, and J. L. Reno, "Surface-emitting distributed feedback terahertz quantum-cascade lasers in metal-metal waveguides," Optics Express, 15, 113-128 (2007).

Alan Wei Min Lee, Qi Qin, Sushil Kumar, Benjamin S. Williams, Qing Hu, John L. Reno, "High-power and high-temperature THz quantum-cascade lasers based on lens-coupled metal-metal waveguides," submitted to Optics Letters (2007).

Pablo Jarillo-Herrero
Professor
Department of Physics

COLLABORATORS
J. Kong

POSTDOCTORAL FELLOWS
M. Zaffalon

GRADUATE STUDENTS
B. Baugher
J. Sanchez-Yamagishi
T. Taychatanapat
J.n Wang
L. Campos

SUPPORT STAFF
M. Wolf, Admin. Asst.

B. Özyilmaz, P. Jarillo-Herrero, D. Efetov and P. Kim,"Electronic Transport in Locally Gated Graphene Nanoconstrictions," *Appl. Phys. Lett.* 91, 192107 (2007).

B. Özyilmaz, P. Jarillo-Herrero, D. Efetov, D.A. Abanin, L.S. Levitov and P. Kim, "Electronic Transport and Quantum Hall Effect in Bipolar Graphene p-n-p Junctions," *Phys. Rev. Lett.* 99, 166804 (2007).

H.B. Heersche, P. Jarillo-Herrero, J.B. Oostinga, L.M.K. Vandersypen and A. Morpurgo, "Manifestations of phase-coherent transport in graphene - The Josephson effect, weak localization, and aperiodic conductance fluctuations," *European Physical Journal-Special Topics* 148, 27 (2007).

H.B. Heersche, P. Jarillo-Herrero, J.B. Oostinga, L.M.K. Vandersypen and A. Morpurgo, "Induced superconductivity in graphene," *Solid State Communications* 143, 72 (2007).

H.B. Heersche*, P. Jarillo-Herrero*, J.B. Oostinga, L.M.K. Vandersypen and A. Morpurgo, "Bipolar supercurrent in graphene," *Equal contribution. *Nature* 446, 56 (2007).

S. Sapmaz, P. Jarillo-Herrero, L.P. Kouwenhoven and H.S.J. van der Zant, "Quantum dots in carbon nanotubes," *Semiconductor Science and Technology* 21, s52 (2006) (Focus issue on Charge transport in carbon nanotubes)

S. Sapmaz, C. Meyer, P. Beliczynski, P. Jarillo-Herrero and Leo P. Kouwenhoven, "Excited state spectroscopy in carbon nanotube double quantum dots," *Nano Letters* 6, 1350 (2006) (featured in the cover).

P. Jarillo-Herrero, J.A. van Dam and L.P. Kouwenhoven, "Quantum supercurrent transistors in carbon nanotubes," *Nature* 439, 953 (2006).

S. Sapmaz, P. Jarillo-Herrero, Ya.M. Blanter, C. Dekker and H.S.J. van der Zant, "Tunneling in suspended carbon nanotubes assisted by longitudinal phonons," *Phys. Rev. Lett.* 96, 026801 (2006).

S. Sapmaz, P. Jarillo-Herrero, Ya.M. Blanter and H.S.J. van der Zant, "Coupling between electronic transport and longitudinal phonons in suspended nanotubes," *New Journal of Physics* 7, 243 (2005), (Focus issue on Nano-ElectroMechanical Systems).

P. Jarillo-Herrero, J. Kong, H.S.J. van der Zant, C. Dekker, L.P. Kouwenhoven and S. De Franceschi. "Tunable Orbital Pseudospin and Multi-level Kondo Effect in Carbon Nanotubes," in *Proc. Int. Winterschool on Electronic Properties of Novel Materials* (2005).

P. Jarillo-Herrero, J. Kong, H.S.J. van der Zant, C. Dekker, L.P. Kouwenhoven and S. De Franceschi, "Electronic transport spectroscopy of carbon nanotubes in a magnetic field," P*hys. Rev. Lett.* 94, 156802 (2005).

S. Sapmaz, P. Jarillo-Herrero, J. Kong, C. Dekker, L.P. Kouwenhoven and H.S.J. van der Zant, "Electronic excitation spectrum of metallic carbon nanotubes," *Phys. Rev. B* 71, 153402 (2005).

P. Jarillo-Herrero, J. Kong, H.S.J. van der Zant, C. Dekker, L.P. Kouwenhoven and S. De Franceschi. "Orbital Kondo effect in carbon nanotubes," *Nature* 434, 484 (2005).

P. Jarillo-Herrero, S. Sapmaz, C. Dekker, L.P. Kouwenhoven and H.S.J. van der Zant, "A few electron-hole semiconductor carbon nanotube quantum dot," in *Proc. International Winterschool on Electronic Properties of Novel Materials* 583 (2004).

P. Jarillo-Herrero, S. Sapmaz, C. Dekker, L.P. Kouwenhoven and H.S.J. van der Zant, "Electron-hole symmetry in a semiconducting carbon nanotube quantum dot," *Nature* 429, 389 (2004).

Sang-Gook Kim
Associate Professor
Department of Mechanical Engineering

COLLABORATORS
H. Asada, MechE
G. Barbastathis, MechE
G. Chen, MechE
V. Bulović, EECS
A. P. Chandrakasan, EECS
G. Rutledge, ChE
M. A. Schmidt, EECS

GRADUATE STUDENTS
S. Kim, MechE
S. Bathurst, MechE
A. Hajati, EECS
N. Reticker-Flynn, MechE
J. Peck, MechE/TPP
H. Lee, MechE
Dr. H. Lee, Research Associate
Dr. M. de Volder, Visiting Engineer
Dr. M. Schlipf, Visiting Engineer

SUPPORT STAFF
R. Hardin, Admin. Asst.

S. G. Kim, Z. Traina and H. Lee, "Folding Assembly of Microactuators," *CIRP Annals -Manufacturing Technology*, vol. 57, 2008

H.J. In, H. W. Lee, S. G. Kim, and G. Barbastathis, "Carbon nanotube based magnetic actuation of origami membranes," *Journal of Vacuum Science and Technology B*, vol. 26, no. 6, pp. 2509-2512, 2008

S. Bathurst, H.W. Lee and S.G. Kim, "Direct Printing of Lead Zirconate Titanate Thin Films," *IEEE MEMS 2008*, Tucson, AZ, 2008

A. Hajati and S. G. Kim, "Rectifierless Piezoelectric Micro Power Generator," *SPIE Smart Structures and Materials & Nondestructive Evaluation and Health Monitoring 2008,* San Diego, CA, 2008

A. Hajati and S. G. Kim, Energy Harvesting Piezoelectric MEMS Devices for Self-Supportive Wireless Sensors, Proceedings of Innovation Conference NSF Engineering Research, Knoxville, Tennessee, 2008

S. G. Kim, "Complexity of Assembly at Micro and Nano Scales: Axiomatic Approach," *SAE World Congress 2008* (invited), Chicago 2008

S. Bathurst, J. Jeon, H.W. Lee and S. G. Kim, "PZT MEMS by Thermal Ink Jet Printing," *Solid-State Sensor and Actuator Workshop*, Hilton Head, SC, 2008

H. J. In, A .J. Nichol, H. W. Lee, S. G. Kim, G. Barbastathis, "Carbon Nanotube-Based Magnetic Actuation of Origami Membranes," *Proc. International Conference on Electron, Ion and Photon Beam Technology and Nanofabrication*, Portland, OR, 2008

J. Peck and S.G. Kim, "Improving Emergency Department Patient Flow through Optimal Fast Track Usage," *ACEP Research Forum,* American College of Emergency Physicians Scientific Assembly, Chicago, IL, 2008

Bathurst, S., Jeon, J. Lee, H.W. and S.-G. Kim, "Ink Jet Printing of PZT Thinfilms for MEMS Applications," presented at *Digital Fabrication*, Pittsburgh, PA, 2008.

S. H. Kim, H. W. Lee and S.-G. Kim, " Deterministic Transplanting Assembly of Individual Carbon Nanotubes to MEMS Cantilevers," in *Proc. μTAS 2008 Symposium*, San Diego, CA, 2008

N. Reticker-Flynn, H. W. Lee and S.-G. Kim, "Printing of Temperature Sensitive Hydrogel for Compact Microfluidic Valves," in *Proc. μTAS 2008 Symposium*, San Diego, CA, 2008

H. W. Lee, S. H. Kim and S.-G. Kim, "Effective Parameters For Growing Vertically-Aligned Individual Freestanding Carbon Nanotubes/Nanofibers (CNs) using Plasma Enhanced Chemical Vapor Deposition (PECVD)," *Mater. Res. Soc. Symp. Proc.* Boston, MA, 2008

S. H. Kim, H. W. Lee and S.-G. Kim, "Double Polymeric Layer Encapsulation Process for Transplanting Assembly of Carbon Nanotubes into MEMS," *Mater. Res. Soc. Symp. Proc.* Boston, MA, 2008

H. W. Lee, H. J. In, G. Barbastathis, and S-G Kim, "Growth of Single Strand Carbon Nanotube Arrays on Foldable Titanium Nitride Membranes," *Mater. Res. Soc. Symp. Proc.* Boston, MA, 2008

H. J. In, H. W. Lee, and S-G Kim, G. Barbastathis, "Nano-manufacturing of Carbon Nanotubes on Titanium Nitride," *6th International Symposium on Nanomanufacturing*, Athens, Greece, Nov. 12-14, 2008

S. H. Kim, H. W. Lee and S.G. Kim, "Integration of Carbon Nanotubes into MEMS Devices via Deterministic Transplanting," *IEEE MEMS 2009,* Sorrento, Italy, 2009

S. Bathurst and S.-G. Kim, "Designing Direct Printing Process for Improved Piezoelectric Micro Devices," *Annals of the CIRP (Int'l Academy for Production Engineering)*, vol. 58, 2009

J. Peck, S-G. Kim, "Improving Patient Flow Through Axiomatic Design of Hospital Emergency Departments," *Proc. CIRP Design Conference,* Cranfield, UK, 2009

S. Bathurst, H.W. Lee, and S.G. Kim, "Design Against The Coupled Nature Of PZT Spin Coating," *Proc. 5th International Conference on Axiomatic Design,* Portugal, 2009

J. Peck, E. Kolb, T. Lee and S.G. Kim, "Lessons Learned by Applying Axiomatic Design to an Emergency Department," P*roc. 5th International Conference on Axiomatic Design,* Portugal 2009

H. J. In, H. W. Lee, and S-G Kim, G. Barbastathis, "Nano-manufacturing of Carbon Nanotubes on Titanium Nitride," *Int. J. of Nanomanufacturing,* 2009, accepted for publication

S. H. Kim, H. W. Lee and S.G. Kim, "Assembly of Individual Nanostructures to Micro Devices," *Proc. 6th Annual Conference on Foundations of Nano Science: Self-Sssembled Architectures and Devices,* Snowbird, Utah, 2009

S. Kim, H.W. Lee and S-G. Kim, "Transplanting Assembly of CNT-tipped AFM Probes," accepted to *Applied Physics Letters*, 2009

Sang-Gook Kim, *Multi-scale Assembly: Design, Processes and Complexity, In; Nanomanufacturing*, S. Chen, Ed., American Scientific Publishers, to be published.

Lionel C. Kimerling
Professor
Department of Materials Science and Engineering

COLLABORATORS
A.M. Agarwal, MIT-MPC
J. Michel, MIT-MPC
A. Eshed, MIT-MPC
X. Duan, MIT-MPC
R. Soref, USAF AFRL
M. Beals, MIT-MPC
D. Okamoto, NEC
Kazumi Wada, Univ. of Tokyo
H. Atwater, CalTech
M. Lipson, Cornell Univ.
M. Brongersma, Stanford Univ.
P. Fauchet, U. of Rochester
T.L. Koch, Lehigh Univ.
D. Prather, Univ. of Delaware
L. Dal Negro, Boston Univ.
K. Richardson, Clemson U.

POSTDOCTORAL ASSOCIATES
J. Liu, MIT-MPC

GRADUATE STUDENTS
R. Camacho-Aguilera, Res. Asst., DMSE
J. Cheng, Res. Asst., DMSE
L. Chiao, Sp. Student, DMSE
J. Hu, Res. Asst., DMSE
K. McComber, Res. Asst., DMSE
V. Ragunathan, Res. Asst., DMSE
X. Sheng, Res. Asst., DMSE
M. Vanhoutte, Res. Asst., DMSE
B. Wang, Res. Asst., DMSE
J. Wang, Res. Asst., DMSE
T. Zens, Res. Asst., DMSE

SUPPORT STAFF
L.A. Page, Admin. Asst. II

R. Sun,, K. McComber, J. Cheng, D.K. Sparacin, M. Beals, J. Michel, L.C. Kimerling, "Transparent amorphous silicon channel waveguides with silicon nitride intercladding layer," Applied Physics Letters **94**: 141108 (2009).

S. Saini, C.Y. Hong, S. Bernardis, N. Pfaff, L.C. Kimerling, J. Michel, "Hybrid waveguides for optically pumped amplifiers," Applied Physics Letters 94:091117 (2009).

Jifeng Liu and Jurgen Michel, "High Performance Ge Devices for Electronic-Photonic Integrated Circuits " ECS Transactions **16**: 575 (2008).

L. Zeng, P. Bermel, Y. Yi, B. A. Alamariu, K. A. Broderick, J. Liu, C. Hong, X. Duan, J. Joannopoulos, L.C. Kimerling, "Demonstration of enhanced absorption in thin film Si solar cells with textured photonic crystal back reflector," Applied Physics Letters **93**:221105 (2008).

J. Hu, V. Tarasov, N. Carlie, L. Petit, A. Agarwal, K. Richardson, L.C. Kimerling, "Exploration of waveguide fabrication from thermally evaporated Ge-Sb-S glass films," Optics Express **30** (10):1560-1566 (2008).

J. Hu, N. Carlie, N.N. Feng, L. Petit, A. Agarwal, K. Richardson, L.C. Kimerling, "Planar waveguide-coupled, high-index-contrast, high-Q resonators in chalcogenide glass for sensing, Optics Letters **33**:2500 (2008)

J. Wang, J. Hu, X. Sun, A. Agarwal, D. Lim, R. Synowicki, and L. Kimerling, "Structural, electrical and optical properties of thermally evaporated nanocrystalline PbTe films," Journal of Applied Physics **104**: 053707 (2008).

J. Hu, N. Carlie, L. Petit, A. Agarwal, K. Richardson, and L.C. Kimerling, "Demonstration of chalcogenide glass racetrack micro-resonators," Optics Letters **33**:761 (2008).

J. F. Liu, M. Beals, A. Pomerene, S. Bernardis, R. Sun, J. Cheng, L. C. Kimerling and J. Michel, "Waveguide-integrated, ultra-low energy GeSi electro-absorption modulators" Nature Photonics **2**, 433 (2008)

T. Anderson, L. Petit, N. Carlie, J. Choi, J. Hu, A. Agarwal, L.C. Kimerling, K. Richardson, M. Richardson, "Femtosecond laser photo-response of Ge23Sb7S70 films," Optics Express **16**: 20081 (2008).

R. Sun, L. Wang, J. Cheng, L. C. Kimerling, M. Balseanu, L.-Q. Xia, and H. M'saad, "Theoretical modeling on hydrogen evolution in Ultraviolet light-treated hydrogenated silicon nitride," Journal of Applied Physics, **104**:094103 (2008).

R. Sun, M. Beals, A. Pomerene, J. Cheng, C.Y. Hong, L.C. Kimerling, and J. Michel, "Impedance matching vertical optical waveguide couplers for dense high index contrast circuits," Optics Express **16**:11682-11690 (2008).

J. Hiltunen, D. Seneviratne, R. Sun, M. Stolfi, H. L. Tuller, J. Lappalainen, and V. Lantto, "Optical properties of BaTiO3 thin films: Influence of oxygen pressure utilized during pulsed laser deposition," Journal of Electroceramics, DOI 10.1007/s10832-008-9463-9, published online March 7, 2008.

W.N. Ye, J. Michel, L.C. Kimerling, "Athermal High-Index-Contrast Waveguide Design," Photonics Technology Letters, IEEE **20** (11): 885-887 (June 1, 2008).

V. Sorianello, A. Perna, L. Colace, G. Assanto, H.C. Luan, L.C. Kimerling, "Near-infrared absorption of germanium thin films on silicon," Applied Physics Letters **93** (11):111115 (Sept. 15, 2008).

S. Saini, C.Y. Hong, N. Pfaff, L. C. Kimerling, and J. Michel, "Partial confinement photonic crystal waveguides," Applied Physics Letters **93**, 261102 (2008).

Leslie A. Kolodziejski
Professor
Department of Electrical Engineering and Computer Science

COLLABORATORS
E.P. Ippen, MIT
J.D. Joannopoulus, MIT
F.X. Kaertner, MIT
R. Ram, MIT
M. Soljacic, MIT
J. Wang, MIT Lincoln Labs
Hamad Albrithen, KACST
Abdelmajid AlSalhi, KACST

RESEARCH STAFF
G. Petrich, Principal Research Scientist

GRADUATE STUDENTS
M. Araghchini, Res. Asst., EECS
R. Bryant, Res. Asst., EECS
P. Chu, Res. Asst., DMSE
S. Nabanja, Res. Asst., EECS
O. Shamir, Res. Asst., EECS
T. Shih, Res. Asst., EECS

SUPPORT STAFF
D. Stewart, Admin. Asst.

T.-M. Shih, A. Kurs, M. Dahlem, G. S. Petrich, M. Soljacic, E.P . Ippen, L. A. Kolodziejski, K. Hall, and M. Kesler, "Supercollimation in Photonic Crystals Composed of Silicon Rods" *Appl. Phys. Lett.*, vol. 93, no. 13, p. 131111 (2008).

T.-M. Shih, A. Kurs, M. Dahlem, G. S. Petrich, M. Soljacic, E. P. Ippen, L. A. Kolodziejski, K. Hall, and M. Kesler, "Supercollimation in Photonic Crystals Composed of Silicon Rods" *Virtual Journal of Nanoscale Science and Technology*, vol. 18, no. 16 (2008).

T.-M. Shih, M. Dahlem, A. Kurs, G.S. Petrich, M. Soljacic, E.P. Ippen, L.A. Kolodziejski, K. Hall, and M. Kesler, "Supercollimation in Photonic Crystals Composed of Nano-Scale Silicon Rods" *Lasers and Electro-Optics, 2008 and 2008 Conference on Quantum Electronics and Laser Science. CLEO/QELS 2008.* Conference on 4-9 May 2008 Page(s):1 - 2

D. Pudo, H. Byun, J.T. Gopinath, G.S. Petrich, E.P. Ippen, F.X. Kaertner, and L.A. Kolodziejski, "Nonlinear Phase Response of a Saturable Bragg Reflector for Modulation Depth Control" *Lasers and Electro-Optics, 2008 and 2008 Conference on Quantum Electronics and Laser Science.* CLEO/QELS 2008. Conference on 4-9 May 2008 Page(s):1 - 2

Jing Kong
Assistant Professor
Department of Electrical Engineering and Computer Science

COLLABORATORS
M. Dresselhaus, EECS
A. P. Chandrakasan, EECS
T. Palacios, EECS
P. Jarrillo-Herrero, Physics
F. Stellacci, DDMSE,
J. Zhang, Chemistry,
Peking University
Z.F.Liu, Chemistry,
Peking University

POSTDOCTORAL ASSOCIATES
J.K. Yuan

GRADUATE STUDENTS
H. Farhat, Res. Asst., DMSE
A. R. Cecco, Res. Asst., DMSE
D. A. Nezich, Res. Asst., Physics
K. J. Lee, Res. Asst., EECS
M. Hofmann, Res. Asst., EECS

SUPPORT STAFF
E. Moran, Admin. Asst

H. Farhat, H. Son, G.G. Samsonidze, S. Reich, M.S. Dresselhaus, and J. Kong, "Phonon softening in individual metallic carbon nanotubes due to the Kohn anomaly," *Physical Review Letters*, vol. 99, no. 14 , pp. 145506:1-4, Oct. 2007.

X.J. Duan, H.B. Son, B. Gao, J. Zhang, T.J. Wu, G.G. Samsonidze, M.S. Dresselhaus, Z.F. Liu, and J. Kong, "Resonant raman spectroscopy of individual strained single-wall carbon nanotubes," *Nano Letters*, vol. 7, no. 7, pp. 2116-2121, June 2007.

H. Son, G.G. Samsonidze, J. Kong, Y.Y. Zhang, X.J. Duan, J. Zhang, Z.F. Liu, and M.S. Dresselhaus, "Strain and friction induced by van der Waals interaction in individual single walled carbon nanotubes," *Applied Physics Letters*, vol. 90, no. 25, pp. 253113:1-3, June 2007.

A. Reina, M. Hofmann, D. Zhu, and J. Kong, "Growth mechanism of long and horizontally aligned carbon nanotubes by chemical vapor deposition," *Journal of Physical Chemistry C*, vol. 111, no. 20, pp. 7292-7297, May 2007.

Y.Y. Zhang, H. Son, J. Zhang, J. Kong, and Z.F. Liu, "Laser-heating effect on Raman spectra of individual suspended single-walled carbon nanotubes," *Journal of Physical Chemistry C*, vol. 111, no. 5, pp. 1988-1992, Jan. 2007.

Y.Y. Zhang, H. Son, J. Zhang, M.S. Dresselhaus, J. Kong, and Z.F. Liu, "Raman spectra variation of partially suspended individual single-walled carbon nanotubes,"*Journal of Physical Chemistry C*, vol. 111, no. 5, pp. 1983-1987, Jan. 2007.

S. Bhaviripudi, E. Mile, S. Steiner, A.T. Zare, M.S. Dresselhaus, A. Belcher, and J. Kong, "CVD synthesis of single-walled carbon nanotubes from gold nanoparticle catalysts," *Journal of the American Chemical Society,* vol. 129, pp. 1516-1517, Jan. 2007.

X. Zhang, K. Jiang, C. Feng, P. Liu, L. Zhang, J. Kong, T. Zhang, Q. Li, and S. Fan, "Spinning and processing continuous yarns from 4-inch wafer scale super-aligned carbon nanotubes arrays," *Advance Materials,* vol. 18, pp. 1505-1510, May 2006.

H.B. Son, A. Reina, M.S. Dresselhaus, and J. Kong, "Characterizing the chirality distribution of single-walled carbon nanotube materials with tunable Raman spectroscopy," *Physica Status Solidi (b),* vol. 243, no. 13, pp. 3161-3165, Oct. 2006.

S. Bhaviripudi, A. Reina, J. Qi, J. Kong, and A. Belcher, "Block-copolymer assisted synthesis of arrays of metal nanoparticales and their catalytic activities for the growth of SWNTs," *Nanotechnology,* vol. 17, pp. 5080-5086, Sept. 2006.

H. Son, A. Reina, G.G. Samsonidze, R. Saito, A. Jorio, M.S. Dresselhaus, and J. Kong, "Raman characterization of electronic transition energies of metallic single-wall carbon nanotubes," *Physical Review B,* vol. 74, p. 073406, Aug. 2006.

X. Zhang, K. Jiang, C. Feng, P. Liu, L. Zhang, J. Kong, T. Zhang, Q. Li, and S. Fan, "Spinning and processing continuous yarns from 4-inch wafer scale super-aligned carbon nanotubes arrays," *Advanced Materials,* vol. 18, pp. 1505-1510, May 2006.

F. Villalpando-Paez, A. Zamudio, A.L. Elias, H. Son, E.B. Barros, S.G. Chou, Y.A. Kim, H. Muramatsu, T. Hayashi, J. Kong, H. Terrones, G. Dresselhaus, M. Endo, M. Terrones, and M.S. Dresselhaus, "Synthesis and characterization of long strands of nitrogen-doped single-walled carbon nanotubes," *Chemical Physical Letters,* vol. 424, pp. 345-352, Apr. 2006.

J. Lu, T. Kopley, D. Dutton, J. Liu, C. Qian, H. Son, M.S. Dresselhaus, and J. Kong, "Generating suspended single-walled carbon nanotubes across a large surface area via patterning self-assembled catalyst-containing block copolymer thing films," *Journal of Physical Chemistry Letters B,* vol. 110, pp. 10585-10589, Apr. 2006.

Y.Y. Zhang, J. Zhang, H.B. Son, J. Kong, and Z.F. Liu, "Substrate-induced Raman frequency variation for single-walled carbon nanotubes," *Journal of the American Chemical Society*, vol. 127, no. 49, p. 17156, Dec. 2005.

B.J. LeRoy, J. Kong, V.K. Pahilwani, C. Dekker, and S.G. Lemay, "Three-terminal scanning tunneling spectroscopy of suspended carbon Nanotubes," *Physics Review B*, vol. 72, pp. 075413:1-5, Aug. 2005.

P. Jarillo-Herrero, J. Kong, H.S.J. van der Zant, C. Dekker, L.P. Kouwenhoven, and S. De Franceschi, "Electronic transport spectroscopy of carbon nanotubes in a magnetic field," *Physics Review Letters,* vol. 94, pp. 156802: 1-4, Apr. 2005

S. Sapmaz, P. Jarillo-Herrero, J. Kong, C. Dekker, L.P. Kouwenhoven, and H.S.J. van der Zant, "Excitation spectrum of metallic carbon nanotubes," *Physics Review B*, vol. 71, pp. 153402:1-4, Apr. 2005.

Jeffrey H. Lang
Professor
Department of Electrical Engineering and Computer Science

COLLABORATORS
A.I. Akinwande, MIT
M.G. Allen, Georgia Inst. of Tech.
J.G. Brisson, MIT
A.P. Chandrakasan, MIT
T. Daniel, University of WA
J.G. Hildebrand, University of AZ
F.S. Hover, MIT
A.H. Slocum, MIT
M.A. Schmidt, MIT
Z. S. Spakovszky, MIT
M.S. Triantafyllou, MIT
D.L. Trumper, MIT
J. Voldman, MIT
E.N. Wang, MIT
M. Zahn, MIT

GRADUATE STUDENTS
B. Cannon, EECS
S. Chang, EECS
V. Fernandez, MechE
S. Hou, EECS
D. Jenicek, EECS
Z. Trimble, MechE

SUPPORT STAFF
D. Bizi, Admin. Asst. I

V. I. Fernandez, S. M. Hou, F. S. Hover, J. H. Lang and M. S. Triantafyllou; "MEMS-array pressure sensing for underwater navigation," *Proc. Undersea Distributed Network Systems Conference,* Newport, RI, February 13-15, 2007.

J. W. Phinney, D. J. Perreault and J. H. Lang; "Radio-frequency inverters with transmission-line input networks," *IEEE Transactions on Power Electronics;* 22, 1154-1161, July 2007.

J. W. Phinney, D. J. Perreault and J. H. Lang; "Synthesis of lumped transmission-line analogs," *IEEE Transactions on Power Electronics*, 22, 1531-1542, July 2007.

V. I. Fernandez, S. M. Hou, F. S. Hover, J. H. Lang and M. S. Triantafyllou; "Lateral line inspired MEMS-array pressure sensing for passive underwater navigation," *Proc. Unmanned Untethered Submersible Technology Symposium*, Sensors Paper #4, Durham, NH, August 19-22,2007.

A. C. Weber, J. H. Lang and A. H. Slocum; "111 Si etched planar electrical contacts for power MEMS relays'," *Proc. 53rd IEEE Holm Conference on Electrical Contacts,* 156-159, Pittsburgh, PA, Sept 15-19, 2007.

H. Ma, J. H. Lang and A. H. Slocum; "Technique for measuring the dielectric constant of liquids and gases without the use of calibration standards," *Proc. μTAS 2008 Symposium*, 1692-1694, Paris, France, October 7-11, 2007.

H. Ma, J. H. Lang and A. H. Slocum; "Design of an electrochemical impedance test cell with servomechanically adjustable cell constant," *Proc. IEEE Sensors Conference,* 1233-1236, Atlanta, GA, October 28-31, 2007.

M. B. Read, A. H. Slocum, R. Martens, J. H. Lang, A. C. Weber and O. Yaglioglu; "A highly repeatable MEMS-based electrical contact test system," *Proc. Tenth International Conference of the European Society for Precision Engineering and Nanotechnology (EUSPEN 2008),* 389-393, Zurich, Switzerland, May 18-22, 2008.

A. C. Weber, J. H. Lang and A. H. Slocum; "A MEMS-relay for make-break power switching applications," *Proc. Solid-State Sensors, Actuators and Microsystems Workshop,* 52-53, Hilton Head Island, SC, June 1-5, 2008.

M. B. Read, A. C. Weber. O. Yaglioglu, R. Martens, J. H. Lang and A. H. Slocum, "Two-coupon system for the repeatable measurement of flat microscale contact resistance," P*roc. International Conference on Electrical Contacts,* 246-250, Saint-Malo, France, June 9-12, 2008.

H. Ma, J. H. Lang and A. H. Slocum; "Permittivity measurements using adjustable microscale electrode gaps between millimeter-sized spherical electrodes," *Review of Scientific Instruments,* 79, March 2008.

B. C. Yen, F. Herrault, M. G. Allen, F. F. Ehrich, K. J. Hillman, S. Jacobson, C. H. Ji, J. H. Lang, H. Li, Z. S. Spakovszky and D. R. Veazie; "Characterization of a fully-integrated permanent-magnet turbine generator," *Proc. 8TH International Workshop on Micro/Nano Technology for Power Generation and Energy Conversion Applications (Power MEMS),* 121-124, Sendai, Japan, November 9-12, 2008.

D. Golda, J. H. Lang and M. L. Culpepper; "Two-layer electroplated microcoils with a PECVD silicon dioxide interlayer dielectric," *IEEE/ASME Journal of Microelectromechanical Systems*, 17, 1537-1545, December 2008.

J. L. Steyn, S. H. Kendig, R. Khanna, S. D. Umans, J. H. Lang and C. Livermore; "A self-excited MEMS electroquasistatic induction turbine-generator," I*EEE/ ASME Journal of Microelectromechanical Systems,* 18, 424-432, April 2009.

H. Ma, J. H. Lang and A. H. Slocum; "Calibration-free measurement of permittivity and conductivity using electrochemical impedance test cell with servomechanically adjustable cell constant," *IEEE Sensors Journal*, 2009, to be published.

Hae-Seung Lee

Professor, Director of Center for Integrated Circuits and Systems
Department of Electrical Engineering and Computer Science

GRADUATE STUDENTS
L. Brooks, Res. Asst., EECS
A. Chow, Res. Asst., EECS
J. Chu, Res. Asst., EECS
J. Feng, EECS
M. Guyton, Res. Asst., EECS
P. Lajevardi, Res. Asst., EECS
S. Lee, Res. Asst., EECS
M. Markova, Res. Asst., EECS

SUPPORT STAFF
C. Collins, Assistant to Director of Center for Integrated Circuits and Systems

H.-S. Lee, "Comparator and Zero-Crossing Based ADC's: Challenges and Possible Solutions," *ISSCC Special Evening Topics Session*, San Francisco, CA, Feb. 2008.

H.-S. Lee and C. G. Sodini, "Mixed-Signal Integrated Circuits-Digitizing the Analog World," *Proceedings of IEEE*, vol. 96, pp. 323-334, Feb. 2008.

S.-K. Shin, Y.-S. You, S.-H. Lee, K.-H. Moon, J.-W. Kim, L. Brooks., and H.-S. Lee, "A Fully-Differential Zero-Crossing-Based 1.2V 10b 26MS/s Pipelined ADC in 65nm CMOS," *Digest of Technical Papers, Symposium on VLSI Circuits,* Honolulu, HI, June 2008.

M-Y Choi, S-o Lee, S-B You, W-S Yeum, H-J Park, J-W Kim, and H-S Lee, "A 101-dB SNR Hybrid Delta-Sigma Audio ADC using Post Integration Time Control, " *Digest of Technical Papers, IEEE Custom Integrated Circuits Conference,* San Jose, September 2008.

T-H Oh, H-Y Lee, J-H Kim, H-J Park, K-H Moon, J-W Kim, and H-S Lee, "A 16b 10MS/s Digitally Self-Calibrated ADC with Time Constant Control, "*Digest of Technical Papers, IEEE Custom Integrated Circuits Conference*, San Jose, September 2008.

N. Sun, H-S Lee, and D. Ham, "Digital background calibration in pipelined ADCs using commutated feedback capacitor switching," *IEEE Trans. Circuits and Systems,* Sept. 2008.

L. Brooks and H.-S. Lee, "Background calibration of Pipelined ADCs Via Decision Boundary Gap Estimation," *IEEE Trans. Circuits and Systems*, Nov. 2008.

L. Brooks and H.-S. Lee, " A 12b, 50MS/s, Fully Differential Zero-Crossing Based ADC without CMFB," *Digest of Technical Papers IEEE ISSCC*, Feb. 2009.

T. Sepke, P. Holloway, C. G. Sodini, and H.-S. Lee, "Noise Analysis for Comparator-Based Circuits," *IEEE Trans. Circuits and Systems,* March, 2009.

Carol Livermore

Associate Professor
Department of Mechanical Engineering

COLLABORATORS
G. Barbastathis, MIT
T. Havel, MIT
L. Velasquez-Garcia, MIT

GRADUATE STUDENTS
G. Agarwal, Res. Asst., MechE
F. Eid, Res. Asst., MechE
F. Hill, Res. Asst., MechE
N. Shaar, Res. Asst., MechE

SUPPORT STAFF
N. Weaver, Admin. Asst.

Agarwal, G., A. Servi, F. Eid, and C. Livermore, "Shape-selective Assembly of Deformable Systems using Templated Assembly by Selective Removal," *6th Annual Conference on the Foundations of Nanoscience*, Snowbird, UT, April 2009.

Steyn, J.L., S.H. Kendig, R. Khanna, S.D. Umans, J.H. Lang, and C. Livermore, "A Self-Excited MEMS ElectroQuasiStatic Induction Turbine-Generator," *Journal of Microelectromechanical Systems* 18, 424-432, April 2009.

Shaar, N., G. Barbastathis, and C. Livermore, "Controlled latching of microplates for 3D MEMS assembly," International Conference and Exhibition on Device Packaging, Scottsdale, AZ, March 2009.

Hill, F.A., T. Havel, A. John Hart, and C. Livermore, "Storing Elastic Energy in Carbon Nanotubes," presented at *Power MEMS 2008*, Sendai, Japan, November 2008.

Wilhite, B.A., T.F. Hill, L.F. Velasquez-Garcia, A.H. Epstein, K.F. Jensen, and C. Livermore, "Design of a Silicon-Based Microscale Trickle-Bed System for Singlet-Oxygen Production," *American Institute of Chemical Engineers Journal* 54, 2441-2455, September 2008.

Eid, F., S. Jung, and C. Livermore, "Templated assembly by selective removal (TASR): Simultaneous, selective assembly and model verification," *Nanotechnology* 19, 285602 (8 pp.), July 2008.

Shaar, N., G. Barbastathis, and C. Livermore, "Cascaded Mechanical Alignment for Assembling 3D MEMS," in P*roc. 18th IEEE International Conference on Micro Electro Mechanical Systems*, Tuscon, AZ, January 2008.

Velásquez-García, L.F., T.F. Hill, B.A. Wilhite, K.F. Jensen, A.H. Epstein, and C. Livermore, "A MEMS Singlet Oxygen Generator – Part I: Device Fabrication and Proof of Concept Demonstration," *IEEE Journal of Microelectromechanical Systems* 16 (6), 1482-1491, December 2007.

Hill, T.F., L.F. Velásquez-García, B.A. Wilhite, W.T. Rawlins, S. Lee, S.J. Davis, K.F. Jensen, A.H. Epstein, and C. Livermore, "A MEMS Singlet Oxygen Generator – Part II: Experimental Exploration of the Performance Space," *IEEE Journal of Microelectromechanical Systems* 16 (6), 1492-1505, December 2007.

Hill, F.A., T.F. Havel, and C. Livermore, "A Portable Power Source Based on MEMS and Carbon Nanotubes," *Proceedings of IMECE 2007*, Seattle, WA, November 2007.

Velasquez-Garcia, L.F., T.F. Hill, B.A. Wilhite, K.F. Jensen, A.H. Epstein, and C. Livermore, "A MEMS Singlet Oxygen Generator for a MEMS Chemical Oxygen Iodine Laser," P*roceedings of Power MEMS 2006,* Berkeley, CA, 117-120, November 2006.

Hill, T.F., B.A. Wilhite, L.F. Velasquez-Garcia, A.H. Epstein, K.F. Jensen, and C. Livermore, "A MEMS Singlet Oxygen Generator," S*olid State Sensor, Actuator, and Microsystems Workshop*, Hilton Head Island, SC, June 2006.

Jung, S. and C. Livermore, "Achieving Selective Assembly with Template Topography and Ultrasonically Induced Fluid Forces," *Nano Letters* 5 (11), 2188-2194, November 2005.

Nagle, S.F., C. Livermore, L.G. Frechette, R. Ghodssi, and J.H. Lang, "An Electric Induction Micromotor," *IEEE Journal of Microelectromechanical Systems* 14 (5), 1127-1143, October 2005.

Steyn, J.L., S.H. Kendig, R. Khanna, T.M. Lyszczarz, S.D. Umans, J.U. Yoon, C. Livermore, and J.H. Lang, "Generating Electric Power with a MEMS Electroquasistatic Induction Turbine-Generator," *MEMS 2005*, Miami, FL, January 2005.

Wilhite, B.A., C. Livermore, Y. Gong, A.H. Epstein, and K.F. Jensen, "Design of a MEMS-Based MicroChemical Oxygen Iodine Laser System," *IEEE Journal of Quantum Electronics* 40 (8), 1041-1055, August 2004.

Livermore, C., A. Forte, T. Lyszczarz, S.D. Umans, A.A. Ayon, and J.H. Lang, "A High-Power MEMS Electric Induction Micromotor," *IEEE Journal of Microelectromechanical Systems* 13 (3), 465-471, June 2004.

Livermore, C., A. Forte, T. Lyszczarz, S.D. Umans, and J. Lang, "Microscale Electric Induction Machines for Power Applications," *Proc. Electrostatics 2003*, Edinburgh, Scotland, 45-52, March 2003.

Scott R. Manalis
Professor
Department of Biological and Mechanical Engineering

COLLABORATORS
A. Amon, MIT
A. Belcher, MIT
T. Burg, MPI
J. Han, MIT
J. Foster, IMT
A. Grossman, MIT
D. Schauer, MIT
S. Jiang, Univ of Washington
M. Kirschner, Harvard
M. Lang, MIT
P. Mallick, UCLA
T. Squires, UCSB
V. Mootha, Harvard

POSTDOCTORAL ASSOCIATES
W. Grover, BE
S. Knudsen, BE
J. Lee, BE
D. Nida, BE

GRADUATE STUDENTS
A. Bryan, BE
R. Chunara, HST, EECS
F. Delgado, BE
P. Dextras, BE
A. Gulati, BE
M. von Muhlen, BE
S. Son, MechE
Y.C. Weng, BE

SUPPORT STAFF
M. Tangney

P. Dextras, T.P. Burg, S.R. Manalis, "Integrated Measurement of the Mass and Surface Charge of Discrete Microparticles Using a Suspended Microchannel Resonator," submitted

T.P. Burg, J.E. Sader, S.R. Manalis"Non-Monotonic Energy Dissipation in Microfluidic Resonators," submitted

S.M. Knudsen, M.G. von Muhlen, D.B. Schauer, S.R. Manalis, "Determination of Bacterial Antibiotic Resistance Based on Osmotic Shock Response," submitted.

A. K. Bryan, A. Goranov, A. Amon, S. R. Manalis, "Measurement of mass, density, and volume of yeast through the cell cycle," submitted.

S. Son, W.H. Grover, T.P. Burg, S.R. Manalis. Suspended microchannel resonators for ultra-low volume universal detection. *Analytical Chemistry*. 2008; 80 4757-4760.

W.H. Grover, M. von Muhlen, S.R. Manalis. Teflon films for chemically-inert microfluidic valves and pumps. *Lab on a Chip*. 2008; 8 913-918.

T.M. Squires, R.J. Messinger, S.R. Manalis. Making it stick: convection, reaction, and diffusion in surface based biosensors. *Nature Biotechnology.* 2008; 26 417-426.

R. Chunara, M. Godin, S. M. Knudsen, S.R. Manalis. Mass-based readout for agglutination assays. *Applied Physics Letters*. 2007; 91 193902.

M. Godin, A.K. Bryan, T. Burg, and S.R. Manalis, Measuring the mass, density and size of particles and cells using a suspended microchannel resonator. *Applied Physics Letters*. 2007; 91 123121.

T.P. Burg M.Godin, W. Shen, G. Carlson, J.S. Foster, K. Babcock, and S.R. Manalis. Weighing of Biomolecules, Single Cells, and Single Nanoparticles in Fluid. *Nature* 2007; 446 1066-1069

J. Hou, M. Godin, K. Payer, R. Chakrabarti, S.R. Manalis. Integrated Microelectronic Device for Label-free Nucleic Acid Amplification and Detection. *Lab on a Chip* 2007; 7 347-354.

Ichiro Masaki
Director
Intelligent Transportation Research Center

COLLABORATORS
J. F. Coughlin
B. K. P. Horn
H.-S. Lee
C. G. Sodini
J. M. Sussman

GRADUATE STUDENTS
Y. Fang, Res. Asst., EECS
B. Bilgic, Res. Asst., EECS

VISTING SCIENTISTS
T.H. Fang
S. Yokomitsu

SUPPORT STAFF
V. DiNardo, Admin. Asst. II

Yajun Fang, Sumio Yokomitsu, Berthold Horn, Ichiro Masaki, "A Layered-based Fusion-based Approach to Detect and Track the Movements of Pedestrians through Partially Occluded Situations." IEEE Intelligent Vehicles Symposium 2009 (IV2009).

Berthold Horn, Yajun Fang, Ichiro Masaki, "Hierarchical framework for direct gradient-based time-to-contact estimation." IEEE Intelligent Vehicles Symposium 2009 (IV2009).

Fang. Y., Horn. B.K.P., Masaki I., "Systematic information fusion methodology for static and dynamic obstacle detection in ITS." 15th World Congress On ITS, 2008.

Horn. B.K.P., Fang. Y., Masaki I., "Time to Contact Relative to a Planar Surface." Berthold Horn, Yajun Fang, Masaki. I., IEEE Intelligent Vehicles Symposium 2007 (IV2007).

Herrington, W.F., Jr., Horn. B. K. P. and Masaki. I., "Application of the Discrete Haar Wavelet Transform to Image Fusion for Nighttime Driving", IEEE Intelligent Vehicles Symposium 2005 (June 6-8, 2005),

Fang, Y., K. Yamada, Y. Ninomiya, B. Horn and Masaki. I., "A Shape-Independent-Method for Pedestrian Detection with Far Infrared-images." Special issue on "In-Vehicle Computer Vision Systems" of IEEE Transactions on Vehicular Technology, Vol.53, No.6, Nov. 2004, pp.1679-1697.

Fang, Y., K. Yamada, Y. Ninomiya, Horn. B. K. P. and Masaki. I., "Comparison between Infrared-image-based and Visible-image-based Approaches for Pedestrian Detection," IEEE Intelligent Vehicles Symposium 2003 (IV2003, pp.505-510). First Prize, Best Paper Award by IEEE ITS Council

Kato. T., Ninomiya. Y., Masaki. I., „An Obstacle Detection Method by Fusion of Radar and Motion Stereo." SICE Annual Conference in Fukui, August 4-6, 2003

Fang, Y., Masaki. I. and Horn. B. K. P., "Depth-Based Target Segmentation for Intelligent Vehicles: Fusion of Radar and Binocular Stereo," IEEE Transactions on Intelligent Transportation Systems, Vol.3, No.3, Sept. 2002, pp.196-202.

Kato. T., Ninomiya. Y., Masaki. I., „An Obstacle Detection Method by Fusion of Radar and Motion Stereo." IEEE Transactions on Intelligent Transportation Systems, Vol.3, No.3, Sep. 2002, pp.182-188.

Kato. T., Ninomiya. Y., Masaki. I., "Preceding vehicle recognition based on learning from sample images." IEEE Transactions on Intelligent Transportation Systems, Vol.3, No.4, Dec. 2002, pp.252-260.

Fang, Y., Masaki. I. and Horn. B. K. P., "Distance/Motion Based Segmentation under Heavy Background Noise," IEEE Intelligent Vehicles Symposium 2002 (IV2002, pp.483-488).

Fang, Y., Ninomiya. Y., Masaki. I., "Intelligent Transportation Systems, Challenges and Opportunities," The 2nd International Symposium on Multimedia Mediation Systems, 2002 (pp.72-77). Invited Paper

Fang, Y., Masaki. I. and Horn. B. K. P., "Distance Range Based Segmentation in Intelligent Transportation Systems: Fusion of Radar and Binocular Stereo," IEEE Intelligent Vehicles Symposium 2001 (IV2001, pp.171-176).

Yajun Fang, Marcelo Mizuki, Berthold Horn, Ichiro Masaki, "TV Camera-based Vehicle Motion Detection and its Chip Implementation." IEEE Intelligent Vehicles Symposium 2000 (IV2000, pp.134-139).

Tomás Palacios
Assistant Professor
Department of Electrical Engineering and Computer Science

COLLABORATORS
F. Calle, ETSIT-UPM, Spain
J. del Alamo, MIT
P. Jarillo-Herrero, MIT
D. Jena, University of Notre Dame
J. Kong, MIT
U. K. Mishra, Univ. California Santa Barbara
E. Monroy, CEA-Grenoble, France
E. Munoz, ETSIT-UPM, Spain
D. Perreault, MIT
H. Xing, Univ. Notre Dame

VISITING SCIENTIST
N. Dandrimont, France
M. Azize, Postdoc, France

VISITING STUDENT
F. Mieville, EPFL, Switzerland

GRADUATE STUDENTS
J. W. Chung, Res. Asst., EECS
F. Gao, Res. Asst., EECS
A. Hsu, Res. Asst., EECS
B. Lu, Res. Asst., EECS
A. Potter, Res. Asst., EECS
O. I. Saadat, Res. Asst., EECS
H. Wang, Res. Asst., EECS

UNDERGRADUATE STUDENTS
A. Huhn
D. Piedra
J. Wu

SUPPORT STAFF
E. Kubicki, Admin. Assistant II

Rajan S., U. K. Mishra, and T. Palacios , "AlGaN/GaN HEMTs: Recent Developments and Future Directions," *International Journal of High Speed Electronics* 18, 913-922, 2008.

Palacios T., " Beyond the AlGaN/GaN HEMT: New Concepts for High-Speed Transistors," in press, *physica status solidi (a)*, Sept. 2008 (invited contribution).

Palacios T., J. W. Chung, O. Saadat, and F. Mieville: " GaN and Digital Electronics: A Way out of Moore 's Law? ," in press, physica status solidi (a), Sept. 2008 (invited contribution).

Wang H., D. Nezich, J. Kong, and T. Palacios : " Graphene Frequency Multipliers," Electron Device Letters, May, 2009.

Wang H. and T. Palacios , "Efficency of Graphene Nanoribbon RF Amplifiers: A Theoretical Analysis ," submitted to Electron Device Letters, Sept. 2008.

Chung J. W., Edwin L. Piner, and T. Palacios , " N-face GaN/AlGaN HEMTs Fabricated through Layer Transfer Technology ," Electron Device Letters 30, 113-116 (2009).

Chung J. W., Edwin L. Piner, and T. Palacios , " Effect of Gate Leakage on the Subthreshold Characteristics of AlGaN/GaN HEMTs ," Electron Device Letters 29, 1196-1198 (2008).

Chung J. W., X. Zhao, Y. Wu, J. Singh and T. Palacios, "Effect of image charges in the drain delay of AlGaN/GaN high electron mobility transistors," Appl. Phys. Lett. 92, 093502, Mar. 2008.

Chung, J.W., Edwin L. Piner, and T. Palacios, "N-face GaN/AlGaN HEMTs Fabricated through Layer Transfer Technology," Electron Device Letters 30, 113-116, 2009.

Palacios, T., "Nitride Transistors for Beyond-Si Digital Electronics," 213th Electrochemical Society Meeting, Phoenix, AZ, May 18-23, 2008.

Palacios, T., "GaN and Digital Electronics: A Way out of Moore's Law?," International Symposium on Compound Semiconductors (ISCS-2008), Freiburg, Germany, September 21-24, 2008.

Palacios, T., "Beyond the AlGaN/GaN HEMT: New Concepts for High-Speed Nitride Transistors," International Workshop on Nitride Semiconductors (IWN-2008), Montreaux, Switzerland, October 6-10, 2008.

Saadat, O. I., J. Chung, E. L. Piner, and T. Palacios, "Gate-first GaN HEMT Technology for High Frequency Applications," International Workshop on Nitride Semiconductors, Montreux, Switzerland, October 6-10, 2008.

Palacios, T., "Heterogeneous Integration of Nitride and Si Electronics," Meeting of the American Physical Society, Pittsburg PA (2009).

David Perreault
Associate Professor
Department of Electrical Engineering and Computer Science

COLLABORATORS
J. Kassakian, MIT
J. Lang, MIT
T. Keim, MIT
J. Dawson, MIT
T. Palacios, MIT
C.R. Sullivan, Dartmouth
A.P. Chandrakasan, MIT
D. Anderson, NSC

GRADUATE STUDENTS
J. Burkhart, Res. Asst., EECS
B. Pierquet, Res. Asst., EECS
D. Giuliano, Draper Fellow, EECS
Y. Han, Res. Asst., EECS
A. Hayman, Res. Asst., EECS
J. Hu, Res. Asst., EECS
W. Li, Res. Asst., EECS
R. Pilawa, Res. Asst., EECS
A. Sagneri, Res. Asst., EECS
A. Trubitsyn, Res. Asst., EECS

SUPPORT STAFF
V. Mizuno, Admin. Asst. II

Pierquet, B.J., T.C. Neugebauer, and D.J. Perreault, "A Fabrication Method for Integrated Filter Elements with Inductance Cancellation," *IEEE Transactions on Power Electronics* Vol. 24, No. 3, pp. 838-848, March 2009.

Chung, S., P.A. Godoy, T.W. Barton, E.W. Huang, D.J. Perreault, and J.L. Dawson, "Asymmetric Multilevel Outphasing Architecture for Multi-Standard Transmitters," *2009 IEEE Radio Frequency Integrated Circuits Symposium*, June 2009, pp. 237-240.

Perreault, D.J., J. Hu, J.M. Rivas, Y. Han, O. Leitermann, R.C.N. Pilawa-Podgurski, A. Sagneri, and C.R. Sullivan, "Opportunities and Challenges in Very High Frequency Power Conversion," *2009 IEEE Applied Power Electronics Conference*, Feb. 2009, pp. 1-14.

Rivas, J.M., Y. Han, O. Leitermann, A.D. Sagneri, and D.J. Perreault, "A High-Frequency Resonant Inverter Topology with Low Voltage Stress," *IEEE Transactions on Power Electronics*, Vol. 23, No. 4, pp. 1759-1771, July 2008.

Warren, J.R., K.A. Rosowski, and D.J. Perreault, "Transistor Selection and Design of a VHF DC-DC Power Converter," *IEEE Transactions on Power Electronics*, Vol. 23, No. 1, pp. 27-37, Jan. 2008.

Han, Y., A. Li, G. Cheung, C.R. Sullivan, and D.J. Perreault, "Evaluation of Magnetic Materials for Very High Frequency Power Applications," *2008 IEEE Power Electronics Specialists Conference*, June 2008.

Hu, J., A.D. Sagneri, J.M. Rivas, S.M. Davis, and D.J. Perreault, "High-Frequency Resonant SEPIC Converter with Wide Input and Output Voltage Ranges," *2008 IEEE Power Electronics Specialists Conference*, June 2008.

Pilawa-Podgurski, R.C.N., D. Giuliano, and D.J. Perreault, "Merged Two-Stage Power Converter Architecture with Soft Charging Switched-Capacitor Energy Transfer," *2008 IEEE Power Electronics Specialists Conference*, June 2008.

Rivas, J.M., O. Leitermann, Y. Han, and D.J. Perreault, "A Very High Frequency DC-DC Converter Based on a Phi-2 Resonant Inverter," *2008 IEEE Power Electronics Specialists Conference*, June 2008.

Phinney, J.W., D.J. Perreault, and J.H. Lang, "Synthesis of Lumped Transmission-Line Analogs," *IEEE Transactions on Power Electronics*, Vol. 22, No. 4, pp. 1531-1542, July 2007.

Phinney, J.W., D.J. Perreault, and J.H. Lang, "Radio-Frequency Inverters with Transmission-Line Input Networks," *IEEE Transactions on Power Electronics*, Vol. 22, No. 4, pp. 1154-1161, July 2007.

Han, Y., O. Leitermann, D.A. Jackson, J.M. Rivas, and D.J. Perreault, "Resistance Compression Networks for Radio-Frequency Power Conversion," *IEEE Transactions on Power Electronics*, Vol. 22, No.1, pp. 41-53, Jan. 2007.

Tang, S.C., D.M. Otten, T.A. Keim, and D.J. Perreault, "Design and Evaluation of a 42 V Automotive Alternator with Integrated Switched-Mode Rectifier," *2007 IEEE Vehicle Power and Propulsion Conference*, September 2007.

Pierquet, B.J., T.C. Neugebauer, and D.J. Perreault, "A Fabrication Method for Integrated Filter Elements with Inductance Cancellation," *2007 IEEE Applied Power Electronics Conference*, Anaheim, CA, pp. 51-62, Feb. 25 – Mar. 1, 2007.

Pilawa-Podgurski, R.C.N., A.D. Sagneri, J.M. Rivas, D.I. Anderson, and D.J. Perreault, "High-Frequency Resonant Boost Converters," *2007 IEEE Power Electronics Specialists Conference*, pp. 2718 – 2724, June 2007.

Rivas, J.M., Y. Han, O. Leitermann, A.D. Sagneri, and D.J. Perreault, "A High-Frequency Resonant Inverter Topology with Low Voltage Stress," *2007 IEEE Power Electronics Specialists Conference*, pp. 2705 – 2717, June 2007.

Pierquet, B.J., T.C. Neugebauer, and D.J. Perreault, "Inductance Compensation of Multiple Capacitors with Application to Common- and Differential-Mode Filters," *IEEE Transactions on Power Electronics*, Vol. 21, No. 6, pp. 1815-1824, Nov. 2006. (Also, see "Corrections to Inductance Compensation of Multiple Capacitors with Application to Common- and Differential-Mode Filters," *IEEE Transactions on Power Electronics*, Vol. 22, No. 1, pp. 346-347, Jan. 2007.)

Rajeev J. Ram
Professor
Department of Electrical Engineering and Computer Science

COLLABORATORS
H. Lee, RLE
H. I. Smith, EECS
F. X. Kaertner, EECS
J. L. Hoyt, EECS
V. Stojanović, EECS
K. Asanović, UC Berkeley

GRADUATE STUDENTS
R. Amatya, Res. Asst., EECS
S. Goh, Res. Asst., DMSE
E .Kapusta, Res. Asst, EECS
K.S. K. Lee, Res. Asst., EECS
J. Orcutt, Res. Asst., EECS
P. Santhanam, Res. Asst., EECS

SUPPORT STAFF
C. Bourgeois, Admin. Asst. II

Zaman T., X. Guo, R. J. Ram, "Semiconductor Waveguide Isolators," *Journal of Lightwave Technology*, 26 (2), 291 - 301, January 2008

R. Amatya, C. W. Holzwarth, H. I. Smith, and R. J. Ram, "Precision Tunable Silicon Compatible Microring Filters," *IEEE Photonics Technology Letters*, 20, 1739-41, 2008.

Lee, K. S. and Ram, R. J., 2009, Plastic–PDMS bonding for high pressure hydrolytically stable active microfluidics, *Lab on a Chip*, 9, 1618-24, 2009.

C. Batten, A.Joshi, J. Orcutt, A. Khilo, B. Moss, C. W. Holzwarth, M. A. Popovic, H. Li, H. I. Smith, J. Hoyt, F. X. Kaertner, R. J. Ram, V. Stojanović, Krste Asanovic, "Building Manycore Processor-to-DRAM Networks with Monolithic CMOS Silicon Photonics," *IEEE Micro*, to be published, 2009.

Caroline A. Ross
Professor
Department of Materials Science and Engineering

COLLABORATORS
H.I. Smith
C.V Thompson
E.L. Thomas
R.C. O'Handley
Y. Shao-Horn
K.K. Berggren (MIT)
G. Dionne (Lincoln Lab)
J. Borchers (NIST)
G.J. Vancso (U. Twente, NL)
J.A.C. Bland (Cambridge University)
M. Pardavi-Horvath (George Washington U.)
A. Adeyeye, (Nat. Univ. Singapore)
J.Y. Cheng (IBM)
F.Y. Ogrin (U. Exeter, UK)
M. Vazquez (Madrid)

POSTDOCTOAL ASSOCIATES & VISITING SCIENTISTS
F. Castaño
H. S. Kim
D. Navas
H. Miyagawa
C. Nam
C. Garcia
Y. Oh
M. Ciria
V. Ng.

GRADUATE STUDENTS
W. Jung
F. Ilievski
V. Sivakumar
V. Chuang
Y. S. Jung
A. Taussig
I. Colin
B. Ng
L. Bi
K. Gotrik
M. Mascaro

SUPPORT STAFF
G. Joseph, Admin. Asst. II

V. Sivakumar, N. Yabuuchi, C. A. Ross, Y. Shao-Horn, "Partially reversible changes in magnetic properties of CrO2 nanoparticles through electrochemical cycling," *J. Appl. Phys.* 103 07D708 p1-3 (2008)

V. Sivakumar, C. A. Ross, N. Yabuuchi, Y. Shao-Horn, K. Persson and G. Ceder, "Electrochemical Control of the Magnetic Moment of CrO2," *J. Electrochemical Society* 155(8) p83-88 (2008)

C. A. Ross, F.J. Castaño, W. Jung, B.G. Ng, I.A. Colin, D. Morecroft, "Magnetism in multilayer thin film rings," *J. Phys. D.* 41 113002 p1-6 (2008)

F.J. Castaño, B.G. Ng, I.A. Colin, D. Morecroft, W. Jung, C.A. Ross, "Magnetoresistance of submicron multilayer Wheatstone bridges as a probe of magnetic reversal mechanism," *J. Phys. D* 41 132005 (2008)

Hyun-Suk Kim, Lei Bi, G. F. Dionne, and C. A. Ross, "Structure, magnetic and magneto-optical properties of transition metal-doped transparent SnO2 films," P*hys. Rev. B* 77 214436 (2008)

Y.S. Jung, W. Jung, C.A. Ross, "Self-assembled ring structures from a diblock copolymer under circular confinement," Nano Letts. 8 2975-81 (2008)

I. Bita, J. K.W. Yang, Y. S. Jung, C. A. Ross, E. L. Thomas, K. K. Berggren, "Graphoepitaxy of self-assembled block copolymers on 2D periodic patterned templates," *Science* 321 (5821) p939-943 (2008)

Bi L., A.R. Taussig, H.-S. Kim, L. Wang, G. F. Dionne, D. Bono, G. Ceder and C. A. Ross, "Structural, magnetic and optical properties of BiFeO3 and Bi2FeMnO6 epitaxial thin films: an experimental and first principles study," *Phys. Rev. B* 78 104106 (2008)

V.P. Chuang, C.A. Ross, P. Bilalis, N. Hadjichristides, "Nanoscale rings fabricated using Self-Assembled Triblock Terpolymer Templates," *ACS Nano* 2(10) 2007-2014 (2008)

Kim, H.-S., L. Bi, G. F. Dionne, and C. A. Ross, "Structural, magnetic, and magneto-optical properties of transparent Fe-doped SrTiO3 films," *Appl. Phys. Letts.* 93 092506 (2008)

S. Moralejo, F. J. Castaño, C. A. Ross, C. Redondo and F. Castaño, "Collective switching of single-layer and exchange bias coupled nanomagnet arrays," *J. Phys. D* 41 195003 (2008)

G.M. Muller, G. Eilers, Z. Wang, M. Scherff, Ran Ji, K. Nielsch, C.A. Ross, M. Münzenberg, "Magnetization dynamics in optically excited nanostructured nickel films," *New J. Phys.* (2008)

Y.S. Jung, W. Jung, H.L. Tuller, C.A. Ross, "Nanowire conductive polymer gas sensor patterned using self-assembled block copolymer lithography," *Nano Letts.* 8 (11), 3776–3780 (2008)

Y. S. Jung, C.A. Ross, "Solvent vapor induced tunability of self-assembled block copolymer patterns," *Adv. Mater.* 21 2540-2545 (2009)

Y.J. Oh, C.A. Ross, Y.S. Jung, Y. Wang, C.V. Thompson, "Co nanoparticle arrays made by templated solid-state dewetting," *Small* 5 860-856 (2008)

E. Verploegen, T. Zhang, Y. S. Jung, C. Ross, and P. T. Hammond, "Controlling the Morphology of Side Chain Liquid Crystalline Block Copolymer Thin Films through Variations in Liquid Crystalline Content," *Nano Letts.* 8 (10), pp 3434–3440 (2008)

C. A. Ross, Y.S. Jung, V.P. Chuang, F. Ilievski, J.K.W. Yang, I. Bita, E.L. Thomas, H.I. Smith, K.K. Berggren, G.J. Vancso, J.Y. Cheng, "Si-containing block copolymers for self-assembled nanolithography (invited)," J. *Vac. Sci. Technol. B* 26(6) 2489-94 (2008)

C. Nam, B.G. Ng, F. J. Castaño, and C. A. Ross, Effect of magnetic field direction on the remanent resistance levels and vortex chirality of a multilayered magnetic ring," *J. Appl. Phys.* 105 033918 (2009)

C. Nam, B. G. Ng, F. J. Castaño, M. D. Mascaro and C. A. Ross, "Current-driven vortex formation in a magnetic multilayer ring," *Appl. Phys. Letts.* 94 082501 (2009)

K. L. Krycka, B. B. Maranville, J. A. Borchers, F. J. Castaño, B. G. Ng, J. C. Perkinson, C. A. Ross, "Magnetic Domain Formation within Patterned NiFe/Cu/Co Ellipses," *J. Appl. Phys.* 105 07C120 (2009)

J. L. Sánchez Llamazares1, B. Hernando1, V. Prida1, C. García, J. González, R. Varga and C. A. Ross, "Magnetic field influence on the structural transformation in ferromagnetic shape memory alloy Mn50Ni40In10 melt spun ribbons," *J. Appl. Phys.*105 07A945 (2009)

Rahul Sarpeshkar
Associate Professor
Department of Electrical Engineering and Computer Science

COLLABORATORS
J. Wyatt, MIT

POSTDOCTORAL ASSOCIATE
L. Turicchia, EECS

GRADUATE STUDENTS
S. Arfin, Res. Asst., EECS
S. Mandal, Res. Asst., EECS
B. Rapoport, Grad. Student, EECS
W. Wattanapanitch, Res. Asst., EECS
D. P. Kumar, Res. Asst., EECS

SUPPORT STAFF
S. Davco, Admin. Asst.

Sarpeshkar, R., W. Wattanapanitch, S.K. Arfin, B. I. Rapoport, S. Mandal, M. Baker, M. Fee, S. Musallam, and R. A. Andersen, "Low-Power Circuits for Brain-Machine Interfaces," *IEEE Transactions on Biomedical Circuits and Systems*, Vol. 2, No. 3, pp. 173 – 183, September 2008.

Mandal, S., and R. Sarpeshkar, "Power-efficient Impedance-Modulation Wireless Data Links for Biomedical Implants," *IEEE Transactions on Biomedical Circuits and Systems*, Vol. 2, No. 4, pp. 301—315, 2008.

Wee, K.H., L.Turicchia, and R. Sarpeshkar, "An Analog Integrated-Circuit Vocal Tract," *IEEE Transactions on Biomedical Circuits and Systems*, Vol. 2, No. 4, pp. 316—327, 2008.

Mandal, S., S. K. Arfin, and R. Sarpeshkar, "Sub-uHz MOSFET *1/f* noise measurements," *Electronics Letters*, Vol. 45, No. 1, pp. 81-82, January 1 2009.

Mandal, S., S. Zhak, and R. Sarpeshkar, "A Bio-inspired Active Radio-Frequency Silicon Cochlea," *IEEE Journal of Solid-State Circuits*, accepted for publication, expected June 2009.

Martin A. Schmidt
Professor
Department of Electrical Engineering and Computer Science

COLLABORATORS
A. Akinwande, MIT
V. Bulović, MIT
K.F. Jensen, MIT
S.G. Kim, MIT
C.G. Sodini, MIT
J. Sims, Harvard-MGH
M. Toner, Harvard-MGH
D. Keszler, Oregon State University
Research Staff
H. Li, Research Scientist

GRADUATE STUDENTS
K. Cheung, Res. Asst., EECS
E. Lam, Res. Asst., EECS
V. Sharma, Res. Asst., EECS
H. Zhou, Res. Asst., DMSE

R. Huang, T. A. Barber, M. A. Schmidt, R. G. Tompkins, M. Toner, D. W. Bianchi, R. Kapur, W. L. Flejter, "A microfluidics approach for the isolation of nucleated red blood cells (NRBCs) from the peripheral blood of pregnant women," Prenatal Diagnosis, Volume 28 Issue 10, Pages 892 – 899

N. de Mas, A. Gunther, M. A. Schmidt, and K. F. Jensen, "Increasing Productivity of Microreactors for Fast Gas−Liquid Reactions: The Case of Direct Fluorination of Toluene,", Ind. Eng. Chem. Res., 2009, 48 (3), pp 1428–1434

Savoulides, N. Jacobson, S.A., H. Li, L. Ho, Khanna, R., C.-J. Teo, Protz, J.M., L. Wang, Ward, D. Schmidt, M. A., Epstein, A. H., "Fabrication and Testing of a High-Speed Microscale Turbocharger", Journal of Microelectromechanical Systems, Oct. 2008, Volume: 17, Issue: 5, Pages 1270-1282

J. Chen, V. Leblanc, S. H. Kang, P. J. Benning, D. Shut, M. A. Baldo, M. A. Schmidt, and V. Bulović, High definition digital fabrication of organic devices by molecular jet printing, Advanced Functional Materials, vol. 17, no. 15, pp. 2722-2727, Oct. 2007.

V. Leblanc, J. Chen, S. H. Kang, V. Bulović, and M. A. Schmidt, "Micromachined printheads for the evaporative patterning of organic materials and metals," IEEE/ ASME Journal of Microelectromechanical Systems, vol. 16, no. 2, pp. 394-400, Apr. 2007.

L. R. Arana, N. deMas, R. Schmidt, A. J. Franz, M. A. Schmidt, and K. F. Jensen, "Isotropic etching of silicon in fluorine gas for MEMS micromachining," Journal of Micromechanics and Microengineering, vol. 17, no. 2, pp. 384-392, Feb. 2007.

Y. Wada, M. A. Schmidt, and K.F. Jensen,"Flow distribution and ozonolysis in gas-liquid multichannel microreactors," Industrial & Engineering Chemistry Research, vol. 45, no. 24, pp. 8036-8042, Nov. 2006.

B. A. Wilhite, S. E. Weiss, J.Y. Ying, M. A.Schmidt, and K. F. Jensen, "High-purity hydrogen generation in a microfabricated 23 wt % Ag-Pd membrane device integrated with 8:1 $LaNi_{0.95}Co_{0.0503}/Al_20_3$ catalyst," Advanced Materials, vol. 18, no. 13, pp. 1701-1710, July 2006.

J. G. Kralj, M. T. W., Lis, M. A. Schmidt, and K. F. Jensen, "Continuous dielectrophoretic size-based particle sorting," Analytical Chemistry, vol. 78, no. 14, pp. 5019-5025,July 2006.

Henry I. Smith
Professor
Department of Electrical Engineering and Computer Science

COLLABORATORS
J. T. Hastings, Univ. Kentucky
M. Qi, Purdue University
C. V. Thompson, MIT
F. R. Stellacci, MIT
E. Ippen, MIT
F. Kaertner, MIT
M. Schattenburg, MIT
E. L. Thomas, MIT
K. K. Berggren, MIT
V. Stojanović, MIT

GRADUATE STUDENTS
C. Fuceltola, Res. Asst., EECS
C. Holzwarth, Res. Asst., MSE
T. B. O'Reilly, Res. Asst., ME
A. Patel, Res. Asst., EECS
S. Tsai, Res. Asst., EECS
J. Sun, Res. Asst., EECS
L. L. Cheong, Res. Asst., EECS

SUPPORT STAFF
A. Akins, Admin. Asst.
J. Daley, Project Technician
M. Mondol, Facility Manager, SEBL
R. Menon, Research Scientist
T. Savas, Visiting Scientist
E. Moon, Research Scientist
F. Zhang, Research Affiliate

T. B. O'Reilly and H. I. Smith, "Photoresist characterization using double-exposure with interference lithography," J. Vac. Sci. Techno. B 26(1), 128-131 (2008).

J. Sun, C.W. Holzwarth, M. Dahlem, J.T. Hastings, and H.I. Smith, "Accurate Frequency Alignment in Fabrication of High-Order Microring-resonator Filters", Opt. Express 16(20), 15958-15963 (2008).

T. Barwicz, C. W. Holzwarth, P.T. Rakich, M. A. Popovic, E. P. Ippen, and H. I. Smith, "Optical loss in silicon microphotonic waveguides induced by metallic contamination", Appl. Phys. Lett. 92(13), 131108 (2008).

T. B. O'Reilly and H. I. Smith, "Linewidth uniformity in Lloyd's mirror interference lithography systems," J. Vac. Sci. Technol. B 26(6), p.2131 – 2134, Nov/Dec 2008.

C. W. Holzwarth, R. Amatya, M. Dahlem, A. Khilo, F. X. Kärtner, E. P. Ippen, R. J. Ram, and H. I. Smith, "Fabrication strategies for filter banks based on microring resonators," J. Vac. Sci. Technol. B 26(6), p. 2164 – 2165, Nov/Dec (2008).

E. E. Moon, and H. I Smith, "Nanometer, level-alignment to a substrate-embedded coordinate system," J. Vac. Sci. Technol. B 26(6), p. 2341-2344, Nov/Dec (2008).

C. A. Ross, Y. S. Jung, V. P. Chuang, F. Ilievski, J. K. W. Yang, I. Bita, E. L. Thomas, H. I. Smith, K. K. Berggren, G. J. Vansco, and J. Y. Cheng, "Si-containing block copolymers for self-assembled nanolithography," J. Vac. Sci. Technol. B 26(6), p. 2489-2494, Nov/Dec (2008).

H. I. Smith, C. V. Thompson, and M. H. Hong, "Synthesis of Silicon Nanowires and Nanofin Arrays Using Interference Lithography and Catalytic Etching," Nano Letters, Vol. 8(11 , p.3799-3802, (2008).

"System and method for fabrication and replication of diffractive optical elements for maskless lithography," D. Gil, J. T. Hastings, J. G. Goodberlet, R. Menon, P. J. Carter, and H. I. Smith, US Patent 7,348,104, March 25, 2008.

"Imaging System and Method Employing Beam Folding", R. Menon and H. I. Smith, US Patent 7,405,806, July 29, 2008.

"Spatial-phase locking of energy beams for determining two-dimensional location and beam shape," J. T. Hastings, J. G. Goodberlet, F. Zhang, and H. I. Smith US Patent 7,417,234, Aug. 26, 2008.

"Nanoscale imaging via absorbance modulation," R. Menon and H. I. Smith, filed August 2008.

Charles G. Sodini
LeBel Professor
Department of Electrical Engineering & Computer Science

COLLABORATORS
D. Buss, Texas Instruments
P. Holloway, National Semiconductor

GRADUATE STUDENTS
D. He, Res. Asst., EECS
I. Nausieda, Martin Family Society of
Fellows for Sustainability, EECS
K. Nguyen, Res. Asst., EECS
J. Powell, Res. Asst., EECS
E. Winokur, Res. Asst. EECS
K. Chen, Res. Asst. EECS
K. Ryu, Res. Asst., EECS

SUPPORT STAFF
C. Kinsella, Admin. Asst. II

T. Sepke, P. Holloway, C. G. Sodini, and H. S. Lee, "Noise Analysis for Comparator-Based Circuits," *IEEE Transactions on Circuit Systems-I*, vol. 56, no. 3, pp. 541-553, March 2009.

J. D. Powell, H, Kim, and C. G. Sodini, "SiGe Receiver Front Ends for Millimeter-Wave Passive Imaging," *IEEE Transactions on Microwave Theory & Techniques,* vol. 56, no. 11, pp. 2416-2425, Nov. 2008

J. Yu, J. R. Tischler, C. G. Sodini, and V. Bulović, "Using Integrated Optical Feedback to Counter Pixel Aging and Stabilize Light Output of Organic LED Display Technology," *Journal of Display Technology,* vol. 4, no. 3, pp. 308-313, Sept. 2008.

H.-S. Lee and C. G. Sodini, "Analog-to-digital converters: Digitizing the analog world," *Proceedings of the IEEE*, vol. 96, no. 2, pp. 323-334, Feb. 2008.

I. Nausieda, K. Ryu, I. Kymissis, A.I. Akinwande, V. Bulović, and C. G. Sodini, "An organic active-matrix imager," *IEEE Transactions on Electron Devices,* vol. 55, no. 2, pp. 527-532, Feb. 2008.

Vladimir Stojanović
Assistant Professor
Department of Electrical Engineering and Computer Science

COLLABORATORS
E. Alon, UC Berkeley
K. Asanovic, UC Berkeley
A. Kavcic, U. Hawaii
M. Horowitz, Stanford University
D. Markovic, UC Los Angeles
C-K. K. Yang, UC Los Angeles

GRADUATE STUDENTS
N. Blitvić, Res. Asst., EECS
F. Chen, Res. Asst., EECS
M. Georgas, Res. Asst., EECS
B. Kim, Res. Asst., EECS
J. Leu, Res. Asst., EECS
Y. Li, Res. Asst., EECS
B. Moss, Res. Asst., EECS
S. Song, Res. Asst., EESC
R. Sredojeević, Res. Asst., EECS

K.S. Oh, F. Lambrecht, S. Chang, Q. Lin, J. Ren, C. Yuan, J. Zerbe, and V. Stojanović, "Accurate System Voltage and Timing Margin Simulation in High-Speed I/O System Design," *IEEE Transactions on Advanced Packaging*, vol. 31, no. 4, pp. 722-730, 2008.

B. Kim and V. Stojanović, "Modeling and Design Framework: Equalized and Repeated Interconnects for Networks-on-Chip [Invited]," *IEEE Design & Test of Computers*, vol. 25, no. 5, pp. 430-439, 2008.

T. Barwicz, H. Byun, F. Gan, C. W. Holzwarth, M. A. Popovic, P. T. Rakich, M. R. Watts, E. P. Ippen, F. X. Kärtner, H. I. Smith, J. S. Orcutt, R. J. Ram, V. Stojanović, O. O. Olubuyide, J. L. Hoyt, S. Spector, M. Geis, M. Grein, T. Lyszczarz, and J. U. Yoon, " Silicon photonics for compact, energy-efficient interconnects [Invited]," J. Opt. Netw. 6, 63-73 (2007)

B. Kim and V. Stojanović, "A 4 Gb/s/ch 356fJ/b 10 mm Equalized On-Chip Interconnect with Nonlinear Charge-Injecting Transmit Filter and Transimpedance Receiver in 90 nm CMOS Technology," *IEEE International Solid-State Circuits Conference*, San Francisco, CA, pp. 66-67, February 2009.

R. Sredojević and V. Stojanović, "Optimization-based Framework for Simultaneous Circuit and System Design-Space Exploration: A High-Speed Link Example," *IEEE/ACM International Conference on Computer-Aided Design*, San Jose, CA, pp. 314-321, November 2008.

F. Chen, H. Kam, D. Marković, T.J. King, V. Stojanović, and E. Alon, "Integrated Circuit Design with NEM Relays," *IEEE/ACM International Conference on Computer-Aided Design*, San Jose, CA, pp. 750-757, November 2008.

C. Batten, A. Joshi, J. Orcutt, A. Khilo, B. Moss, C. Holzwarth, M. Popovic, H. Li, H. Smith, J. Hoyt, F. Kaertner, R. Ram, V. Stojanović, and K. Asanovic, "Building manycore processor to DRAM networks with monolithic silicon photonics," *IEEE Symposium on High-Performance Interconnects*, Stanford, CA, pp. 21-30, August 2008.

A. Amirkhany, A. Abbasfar, J. Savoj, M. Jeeradit, B. Garlepp, V. Stojanović, M. A. Horowitz "A 24Gb/s Software Programmable Analog Multi-Tone Transmitter," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 4, pp. 999-1009, 2008.

N. Blitvic, L. Zheng, V. Stojanović "Low-complexity Pattern-eliminating Codes for ISI-limited Channels," to appear in *IEEE International Communications Conference*, May 2008.

C. W. Holzwarth, J. S. Orcutt, H. Li, M. A. Popović, V. Stojanović, J. L. Hoyt, R. J. Ram, and H. I. Smith "Localized Substrate Removal Technique Enabling Strong-Confinement Microphotonics in Bulk Si CMOS Processes," to appear in *Optical Society of America - CLEO/QELS Conference*, May 2008.

J. S. Orcutt, A. Khilo, M. A. Popović, C. W. Holzwarth, B. Moss, H. Li, M. S. Dahlem, T. D. Bonifield, F. X. Kärtner, E. P. Ippen, J. L. Hoyt, R. J. Ram and V. Stojanović "Demonstration of an Electronic Photonic Integrated Circuit in a Commercial Scaled Bulk CMOS Process," to appear in *Optical Society of America - CLEO/QELS Conference*, May 2008.

B. Kim and V. Stojanović "Equalized Interconnects for On-Chip Networks: Modeling and Optimization Framework," IEEE/ACM International Conference on Computer-Aided Design, San Jose, CA, pp. 552-559, November 2007

F. Chen, A. Joshi, V.Stojanović and A. Chandrakasan "Scaling and Evaluation of Carbon Nanotube Interconnects for VLSI Applications," *ACM International Conference on Nano-Networks*, Catania, Sep. 2007.

A. Amirkhany, A. Abbasfar, V. Stojanović and M.A. Horowitz "Practical Limits of Multi-Tone Signaling Over High-Speed Backplane Electrical Links," *IEEE International Conference on Communications*, pp. 2693-2698, June 2007.

N. Blitvic and V. Stojanović "Statistical Simulator for Block Coded Channels with Long Residual Interference," *IEEE International Conference on Communications*, pp. 6287-6294, June 2007.

Carl V. Thompson

Stavros Salapatas Professor of Materials Science & Engineering
Department of Material Science & Engineering

COLLABORATORS

D.A. Antoniadis, MIT
W.K. Choi, National University of Singapore
S.J. Chua, Professor, ECE, NUS
E.A. Fitzgerald, MIT
C.L. Gan, Nanyang Technical University
C. Hau-Riege, Advanced Micro Devices
D. Kim, Post Doctoral Research Associate, MSE, MIT
M. Li, Research Affilliate, Panasonic Boston Laboratory
Y. Li, NUS
P. Makaram, Post Doctoral Research Associate, MSE, MIT
Y.J. Park, Texas Instruments
K.L. Pey, Associate Professor, NTU
C.A. Ross, Professor, MSE, MIT
H.I. Smith, MIT

GRADUATE STUDENTS

A. Alobeidi, Res. Asst., DMSE
S. Boles, Res. Asst., DMSE
S.-W. Chang, Res. Asst., DMSE
L.Y Chang, Res. Asst., DMSE
T. Chookajorn, Res. Asst., DMSE
P. Delcroix, Res. Asst., DMSE
H.L. Leong, SMA Fellow, SMA
R. Mitchell, Zerox Fellow, DMSE
R. Nagarajian, DMSE
J. Oh, Res. Asst., DMSE
T.J. Park, Res. Asst., DMSE
G. Qiang, SMA Fellow, NUS
W. Sasangka, SMA Fellow, DMSE
Y.C Shin, , Res. Asst., DMSE
P. Yang, Res. Asst., DMSE
J. Ye, Res. Asst., DMSE
L. You, Res. Asst, DMSE
H. Yu, Res. Asst., DMSE.
J. Yun, SMA Fellow, NUS

SUPPORT STAFF

K. Fitzgerald, Admin. Asst. II

R. Tadepalli, K.T. Turner, and C.V. Thompson, "Mixed Mode Interface Toughness of Wafer-Level Cu-Cu Bonds Using Asymmetric Chevron Test," *J. Mech. Phys. Sol.* 56, 707 (2008).

Z.-S. Choi, R. Mönig, and C.V. Thompson, "Effects of Microstructure on the Formation, Shape, and Motion of Voids During Electromigration in Passivated Copper Interconnects," *J. Mater. Res.* 23, 383 (2008).

R. Tadepalli, K.T. Turner and C.V. Thompson, "Effects of Patterning on the Interface Toughness of Wafer-Level Cu-Cu Bonds," *Acta Mater.* 56, 438 (2008).

H.L. Leong, C.L Gan, C.V. Thompson, K.L Pey, and H.Y. Li, "Application of Contact Theory to Metal-Metal Bonding of Silicon Wafers," *J. Appl. Phys.* 102, 103510 (2007).

W.K. Choi, T.H. Liew, H.G. Chew, F. Zheng, C.V. Thompson. Y. Wang, M.H. Hong, X.D. Wang , L. Li and J. Yun, "A Combined Top-down and Bottom-up approach for Precise Placement of Metal Nanoparticles on Silicon," *Small* 4, 330 (2008).

J. Oh and C.V. Thompson, "Selective Barrier Perforation in Porous Alumina Anodized on Substrates," *Advanced Materials* 20, 1368 (2008).

F.L. Wei, C.S. Hau-Riege, A.P. Marathe, and C.V. Thompson, "Effects of active atomic sinks and reservoirs on the reliability of Cu/low-k interconnects," *J. Appl. Phys.* 103, 084513 (2008).

F.L. Wei , C.L. Gan and T.L. Tan, C.S. Hau-Riege and A.P. Marathe, J.J. Vlassak, and C.V. Thompson, "Electromigration-Induced Extrusion Failures in Cu/low-k Interconnects," *J. Appl. Phys.* 104, 023259 (2008).

J.A. Kalb, Q. Guo, X. Zhang, Y. Li, C. Sow, and C.V. Thompson, "Phase-Change Materials in Optically Triggered Microactuators," *J. Microelectromechanical Systems* 17, 1094 (2008).

G.D. Nessim, A.J Hart, J.S. Kim, D. Acquaviva, J. Oh, C.D. Morgan, M.Seita, J.S. Leib, and C.V. Thompson, "Tuning of Vertically-Aligned Carbon Nanotube Diameter and Areal Density through Catalyst Pre-Treatment," *Nano Letters* 8, 3587 (2008).

W. K. Choi, T. H. Liew, M. K. Dawood, H. I. Smith , C. V. Thompson, and M. H. Hong, "Synthesis of silicon nanowires and nanofin arrays using interference lithography and catalytic etching," Nano Letters 8, 3799 (2008).

Yong-Jun Oh, C. A. Ross, Yeon Sik Jung, Yang Wang, C. V. Thompson, "Co nanoparticles arrays made by templated solid-state dewetting," *Small* 5, 860 (2009).

Q. Guo, M. Li, Y. Li, L. Shi, T.C. Chong, J.A. Kalb, and C.V. Thompson, "Crystallization-induced stress in thin phase change films of different thicknesses," *Appl. Phys. Lett.*, 93, 221907 (2008).

Y. Li, Q. Guo, J.A. Kalb, and C.V. Thompson, "Matching Glass-Forming Ability with the Density of the Amorphous Phase," *Science* 322, 1816 (2008).

H. L. Leong, C. L. Gan, R. I. Made, C. V. Thompson, K. L. Pey, and H. Y. Li, "Experimental characterization and modeling of the contact resistance of Cu–Cu bonded interconnects," *J. Appl. Phys.* 105, 033514 (2009).

H. L. Leong, C. L. Gan, C. V. Thompson, K. L. Pey, and H. Y. Li, "Electromigration-induced bond improvement for three-dimensional integrated circuits," *Appl. Phys. Letts.* 94 (2009).

S.-W. Chang, V.P. Chuang, S.T. Boles, C.A. Ross, and C.V. Thompson, "Densely-packed arrays of ultrahigh-aspect-ratio silicon nanowire fabricated using block copolymer lithography and metal-assisted etching," *Advanced Functional Materials* (2009).

C.V. Thompson, "Carbon Nanotubes as Interconnects: Emerging Technology and Potential Reliability Issues," *46th International Reliability Symposium, IEEE CFP08RPS-PRT,* p. 368 (2008).

Harry L. Tuller
Professor
Department of Materials Science and Engineering

COLLABORATORS
I. D. Kim, KIST, Korea
E. Ivers-Tiffee & D. Gerthsen, University of Karlsruhe, Germany
M. Martin & R. DeSouza, Aachen University, Germany
J. Lewis, Univ. of Illinios
A. Rothschild, Technion University in Israel
D. Nocera, MIT

GRADUATE STUDENTS
W. Jung, Res. Asst., MSE
Y. Jin, Res. Asst., MSE
S. Litzelman, Res. Asst., MSE
G. Whitfield, Res. Asst., MSE
D. Chen, Res. Asst., MSE
J. Engel, Res. Asst., MSE
K. Haga, Visiting student (Kyushu U.)

SUPPORT STAFF
A. Rothwell, Admin. Asst. II

J. L. Hertz and H. L. Tuller, "Micro-fuel Cells" in A. Mitsos and P.I. Barton (eds.), M*icrofabricated Power Generation Devices: Design and Technolog*y, Wiley-VCH, Weinheim, Germany, 2009, pp.51-80.

W.C. Jung, J. L. Hertz, H. L Tuller, "Enhanced Ionic Conductivity and Phase Meta-stability of Nano-sized Thin Film Yttria-doped Zirconia (YDZ)," *Acta Materialia*, **57**, 1399-1404 (2009).

H. L. Tuller, S. J. Litzelman and W.C. Jung, "Micro-ionics: Next Generation Power Sources," *Phys. Chem. Chem. Phys.*, 11, 3023 – 3034 (2009).

A. Bieberle-Hütter, J. L. Hertz, and H. L. Tuller, "Fabrication and Electrochemical Characterization of Planar Pt-CGO Microstructures," *Acta Materiali*, ***56***, 177-187 (2008),

I.-D. Kim, A. Rothschild, D.-J. Yang, and H. L. Tuller, "Macroporous TiO_2 Thin Film Gas Sensors Obtained Using Colloidal Templates," *Sens. Actuators B: Chem.* ***130***, 9–13 (2008)

S. J. Litzelman, R. A. De Souza, B. Butz, and H. L. Tuller, M. Martin, and D. Gerthsen, "Heterogeneously Doped Nanocrystalline Ceria Films by Grain Boundary Diffusion: Impact on Transport Properties," *J. Electroceramics*, published online February 2008.

J. L. Hertz, A. Rothschild, and H. L. Tuller, "Highly Enhanced Electrochemical Performance of Silicon-Free Platinum - Yttria Stabilized Zirconia Interfaces," *J. Electroceramics*, published online March 08.

J. Hiltunen, J. Lappalainen, J. Puustinen, V. Lantto, and H. L. Tuller, "Size-dependent Optical Properties of $BaTiO_3$ - $SrTiO_3$ Superlattices," *Optics Express*, **16,** 8219-8228 (2008)

S.J. Litzelman, J.L. Hertz, W.C. Jung and H.L. Tuller, "Opportunities and Challenges in Materials Development for Thin Film Solid Oxide Fuel Cells," *Fuel Cells*, **8**, 294-302 (2008).

W.C.Jung and H.L. Tuller, "Investigation of Cathode Behavior of Model Thin Film $SrTi_{1-x}Fe_xO_{3-\delta}$ (x =0.35 and 0.5) Mixed Ionic-Electronic Conducting Electrodes," *J. Electrochem. Soc.*, **155,** B1194-B1201 (2008).

J. Hiltunin, D. Seneviratne, R. Sun, M. Stolfi, H.L. Tuller, J. Lappalaninen and V. Lanto, "Crystallographic and Dielectric Properties of Highly Oriented $BaTiO_3$ Thin Films: Influence of Oxygen Pressure Utilized During Pulsed Laser Deposition," *J. Electroceramics*, published online 8 March 2008. 10p.

J. Hiltunin, D. Seneviratne, H.L. Tuller, J. Lappalaninen and V. Lanto, "Optical Properties of $BaTiO_3$ Thin Films: Influence of Oxygen Pressure Utilized During Pulsed Laser Deposition," *J. Electroceramics,* published online 7 March 2008. 5p.

K. Sahner, H.L. Tuller, "Novel Deposition Techniques for Metal Oxides - Prospects for Gas Sensing," *J. Electroceram.*, 23pp, published online September 25, 2008. Feature article.

Y. S. Jung, W.C. Jung, H.L. Tuller, C. A. Ross, "Nanowire Conductive Polymer Gas Sensor Patterned Using Self-Assembled Block Copolymer Lithography," *Nano Lett.* **8**, 3776-3780 (2008).

Joel Voldman
Associate Professor
Department of Electrical Engineering and Computer Science

COLLABORATORS
R. Jaenish, MIT
K.M. Lim, NUS, Singapore
F. McKeon, Harvard Med. School
L. Samson, MIT
P. Sorger, Harvard Med. School
J. White, MIT

POSTDOCTORAL ASSOCIATES
K. Blagović
Y.-C. Toh
W.-M. Tsang

GRADUATE STUDENTS
S. Desai, Res. Asst., EECS
M. Hoehl, Res. Asst., HST
J.R. Kovac, Res. Asst., EECS
N. Mittal, Res. Asst., Physics
L. Pryzbyla, Res. Asst., Biology
P. Sampattavanich, Res. Asst., HST
M. Vahey, Res. Asst., EECS

SUPPORT STAFF
C. Collins, Admin. Asst.

S. P. Desai, D. M. Freeman, and J. Voldman, "Plastic masters - rigid templates for soft lithography," *Lab on a Chip*, in press, 2009.

M. D. Vahey and J. Voldman, "Characterization of diverse cell and particle types using iso-dielectric separation," *Analytical Chemistry*, vol. 81, pp. 2446-55, 2009.

S. P. Desai, M. D. Vahey, and J. Voldman, "Vesicle libraries - tools for dielectrophoresis metrology," *Langmuir*, vol. 25, pp. 3867-75, 2009.

B. M. Taff, S. P. Desai, and J. Voldman, "Electroactive hydrodynamic weirs for microparticle manipulation and patterning," *Applied Physics Letters*, vol. 94, 084102, 2009.

A. M. Skelley, O. Kirak, H. Suh, R. Jaenisch, and J. Voldman, "Microfluidic Control of Cell Pairing and Fusion," *Nature Methods*, vol. 6, pp. 147-52, 2009.

D. C. Daly, P. P. Mercier, M. Bhardwaj, A. L. Stone, J. Voldman, R. Levine, J. G. Hildebrand, and A. P. Chandrakasan, "A Pulsed UWB Receiver SoC for Insect Motion Control," in *ISSCC*, San Francisco, 2009.

M. D. Vahey and J. Voldman, "Sorting concentrated suspensions: particle interactions, emergent behavior, and implications for microfluidic separations," in *Micro Total Analysis Systems '08*, San Diego, CA, USA, 2008, pp. 1474-76.

M. D. Vahey and J. Voldman, "High-throughput cell and particle characterization using iso-dielectric separation," in *Micro Total Analysis Systems '08*, San Diego, CA, USA, 2008, pp. 1187-89.

W. M. Tsang, Z. Aldworth, A. Stone, A. Permar, R. Levine, J. G. Hildebrand, T. Daniel, A. I. Akinwande, and J. Voldman, "Insect flight control by neural stimulation of pupae-implanted flexible multisite electrodes," in *Micro Total Analysis Systems '08*, San Diego, CA, USA, 2008, pp. 1922-24.

A. M. Skelley and J. Voldman, "An active, integrated bubble trap and debubbler for microfluidic applications," in *Micro Total Analysis Systems '08*, San Diego, CA, USA, 2008, pp. 1360-62.

S. Sampattavanich, B. M. Taff, S. P. Desai, and J. Voldman, "Organizing complex multicellular constructs using stencil-delineated electroactive patterning (S-DEP)," in *Micro Total Analysis Systems '08*, San Diego, CA, USA, 2008, pp. 567-69.

S. P. Desai and J. Voldman, "Measuring the impact of dielectrophoresis on cell physiology using a high-content screening platform," in *Micro Total Analysis Systems '08*, San Diego, CA, USA, 2008, pp. 1308-10.

H.-H. Cui, K.-M. Lim, and J. Voldman, "Experiment and modeling of pillar array micro-traps with negative dielectrophoresis," in *Micro Total Analysis Systems '08*, San Diego, CA, USA, 2008, pp. 1012-14.

K. Blagovic, L. Y. Kim, A. M. Skelley, and J. Voldman, "Microfluidic control of stem cell diffusible signaling," in *Micro Total Analysis Systems '08*, San Diego, CA, USA, 2008, pp. 677-679.

M. D. Vahey and J. Voldman, "A new equilibrium method for continuous-flow cell sorting using dielectrophoresis," *Analytical Chemistry*, vol. 80, pp. 3135-43, 2008.

A. M. Skelley and J. Voldman, "An Active Bubble Trap and Debubbler for Microfluidic Systems," *Lab Chip*, vol. 8, pp. 1733-7, 2008.

T. D. Robinson, B.-H. Ooi, B. M. Taff, K. E. Willcox, and J. Voldman, "Surrogate-Based Optimization of a Microfluidic Weir Structure for Single-Cell Manipulation," in *12th AIAA/ISSMO Multidisciplinary Analysis and Optimization Conference*, Victoria, British Columbia, Canada, 2008.

J. R. Kovac and J. Voldman, "Image-based cell sorting using optofluidics," in *2008 IEEE/LEOS Summer Topical Meeting on Optofluidics*, Acapulco, Mexico, 2008.

S. P. Desai, B. M. Taff, and J. Voldman, "A photopatternable silicone for biological microsystems " *Langmuir*, vol. 24, pp. 575-81, 2008.

Evelyn N. Wang
Assistant Professor
Department of Mechanical Engineering

COLLABORATORS
Jeff Lang, MIT
John Brisson, MIT
Gang Chen, MIT
D. Streit, Northrop-Grumman
K. Thorsen, Lockheed-Martin

GRADUATE STUDENTS
K. Chu, Res. Asst., MechE
B. Fellman, Res. Asst., MechE
T. Humplik, Res. Asst., MechE
A. Kariya, Res. Asst., MechE
C. Koveal, Res. Asst., MechE
A. Lenert, Res. Asst., MechE
K. Suabedissen, Res. Asst., MechE
R. Xiao, Res. Asst., MechE

SUPPORT STAFF
T. Swatkowski, Admin. Asst. II

Xiao, R., Chu, K.-H., and E.N. Wang, "Multi-layer Liquid Spreading on Superhydrophilic Nanostructured Surfaces," accepted, Applied Physics Letters, 2009.

Wang, E.N., Bucaro, M., Taylor, J.A., Kolodner, P., Aizenberg, J., and T. Krupenkin, "Droplet Mixing Using Electrically Tunable Superhydrophobic Nanostructured Surfaces," Microfluidics and Nanofluidics, DOI 10.1007/s10404-008-0364-7, 2008.

Krupenkin, T.N., Taylor, J.A., Wang, E.N., Kolodner, P., Hodes, M., and T.R. Salamon,"Reversible Wetting-dewetting Transitions on Electrically Tunable Superhydrophobic Nanostructured Surfaces," Langmuir 23, 9128-9133, 2007.

Wang, E.N., Devasenathipathy, S., Lin, H., Hidrovo, C.H., Santiago, J.G., Goodson, K.E., and T.W. Kenny," A Hybrid Method for Bubble Reconstruction in Two-Phase Microchannels," Experiments in Fluids 40, 847 858, 2006.

Kenny, T.W., Goodson, K.E., Santiago, J.G., Wang, E., Koo, J.-M., Jiang, L., Zhang, L., Fogg, D., Yao, S., Rose, K., Flynn, R., Cheng, C.-H., and C. Hidrovo, "Advanced Cooling Technologies for Microprocessors," International Journal of High Speed Electronics and Systems 16, 301-313, 2006.

Hidrovo, C.H., Kramer, T.A., Wang, E.N., Vigneron, S., Steinbrenner, J.E., Koo, J.-M., Wang, F.-M., Fogg, D.W., Flynn, R.D., Lee, E.S., Cheng, C.-H., Kenny, T.W., Eaton, J.K., and K.E. Goodson, "Two-Phase Microfluidics for Semiconductor Circuits and Fuel Cells," Heat Transfer Engineering 27, 53-63, 2006.

Zhang, L., Wang, E.N., Goodson, K.E., and T.W. Kenny, "Phase Change Phenomena in Silicon Microchannels," International Journal of Heat and Mass Transfer 48, 1572-1582, 2005.

Wang, E.N., Devasenathipathy, S., Santiago, J.G., Goodson, K.E., and T.W. Kenny,"Nucleation and Growth of Vapor Bubbles in a Heated Silicon Microchannel," Journal of Heat Transfer 126, 497, 2004.

Wang, E.N., Zhang, L., Jiang, L., Koo, J.-M., Maveety, J.G., Sanchez, E.A., Goodson,K.E., and T.W. Kenny, "Micromachined Jets for Liquid Impingement Cooling of VLSI Chips," Journal of MicroElectroMechanical Systems 13, 833-842, 2004.

Balandin, A., Wang, K.L., Cai, S., Li, R., Viswanathan, C.R., Wang, E.N., and M.Wojtowicz, "Investigation of Flicker Noise Level and Deep Levels in AlGaN/GaN Heterostructure Field Effect Transistors," Journal of Electronic Materials, 29, 297-301, 2000.

Brian L. Wardle
Charles Stark Draper Assistant Professor
Department of Aeronautics and Astronautics

COLLABORATORS
H.-M. Duong, MIT XVI Postdoc
E. J. Garcia, Gamesa
R. Guzman deVilloria, MIT XVI Postdoc
A. J. Hart, Univ. of Michigan
K.F. Jensen, Chem. E.
W.-S. Kim, MIT XVI Postdoc
S.-G. Kim, MechE
S.-H. Kim, Brown Univ.
S. Maruyama, Univ. of Tokyo
A. Miravete, Univ. Zaragoza
D. Papavassiliou, Univ. Oklahoma
L. Rocha, Univ. of Minho
M. A. Schmidt, EECS
A. H. Slocum, MechE
S.M. Spearing, Univ. Southampton
C. Thompson, DMSE
M. Toner, HST
H. L. Tuller, DMSE
N. Wicks, Schlumberger

GRADUATE STUDENTS
J. Blanco, Visiting Student, AA
H. Cebeci, Visiting Student, AA
F. Fachin, Res. Asst., AA
Stacy Figueredo, Res. Asst., MechE
K. Ishiguro, Visiting Student, AA
M. Kim, Res. Asst., DMSE
L. Megalini, Visiting Student, AA
S. Pont, Visiting Student, AA
S. Steiner, Res. Asst., AA
S. Wicks, Res. Asst., AA
N. Yamamoto, Res. Asst., AA

UNDERGRADUATE STUDENTS
D. Barber, AA
H. Jeffrey, AA
D. S. Saito, ITA (visiting)
M. Tsai, AA

SUPPORT STAFF
J. Kane, Research Specialist
P. Lee, Financial Officer
M. Prendergast, Admin. Asst. II

Wardle, B.L., and S.M. Spearing, "Chapter 9, Structural Considerations," ed. by A. Mitsos and P.I. Barton, *Microfabricated Power Generation Devices: Design and Technology*, Wiley-VCH, Weinheim, 2009. ISBN: 978-3-527-32081-3.

Duong, H.M., Yamamoto, N., Papavassiliou, D.V., Maruyama, S., and B.L. Wardle "Inter Carbon Nanotube Contact in Thermal Transport of Controlled-Morphology Polymer Nanocomposites," *Nanotechnology*, Vol. 20, 2009.

Yamamoto, N., Hart, A.J., Garcia, E.J., Wicks, S., Duong, H.M., Slocum, A.H., and B.L. Wardle, "High-yield Growth and Morphology Control of Aligned Carbon Nanotubes on Ceramic Fibers for Multifunctional Enhancement of Structural Composites," *Carbon*, Vol. 47 (3), March 2009, pp. 551-560.

Blanco, J., Garcia, E.J., Guzman deVilloria, R., and B.L. Wardle, "Limiting Mechanisms in Mode I Interlaminar Toughness of Composites Reinforced with Aligned Carbon Nanotubes," *J. Composite Materials*, Vol. 43 (8), April 2009.

Duong, H., Papavassiliou, D.V., Mullen, K.J., Wardle, B.L., and S. Maruyama, "Calculated Thermal Properties of Single Walled Carbon Nanotube Suspensions," *J. Physical Chemistry C*, 112 (50), 2008, pp. 19860-65.

Bello, D., Wardle, B.L, Ahn, K., Yamamoto, N., Garcia, E.J., Hart, A.J., and M.J. Ellenbecker, "Exposure to Nanoscale Particles and Fibers During Fabrication and Machining of Hybrid CNT Advanced Composites," *J. Nanoparticle Research*, Vol. 11, 2009, pp. 231-249.

Garcia, E.J., Wardle, B.L., and A.J. Hart, "Joining Prepreg Composite Interfaces with Aligned Carbon Nanotubes," *Composites Part A*, Vol. 39, 2008, pp. 1065-1070.

Wardle, B.L., Saito, D.S., Garcia, E.J., Hart, A.J., and R. Guzman deVilloria, "Fabrication and Characterization of Ultra-High Volume Fraction Aligned Carbon-Nanotube-Polymer Composites," *Advanced Materials*, Vol. 20, 2008, pp. 2707-14.

Garcia, E.J., Hart, J., and B.L. Wardle, "Long Carbon Nanotubes Grown on the Surface of Fibers for Hybrid Composites," *AIAA Journal*, Vol. 46, No.6, 2008, pp.1405-1412.

Bello, D., Hart, A.J., Ahn, K., Hallock, M., Yamamoto, N., Garcia, E.J., Ellenbecker, E.J., and B.L. Wardle, "Particle Exposure Levels During CVD Growth and Subsequent Handling of Vertically-aligned Carbon Nanotube Films," *Carbon*, Vol. 46, 2008, pp. 974-978.

Garcia, E.J., Wardle, B.L., Hart, A.J., and N. Yamamoto, "Fabrication and Multifunctional Properties of a Hybrid Laminate with Aligned Carbon Nanotubes Grown In Situ," *Composites Science & Technology*, Vol. 68, No. 9, 2008, pp. 2034-2041.

Quinn, D., Wardle, B.L., and Spearing, S.M., "Residual Stress and Microstructure of As-deposited and Annealed Sputtered Yttria Stabilized Zirconia Thin Films," *Journal of Materials Research*, Vol. 23, No. 3, March, 2008, pp.609-618.

Garcia, E.J., Hart, J., Wardle, B.L. and A. Slocum, "Fabrication and Nanocompression Testing of Aligned CNT/Polymer Nanocomposites," *Advanced Materials*, 19:2151-2156, August 2007.

duToit, N.E. and B. L. Wardle, "Experimental Verification of Models for Microfabricated Piezoelectric Vibration Energy Harvesters," *AIAA Journal*, Vol. 45, No. 5, May 2007, pp. 1126-1137.

Garcia, E.J., Hart, J., Wardle, B.L. and A. Slocum, "Fabrication of Composite Microstructures by Capillarity-driven Wetting of Aligned Carbon Nanotubes with Polymers," *Nanotechnology*, Vol. 18, No. 16, April 2007, pages 165602 (11pp).

duToit, N.E., and B.L. Wardle, "Performance of Microfabricated Piezoelectric Vibration Energy Harvesters," *Integrated Ferroelectrics*, Vol. 83, 2006, pp.13-23.

duToit, N. E., Wardle, B. L., and S.-G. Kim, "Design Considerations for MEMS-scale Piezoelectric Vibration Energy Harvesters," *Integrated Ferroelectrics*, Vol. 71, 2005, pp. 121-160.

THESES AWARDED, 2008–2009

S.B.

Chao, A.
(K. K. Berggren)
Salty Development of an Optical Photoresist

Collins, K.
(C. Livermore)
Computational Fluid Dynamic (CFD) Optimization of Microfluidic Mixing in a MEMS Steam Generator

Mieville, F.
(T. Palacios)
Suitability of GaN HEMTs for Digital Electronics

Quinones, L.
(C. Livermore)
Carbon Nanotubes: A Study on Assembly Methods

S.M.

Alexander, B. A.
(E. N. Wang)
Design of a Microbreather for Two-Phase Microchannel Devices

Chung, H. W.
(A. P. Chandrakasan)
A Low-Power AES Processor with DPA-Resistance

Communal, A.
(D. S. Boning)
Challenges Faced by a Global Team: the Case of the Tool Reuse Program at Intel

Georgas, M.
(V. M. Stojanovic)
An Optical Data Receiver for Integrated Photonic Interconnects

George, D.
(D. S. Boning, C. Fine)
Understanding the Effects of Larger Wafers on the Global Semiconductor Equipment Supply Chain

He, D.
(C. G. Sodini)
An Organic Thin-Film Transistor Circuit for Large Area Temperature Sensing

Hill, T.
(C. Livermore)
Energy Storage in Carbon Nanotube Supersprings

Hu, X.
(K. K. Berggren)
Coupling Light to Superconductive Photon Counters

Jin, Y.
(H. L. Tuller)
Toxic Gas Sensors using Thin Film Transistor Platform at Low Temperature

Lee, S.
(A. P. Chandrakasan and H.-S. Lee)
Front-end Design ofUltrasound Image System

Leu, J.
(K. K. Berggren)
Templated Self-Assembly of sub-10 nm Quantum Dots

Leu, C. Y.
(V. M. Stojanovic)
A 9GHz Injection Locked Loop Optical Clock Receiver in 32-nm CMOS

Li, L.
(J. Han)
Immunoassay Sensitivity and Kinetic Enhancement in Cell Culture Media using Electrokinetic Preconcentration

Liu, V.
(J. Han)
Development of an Integrated Capillary valve-based Preconcentrator and a Surface-based Immunoassay

Lu, K.
(C. G. Sodini)
Digital Phase Tightening for Improved Spatial Resolution in Millimeter-Wave Imaging Systems

Mittal, S.
(S. N. Bhatia)
Micropatterned Cell Arrays for Detecting DNA Damage

Moss, B.
(V. M. Stojanovic)
Charge-Injection Circuits for Monolithic Silicon-Photonic Devices: Switches and Modulators

Nabanja, S.
(L. A. Kolodziejski)
Design and Fabrication of Quantum-Dot Lasers

Peck, J.
(S. G. Kim)
Securing the Safety Net: Applying Manufacturing Systems Methods towards Understanding and Redesigning a Hospital Emergency Department

Pulitzer, S.
(D. S. Boning)
Transitioning Technology from R&D to Production

Schmitt, C.
(A. P. Chandrakasan)
Carbon Nanotube-Based Nanorelays for Low-Power Circuit Applications

Schoener, D.
(C. G. Sodini)
Supply Chain Risk Management Through Bill of Materials & Component Analysis

Winston, D.
(K. K. Berggren)
Nodal Photolithography: Lithography via Far-Field Optical Nodes in the Resist

Yip, M.
(A. P. Chandrakasan)
A Highly Digital, Reconfigurable and Voltage Scalable SAR ADC

Zhou, H.
(M. A. Schmidt)
Micromechanical actuators for insect flight mechanics

M.Eng.

Harrison, B.
(J. A. del Alamo)
Expanding the Capabilities of ELVIS iLabs using Component Switching

Henry, W.
(V. M. Stojanovic)
System Architecture for a Mode-Matched MEMS Gyroscope

Liang, H.
(A. P. Chandrakasan)
A High Speed Image Transmission System for Ultra-Wideband Wireless Links

Ma, Y.
(V. M. Stojanovic)
Companding Techniques for High Dynamic Range Audio CODEC Receiver Path

Mukherjee, K.
(H. L. Tuller)
Electrospun Nanofibers – Opportunities in Environment and Energy

Nagarajan, R.
(C. V. Thompson)
Commercialization of Low Temperature Cu Thermocompression Wafer Bonding for 3DI

Price, M.
(V. M. Stojanovic)
Asynchronous Data-dependent Jitter Compensation

Qixun, W.
(C. V. Thompson)
Commercialization of Gallium Nitride Nanorod Arrays on Silicon for Solid-State Lighting

Shamir, O.
(L. A. Kolodziejski)
Development of Ultra-Broadband Modulators

Song, Y.
(H. L. Tuller)
Oxide Based Thermoelectric Materials for Large Scale Power Generation

Ph.D.

Anikeeva, P.
(V. Bulovic)
Physical Properties and Design of Light-Emitting Devices Based on Organic Materials and Nanoparticles

Bhardwaj, M.
(A. P. Chandrakasan)
Communications Under Observation Constraints

Bora, M.
(M. A. Baldo)
Chemical and biosensors

Bradley, M. S.
(V. Bulovic)
Engineering J-Aggregate Cavity Exciton-Polariton Devices

Daly, D.
(A. P. Chandrakasan)
Digital ADCs and Ultra-Wideband RF Circuits for Energy Constrained Wireless Applications

Dauler, E.
(K. K. Berggren)
Multi-element superconducting nanowire single-photon detectors

Drego, N.
(D. S. Boning, A. P. Chandrakasan)
Characterization and Mitigation of Process Variation in Digital Circuits and Systems

Finchelstein, D.
(A. P. Chandrakasan)
Low-Power Techniques for Video Decoding

Giermann, A.
(C. V. Thompson)
Templated Dewetting of Thin Solid Films

Harris, T. J.
(S. N. Bhatia)
Nanoparticle Coatings for Spatial and Temporal Control of Cancer Imaging and Therapy

Hill, T.
(C. Livermore)
Microchemical Systems for Singlet Oxygen Generation

Ho, J.
(V. Bulovic)
Organic Lateral Heterojunction Devices for Vapor-phase Chemical Detection

Ickes, N.
(A. P. Chandrakasan)
A Micropower DSP for Sensor Applications

Lee, J.-K.
(D. A. Antoniadis)
Design and Characterization of Si/SiGe Heterostructure sub-100-nm p-MOSFET

Leib, J.
(C. V. Thompson)
Relationships Between Grain Structure and Stress in Thin Volmer-Weber Metallic films

Lim, D.
(D. S. Boning)
Characterization of Process Variability and Robust Optimization of Analog Circuits

Litzelman, S.
(H. L. Tuller)
Modification of Space Charge Transport in Nanocrystalline Cerium Oxide by Heterogeneous Doping

Nayfeh, O.
(D. A. Antoniadis)
Nonvolatile Memory Devices with Colloidal, 1.0 nm Silicon Nanoparticles: Principles of Operation, Fabrication, Measurements, and Analysis

Nessim, G. D.
(C. V. Thompson)
Carbon Nanotube Synthesis for Integrated Circuit Interconnects

Powell, J.
(C. G. Sodini)
SiGe Receiver Front End and Packaged Wideband Antennas for Millimeter-Wave Passive Imaging

Ramadass, Y.
(A. P. Chandrakasan)
Energy Processing Circuits for Low-Power Applications

Sou, K. C.
(L. Daniel, A. Megretski)
A Quasi-Convex Optimization Approach to Parameterized Model Order Reduction

Verma, N.
(A. P. Chandrakasan)
Ultra-Low-Power SRAM Design in High Variability Advanced CMOS

von Maltzahn, G.
(S. N. Bhatia)
A Systems Approach to Engineering Cancer Nanotechnologies

Wee, K. H.
(R. Sarpeshkar)
An Analog VLSI Vocal Tract

Yang, J.
(K. K. Berggren)
Advancements in superconducting nanowire single photon detectors and development of fabrication methods for sub-10-nm lithography

Yen, B.
(J. H. Lang)
A Fully-Integrated Multi-Watt Permanent-Magnet Turbine Generator

Zhak, S. M
(R. Sarpeshkar)
Modeling and Design of an Active Silicon Cochlea

VLSI MEMO SERIES

MTL maintains a comprehensive Memo Series covering the activities of MTL and related microsystems research at MIT. A chronological list of memos issued from 2008-present appears below Copies of MTL Memos are available online exclusively to members of the Microsystems Industrial Group (MIG) at MTL.

MIG members are invited to sign up for an account that will grant them access to these materials in a password-protected directory. Visit our website at mtlweb.mit.edu for more information and current memos.

08-2044	Improving OLED Technology for Displays	J. Yu
08-2045	Characterization of Process Variability and Robust Optimization of Analog Circuits	D. Lim
08-2046	Advanced Materials, Process, and Designs for Silicon Photonic Integration	R. Sun
09-2047	Charge Recombination in Organic Small-molecule Solar Cells	Jiye Lee
09-2048	Engineering J-Aggregate Cavity Exciton-Polariton Devices	M. Scott Bradley
09-2049	Collective Analog Bioelectronic Computation	S. Mandal
09-2050	A High Speed Image Transmission System for Ultra-Wideband Wireless Links	H. Liang
09-2051	Fabrication of Critical-Angle Transmission Gratings for High Efficiency X-ray Spectroscopy :	M. Ahn
09-2052	Modeling and Design of an Active Silicon Cochlea	S. M. Zhak
09-2053	Circuit Design for Logic Automata	K. Chen
09-2054	Nanofluidic System for Single Molecule Manipulation and Analysis	Y. Sen
09-2055	Design and Fabrication of Quantum-Dot Lasers	S. Nabanja
09-2056	An Organic Thin-Im Transistor Circuit for Large-area Temperature-sensing	D. He
09-2057	Carbon Nanotube-Based Nanorelays for Low-Power Circuit Applications	C. Schmitt
09-2058	Digital ADCs and Ultra-Wideband RF Circuits for Energy C onstrained Wireless Applications	D. Daly
09-2059	Reliability of GaN High Electron Mobility Transistors on Silicon Substrates	S. Demirtas
09-2060	Computationally Efficient Characterization of Standard Cells for Statistical Static Timing Analysis	S. Chou
09-2061	A Test Structure for the Measurement and Characterization of Layout-Induced Transistor Variation	A. Chang
09-2062	Chip-Scale Quadrupole Mass Filters for a Micro-Gas Analyzer	Kerry Cheung
09-2063	Advanced Materials, Process, and Designs for Silicon Photonic Integration	Rong Sun
09-2064	Ultra-Low-Power SRAM Design In High Variability Advanced CMOS	Naveen Verma
09-2065	A Highly Digital, Reconfigurable and Voltage Scalable SAR ADC	Marcus Yip
09-2066	Low-Power Techniques for Video Decoding	Daniel Finchelstein
09-2067	Communications in the Observation Limited Regime	Manish Bhardwaj
09-2068	Modeling of Advanced Integrated Circuit Planarization Processes: Electrochemical-Mechanical Planarization (eCMP), STI CMP using Non-Conventional Slurries	Joy Johnson

MTL SEMINAR SERIES

MTL hosts a series of talks each semester known as the MTL Seminar Series. Speakers for the series are selected on the basis of their knowledge and competence in the areas of microelectronics research, manufacturing, or policy. The series is held on the MIT Campus during the academic year on Tuesdays at 4:00 pm. The seminar series is open to the public. A listing of recent seminars is also provided at http://mtlweb.mit.edu.

Streaming videos of the series are available online exclusively to individuals whose companies are members of the Microsystems Industrial Group at MTL. For more information regarding the MTL Seminar Series, send e-mail to valeried@mit.edu.

Fall 2008

September 30
Lakshminarayan Srinivasan, Ph.D; Massachusetts General Hospital
Fast responses without false starts: Dorsal anterior cingulate cortex in simple reactive behavior

October 7
Alyssa Apsel, Ph.d, Cornell University
Mixed Signal Electronics in a Digital Environment

October 21
Dr. Umesh Mishra, UCSB
Could Gallium Nitride and Silicon be the dominant semiconductors in the future?

October 28
Dr. Martin Izzard, Texas Instruments
Gaining Focus: Developing an "Applications-Oriented" Approach to Multicore Processor Architectures

November 4
Dr. Mark Pinto, Applied Materials
Has The Sun Finally Risen on Photovoltaics?

November 18
Mondira Pant, Ph.D, Intel
Challenges in avoiding an unruly power grid in microprocessors

November 18
Marc Baldo, MIT
Excitonics

December 9
Polina Anikeeva
MTL Doctoral Dissertation Seminar: Physical Properties and Design of Light-Emitting Devices Based on Organic Materials and Nanoparticles

Spring 2009

February 4
Stephen Senturia, Professor Emeritus, MIT; Chairman and CTO, Polychromix
Peanuts vs. Pyramids: Two Perspectives on MEMS

March 3
Beth Pruitt, Assistant Professor of Mechanical Engineering, Stanford University
Microsystems and Mechanotransduction

March 31
Susanne Paul, Black Sand Technologies
Class P Architectures in Linear 3G CMOS Power Amplifiers

April 7
David Arnold, University of Florida
Micromagnets for Microsystems

April 14
Subhasish Mitra
Robust System Design in Scaled CMOS and Emerging Nanotechnologies

April 28
Julia Greer, California Institute of Technology
Mechanical Properties of Materials at Nanoscale

May 5
Christoph Lang, Bosch Research & Technology Center
MEMS Sensors

May 12
Soumyajit Mandal
MTL Doctoral Dissertation Seminar: Collective Analog Bioelectric Computation

ABBREVIATIONS

AFOSR.....Air Force Office of Scientific Research (US)

AFOSR MURI.....Air Force Office of Scientific Research Multi-Disciplinary University Research Initiative (US)

AMD.....Advanced Micro Devices, Inc.

ARL.....Army Research Laboratory (US)

ARL MURI.....Army Research Laboratory Multi-Disciplinary University Research Initiative (US)

ARO.....Army Research Office (US)

BP .....British Petroleum

CICS .....Center for Integrated Circuits and Systems (MIT)

CMSE .....Center for Materials Science and Engineering (MIT)

DARPA.....Defense Advanced Research Projects Agency (US)

DARPA COSMOS.....Defense Advanced Research Projects Agency Compound Semiconductor Materials on Silicon program (US)

DARPA YFA .....Defense Advanced Research Projects Agency Young Faculty Award (US)

DoD .....Department of Defense (US)

DoD NDSEG .....Department of Defense National Defense Science and Engineering Graduate Fellowship (US)

DOE.....Department of Energy (US)

DURINT.....Defense University Research Initiative on Nanotechnology (US)

IARPA.....Intelligence Advanced Research Projects Activity (US)

IBM.....International Business Machines

INSIC.....Information Storage Industry Consortium

ISN.....Institute for Soldier Nanotechnologies (MIT)

KACST .....King Abdulaziz City for Science & Technology

KFAS.....Korea Foundation for Advanced Studies

KFUPM-MIT Research Program .....King Fahd University of Petroleum and Minerals - MIT Research Program (MIT)

KIST .....Korea Institute of Science and Technology

KIST-MIT .....Korea Institute of Science and Technology-MIT Collaboration

MIT .....Massachusetts Institute of Technology (MIT)

MITEI.....MIT Energy Initiative (MIT)

MTL .....Microsystems Technology Laboratories (MIT)

MURI.....Multidisciplinary University Research Initiative (US)

NASA .....National Aeronautics and Space Adminsitration (US)

NCI .....National Cancer Institute (US)

NDSEG .....National Defense Science and Engineering Graduate fellowship (US)

NIH .....National Institutes of Health (US)

NIH NIBIB .....National Institute of Biomedical Imaging and Bioengineering (US)

NOAA .....National Oceanic and Atmospheric Administration (US)

NRI/INDEX .....National Research Initiative (US)

NSERC .....Natural Sciences and Engineering Research Council of Canada

NSF.....National Science Foundation (US)

NSF CAREER.....NSF Faculty Early Career Development Program (US)

NSF GRFP .....NSF Graduate Research Fellowships Program

NSF MRSEC.....NSF Materials Research Science and Engineering Center

NSF NNIN.....NSF National Nanotechnology Infrastructure Network

ONR .....Office of Naval Research (US)

OSU NSEC.....Ohio State University Nanoscale Science and Engineering Center

PECASE .....Presidential Early Career Award for Scientists and Engineers (US)

RLE .....Research Laboratory of Electronics (MIT)

SRC.....Semiconductor Research Corporation

SRC/FCRP C2S2.....Semiconductor Research Corporation/ Focus Center Research Program,Center for Circuits and Systems Solutions

SRC/FCRP IFC .....Semiconductor Research Corporation/ Focus Center Research Program. Interconnect Focus Center

SRC/FCRP MSD .....Semiconductor Research Corporation/ Focus Center Research Program Materials, Structures and Devices

STTR.....Small Business Technology Transfer

TSMC .....Taiwan Semiconductor Manufacuring Corp.

INDEX